National Semiconductor

November 1994

54F/74F190
Up/Down Decade Counter with Preset and Ripple Clock

General Description

The ’F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the ’F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

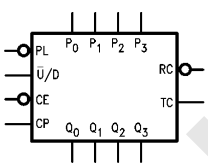
- High-speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

Commercial	Military	Package Number	Package Description
74F190PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F190DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F190SC (Note 1)		M16A	16-Lead (0.150″ Wide) Molded Small Outline, JEDEC
	54F190FM (Note 2)	W16A	16-Lead Cerpack
	54F190LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



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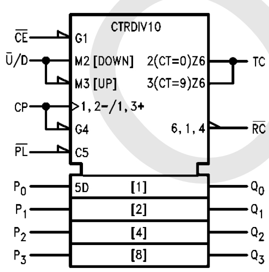
IEEE/IEC



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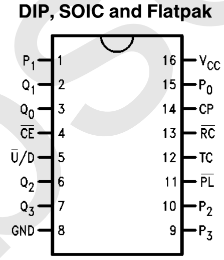
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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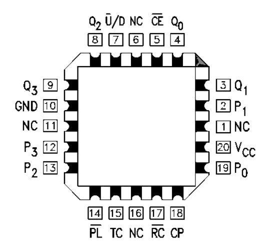
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F U.L. HIGH/LOW	54F/74F Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/3.0	20 µA/−1.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/−0.6 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/−0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 µA/−0.6 mA
$\overline{U}$/D	Up/Down Count Control Input	1.0/1.0	20 µA/−0.6 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	−1 mA/20 mA
$\overline{RC}$	Ripple Clock Output (Active LOW)	50/33.3	−1 mA/20 mA
TC	Terminal Count Output (Active HIGH)	50/33.3	−1 mA/20 mA

Functional Description

The 'F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table, $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the 'F191 data sheet.

$\overline{RC}$ Truth Table

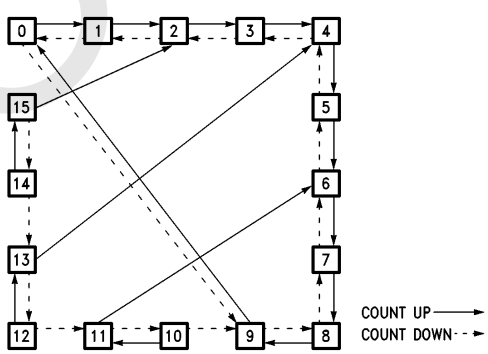
Inputs $\overline{CE}$	Inputs TC*	Inputs CP	Output $\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Clock Transition
⊔ = LOW Pulse

Mode Select Table

Inputs $\overline{PL}$	Inputs $\overline{CE}$	Inputs $\overline{U}$/D	Inputs CP	Mode
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

State Diagram



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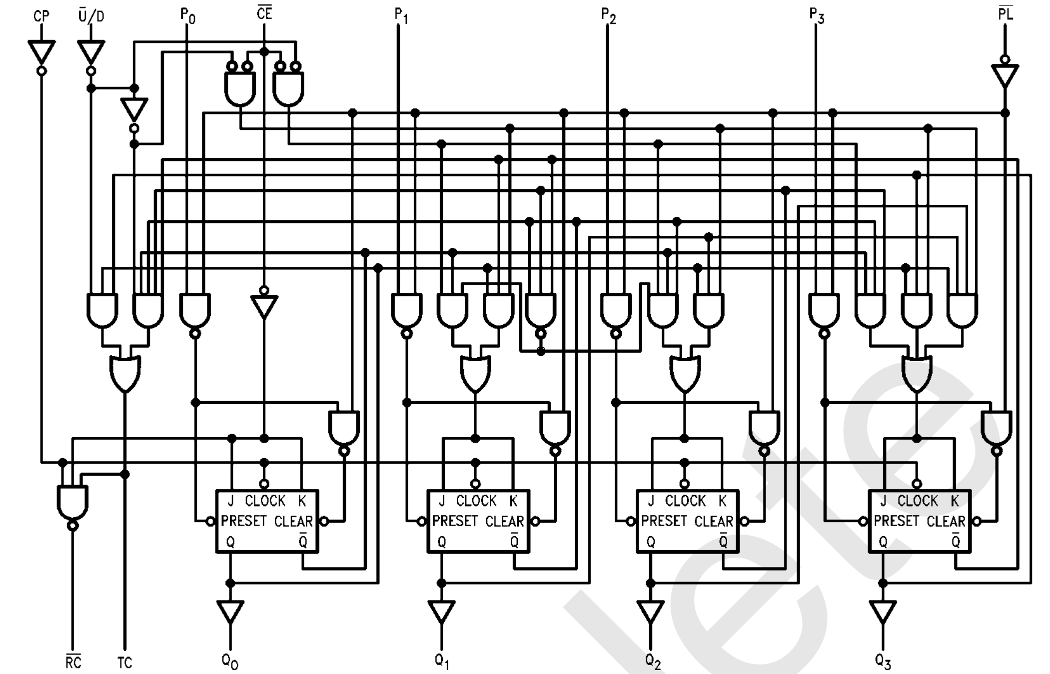
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 74F 10% V_{CC} 74F 5% V_{CC}	2.5 2.5 2.7			V	Min	I_{OH} = −1 mA I_{OH} = −1 mA I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC} 74F 10% V_{CC}			0.5 0.5	V	Min	I_{OL} = 20 mA I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6 −1.8	mA	Max	V_{IN} = 0.5V, except $\overline{CE}$ V_{IN} = 0.5V, $\overline{CE}$
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCL}	Power Supply Current			38	55	mA	Max	V_O = LOW

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} =$ Mil $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	125		75		90		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 5.0	5.5 8.5	7.5 11.0	3.0 5.0	9.5 13.5	3.0 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC	6.0 5.0	10.0 8.5	13.0 11.0	6.0 5.0	16.5 13.5	6.0 5.0	14.0 12.0	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.0 3.0	5.5 5.0	7.5 7.0	3.0 3.0	9.5 9.0	3.0 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.0 3.0	5.0 5.5	7.0 7.0	3.0 3.0	9.0 9.0	3.0 3.0	8.0 8.0	
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	7.0 5.5	11.0 9.0	18.0 12.0	7.0 5.5	22.0 14.0	7.0 5.5	20.0 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{TC}$	4.0 4.0	7.0 6.5	10.0 10.0	4.0 4.0	13.5 12.5	4.0 4.0	11.0 11.0	
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 6.0	4.5 10.0	7.0 13.0	3.0 6.0	9.0 16.0	3.0 6.0	8.0 14.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	5.0 5.5	8.5 9.0	11.0 12.0	5.0 5.5	13.0 14.5	5.0 5.5	12.0 13.0	ns

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units
		Min	Max	Min	Max	Min	Max	
t_s(H) t_s(L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	4.5 4.5		6.0 6.0		5.0 5.0		ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	2.0 2.0		2.0 2.0		2.0 2.0		
t_s(L)	Setup Time, LOW $\overline{CE}$ to CP	10.0		10.5		10.0		ns
t_h(L)	Hold Time, LOW $\overline{CE}$ to CP	0		0		0		
t_s(H) t_s(L)	Setup Time, HIGH or LOW $\overline{U}$/D to CP	12.0 12.0		12.0 12.0		12.0 12.0		ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW $\overline{U}$/D to CP	0 0		0 0		0 0		
t_w(L)	$\overline{PL}$ Pulse Width, LOW	6.0		8.5		6.0		ns
t_w(L)	CP Pulse Width, LOW	5.0		7.0		5.0		ns
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.0		7.5		6.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 190 S C X

Temperature Range Family
- 74F = Commercial
- 54F = Military

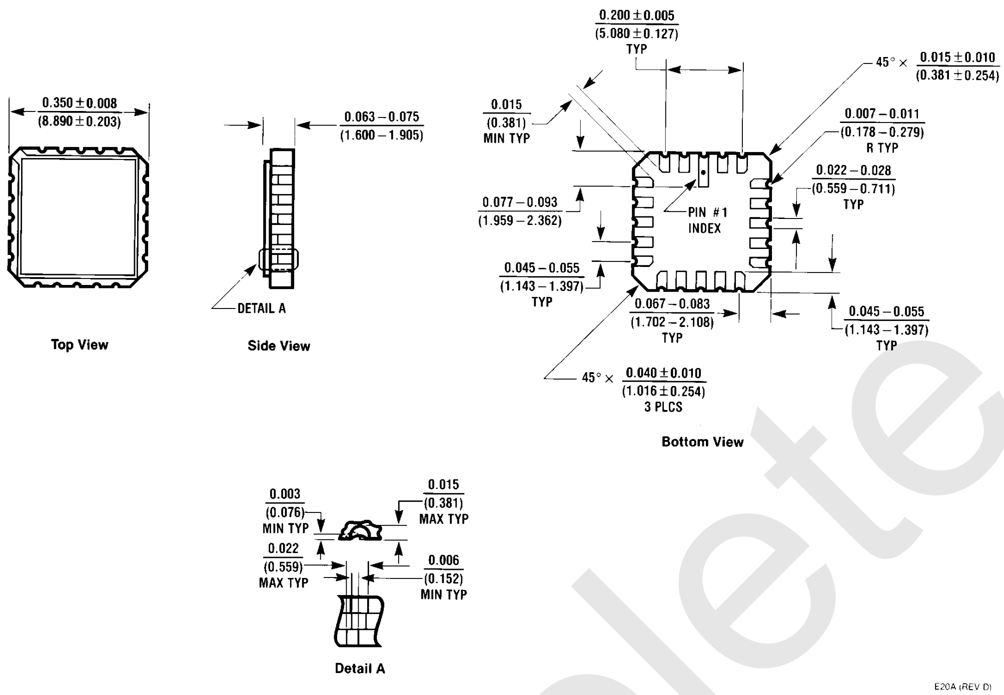
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier (LCC)
- S = Small Outline SOIC JEDEC

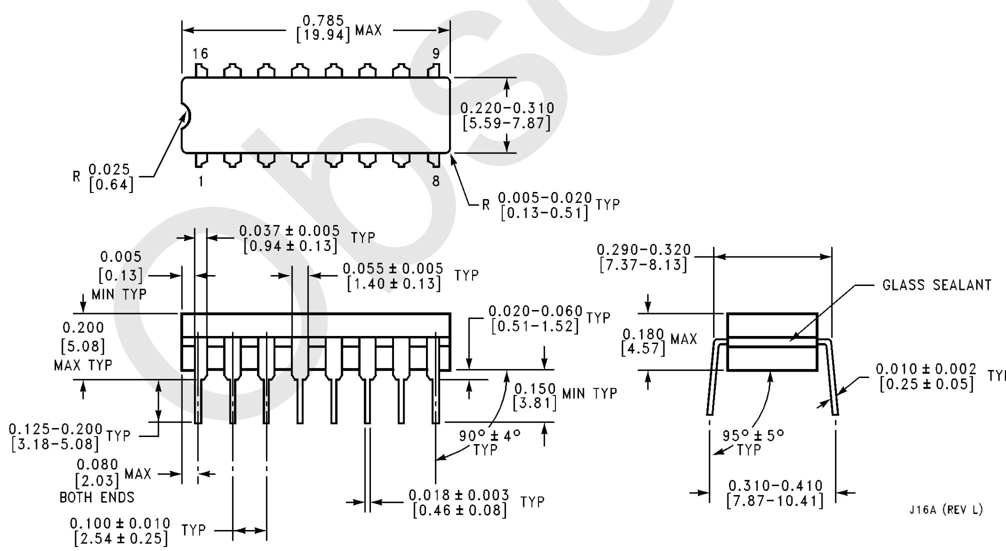
Special Variations
- X = Devices shipped in 13″ reels
- QB = Military grade device with environmental and burn-in processing shipped in tubes

Temperature Range
- C = Commercial (0°C to +70°C)
- M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

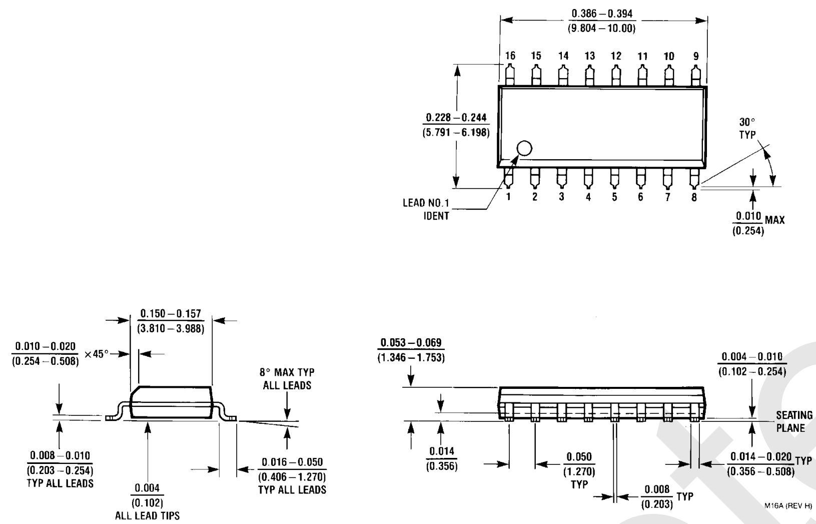


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

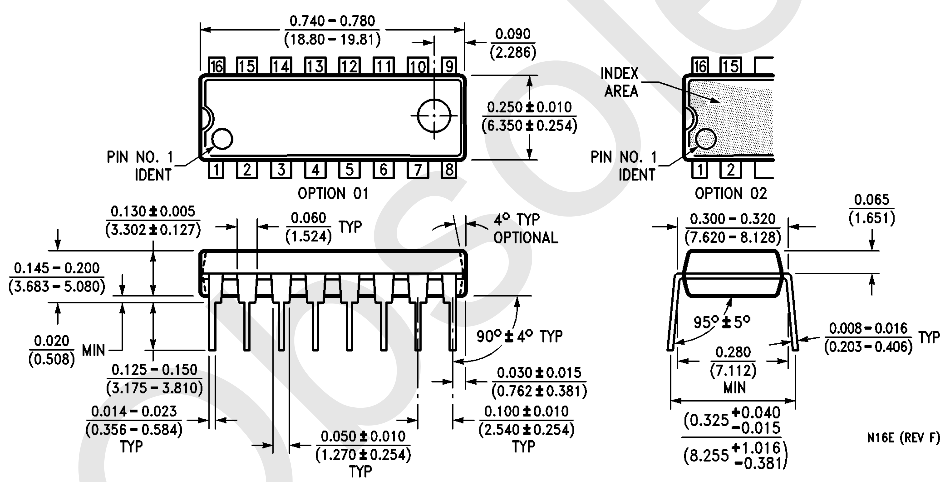


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

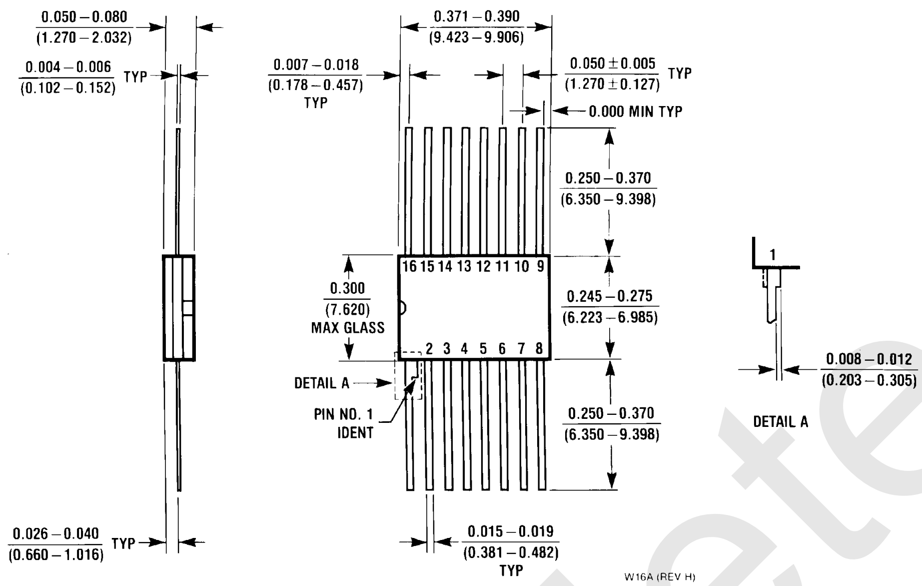


16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A



16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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