

ESD7272

ESD Protection Diodes, Low Capacitance, Dual Channel

The ESD7272 is designed to protect various IOs and data lines from ESD. The low capacitance and low ESD clamping voltage combined with a high standoff voltage makes this device an ideal solution for protecting various types of ICs without causing signal degradation. The small, cost efficient SOT-23 package allows for easy PCB layout and BOM reduction on multiple pin modules.

Features

- Low Capacitance: < 3.0 pF
- Protection for the Following IEC & ISO Standards:
 - ◆ IEC 61000-4-2 (Level 4)
 - ◆ ISO 10605
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Sensor Lines
- PWM Inputs/Outputs
- General I/Os
- Automotive

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

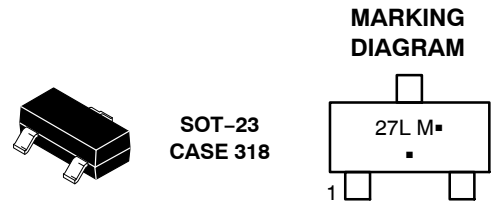
Rating	Symbol	Value	Unit
IEC 61000-4-2 Contact	ESD	±15	kV
IEC 61000-4-2 Air		±15	
ISO 10605 330 pF / 330 Ω Contact		±12	
ISO 10605 330 pF / 2 kΩ Contact		±25	
ISO 10605 150 pF / 2 kΩ Contact		±30	
Operating Junction Temperature Range	T _{J(max)}	-55 to +175	°C
Storage Temperature Range	T _{stg}	-55 to +175	°C
Lead Solder Temperature – Maximum (10 Second Duration)	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



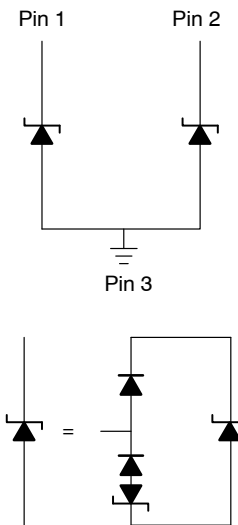
ON Semiconductor®

www.onsemi.com



27L = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

PIN CONFIGURATIONS AND SCHEMATICS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

ESD7272

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Any I/O to GND			24	V
Breakdown Voltage	V_{BR}	$I_T = 1 \text{ mA}$, Any I/O to GND	27	29	36	V
Forward Voltage	V_F	$I_T = 100 \text{ mA}$, GND to Any I/O	2.0	6.0		V
Reverse Leakage Current	I_R	$V_{RWM} = 24 \text{ V}$, Any I/O to GND		0.2	1000	nA
Clamping Voltage	V_C	$I_{PP} = 1 \text{ A}$, Any I/O to GND (8/20 μs pulse)		38	40	V
Clamping Voltage (Note 1)	V_C	IEC61000-4-2, $\pm 8\text{kV}$ Contact	See Figures 3 & 4			
Clamping Voltage TLP (Note 2)	V_C	$I_{PP} = 8 \text{ A}$		38		V
		$I_{PP} = 16 \text{ A}$		41		V
		$I_{PP} = -8 \text{ A}$		-8.0		V
		$I_{PP} = -16 \text{ A}$		-10.5		V
Junction Capacitance	C_J	$V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$ between Any I/O and GND		1.3	2.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For text procedures see Application Note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 4 \text{ ns}$, averaging window; $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$.

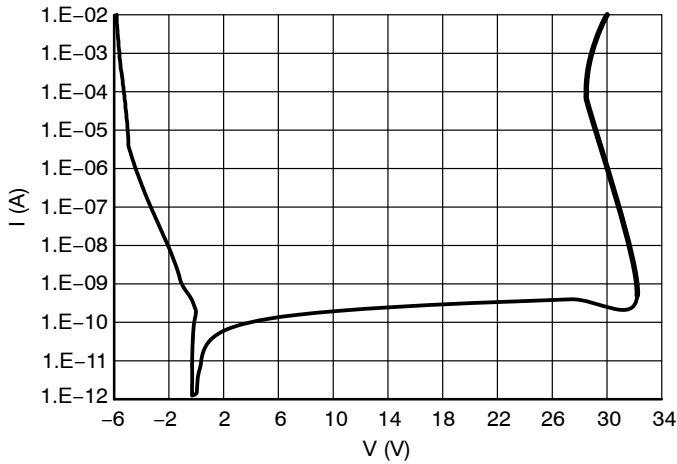


Figure 1. IV Characteristics

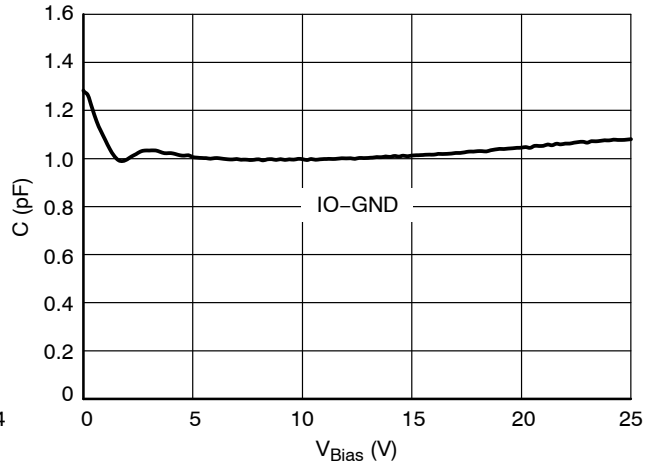


Figure 2. CV Characteristics

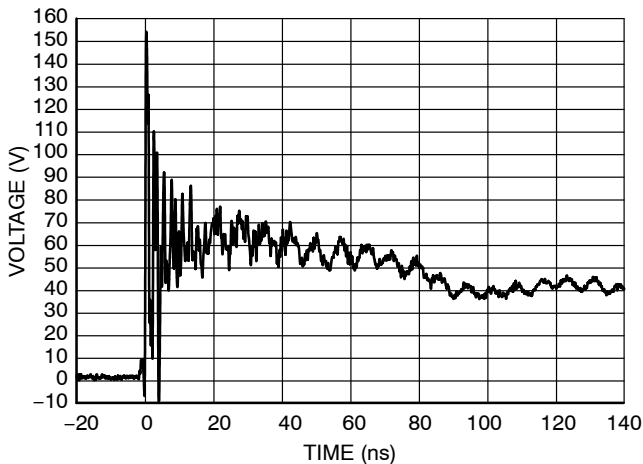


Figure 3. IEC61000-2-4 +8 kV Contact Clamping Voltage

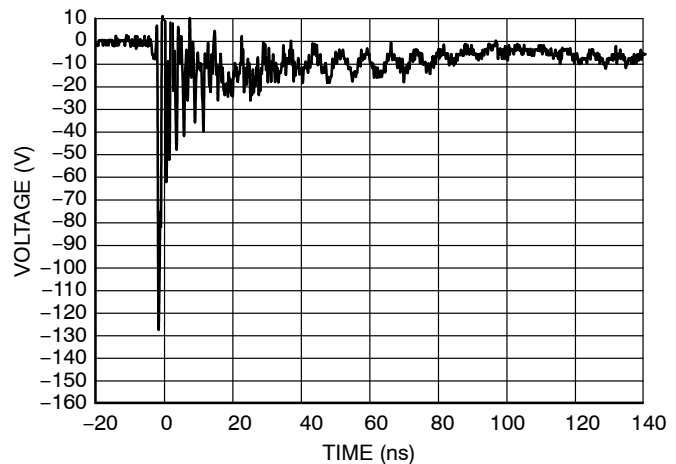


Figure 4. IEC61000-2-4 -8 kV Contact Clamping Voltage

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 5. IEC61000-4-2 Spec

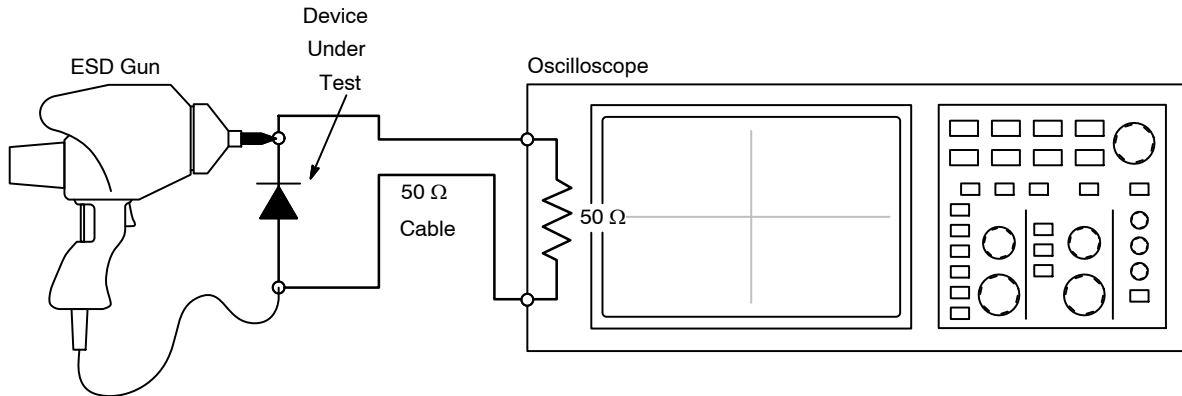


Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

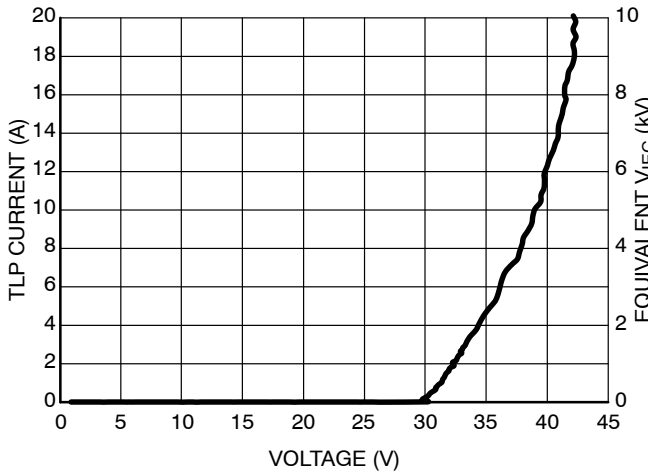


Figure 7. Positive TLP IV Curve

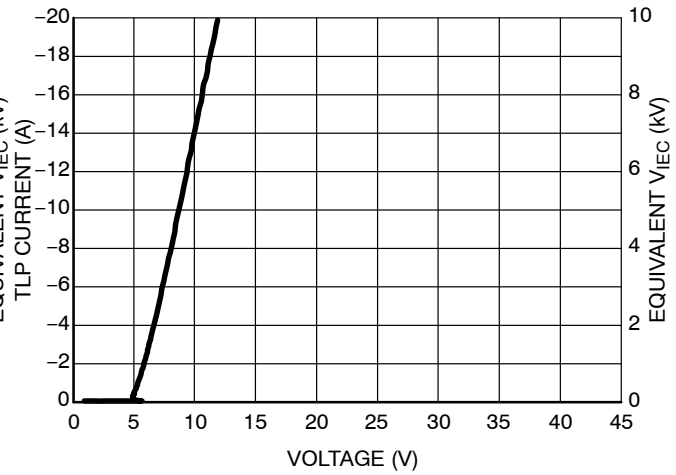


Figure 8. Negative TLP IV Curve

NOTE: TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 300 \text{ ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

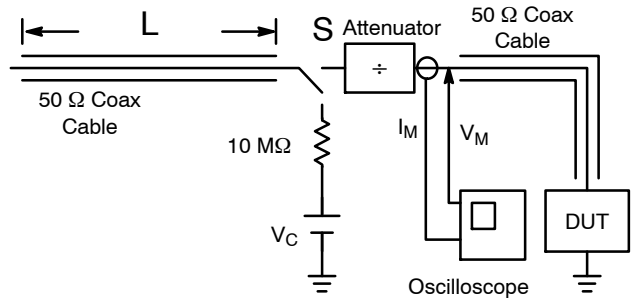


Figure 9. Simplified Schematic of a Typical TLP System

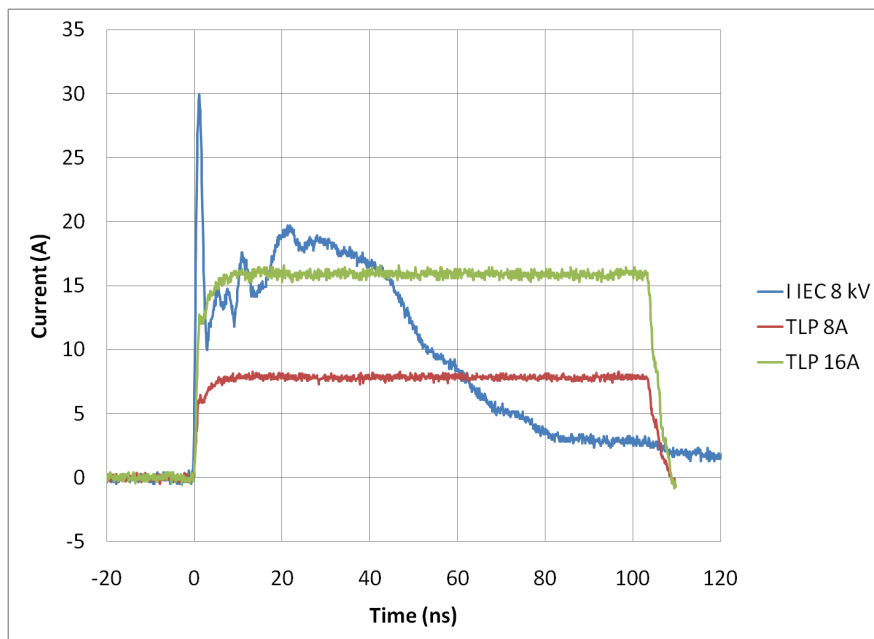


Figure 10. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

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ORDERING INFORMATION

Device	Marking	Package	Shipping†
ESD7272LT1G	27L	SOT-23 (Pb-Free)	3000 / Tape & Reel
SZESD7272LT1G*			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

- | | | | | | |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:
CANCELLED | STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE | | |
| STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE | STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE | STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE | STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE | STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE | STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE-ANODE | STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE |
| STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT | STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE | STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION |
| STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE | STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE | | | | |

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