

## 74ALVC132

### Low Voltage Quad 2-Input NAND Gate with Schmitt Trigger Inputs and 3.6V Tolerant Inputs and Outputs

#### General Description

The ALVC132 contains four 2-input NAND gates with Schmitt Trigger Inputs. The pin configuration and function are the same as the ALVC00 except the inputs have hysteresis between the positive-going and negative-going input thresholds. This hysteresis is useful for transforming slowly switching input signals into sharply defined, jitter-free output signals. This product should be used where noise margin greater than that of conventional gates is required.

The ALVC132 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

This product is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

#### Features

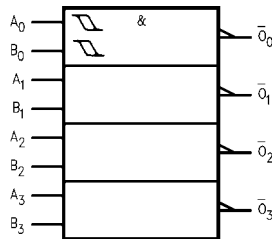
- 1.65V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ 
  - 3.8 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.6 ns max for 2.3V to 2.7V  $V_{CC}$
  - 8.2 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 250V

#### Ordering Code:

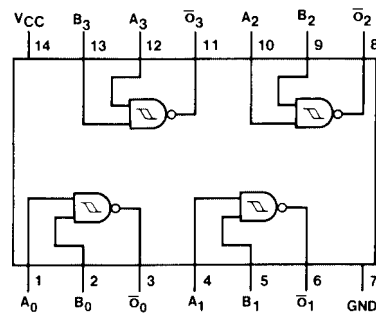
Order Number	Package Number	Package Description
74ALVC132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ALVC132MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Diagram



#### Connection Diagram



#### Pin Descriptions

Pin Name	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V
Output Voltage ( $V_O$ ) (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ ) $V_O < 0V$	-50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 3)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ ) $V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V

**Note 1:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 3:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units	
$V_{T+}$	Positive Threshold		1.65		1.3	V	
			2.3		1.6		
			3.0		2.0		
			3.6		2.2		
$V_{T-}$	Negative Threshold		1.65	0.25		V	
			2.3	0.5			
			3.0	0.7			
			3.6	0.8			
$V_H$	Input Hysteresis		1.65	0.2	0.9	V	
			2.3	0.3	1.0		
			3.0	0.3	1.2		
			3.6	0.3	1.2		
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V	
			$I_{OH} = -4$ mA	1.65	1.2		
			$I_{OH} = -6$ mA	2.3	2		
			$I_{OH} = -12$ mA	2.3	1.7		
				2.7	2.2		
				3.0	2.4		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	V	
			$I_{OL} = 4$ mA	1.65	0.45		
			$I_{OL} = 6$ mA	2.3	0.4		
			$I_{OL} = 12$ mA	2.3	0.7		
				2.7	0.4		
				3	0.55		
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		$\pm 5.0$	$\mu A$	
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		$\pm 10$	$\mu A$	
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$	
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	$\mu A$	

AC Electrical Characteristics										
Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus	1.1	3.8	1.3	4.6	0.8	4.1	1.0	8.2	ns

Capacitance						
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units	
			V <sub>CC</sub>	Typical		
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	6	pF	
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	7	pF	
C <sub>PD</sub>	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 50 pF	3.3	20	pF
				2.5	20	

AC Loading and Waveforms		TABLE 1. Values for Figure 1				
		<table border="1"> <thead> <tr> <th>TEST</th> <th>SWITCH</th> </tr> </thead> <tbody> <tr> <td>t<sub>PLH</sub>, t<sub>PHL</sub></td> <td>Open</td> </tr> </tbody> </table>	TEST	SWITCH	t <sub>PLH</sub> , t <sub>PHL</sub>	Open
	TEST	SWITCH				
t <sub>PLH</sub> , t <sub>PHL</sub>	Open					

FIGURE 1. AC Test Circuit

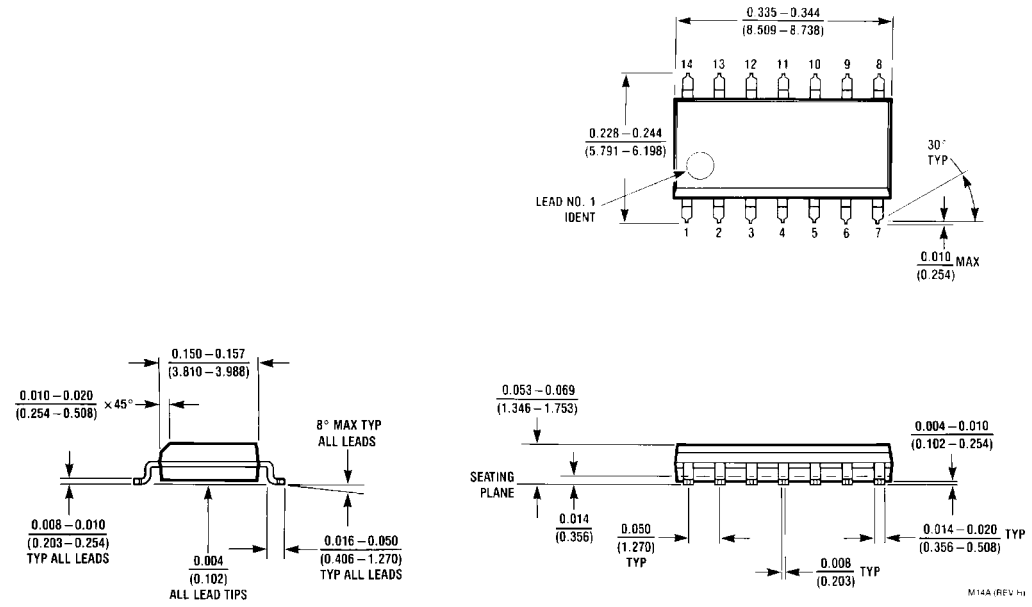
TABLE 2. Variable Matrix  
(Input Characteristics: f = 1MHz; t<sub>r</sub> = t<sub>f</sub> = 2ns; Z<sub>0</sub> = 50Ω)

Symbol	V <sub>CC</sub>			
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V	1.8V ± 0.15V
V <sub>mi</sub>	1.5V	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>mo</sub>	1.5V	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2

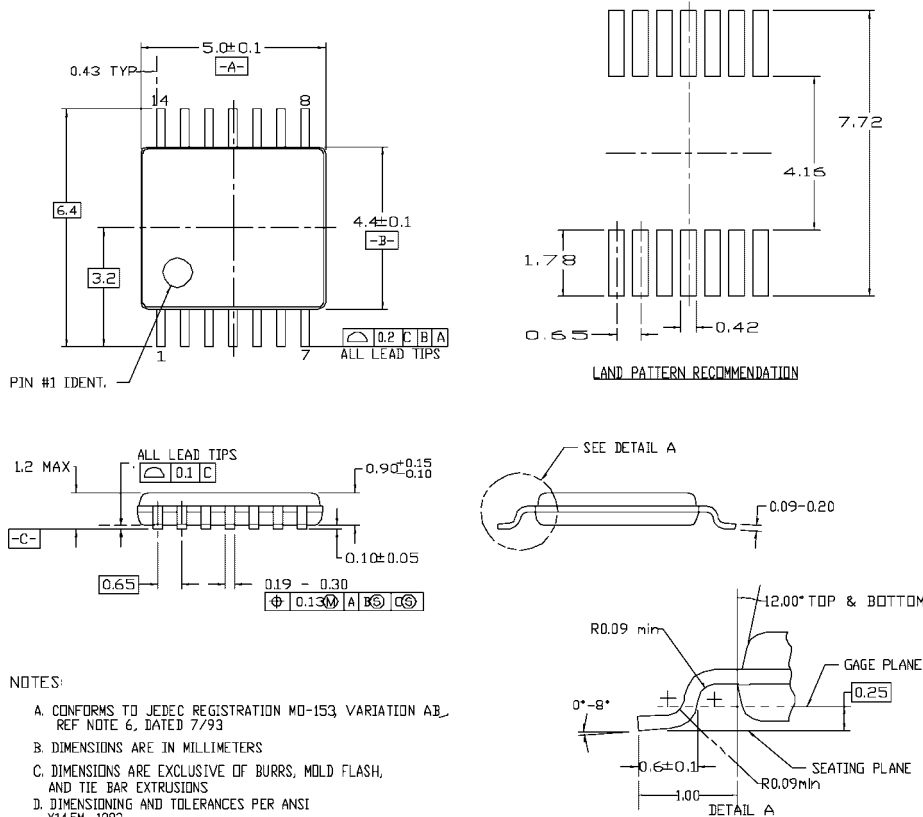
FIGURE 2. Waveform for Inverting and Non-inverting Functions

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
  - B. DIMENSIONS ARE IN MILLIMETERS
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

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