MC74HC161A, MC74HC163A

Presettable Counters
High−Performance Silicon−Gate CMOS

The MC74HC161A and HC163A are identical in pinout to the LS161 and LS163. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

The HC161A and HC163A are programmable 4−bit binary counters with asynchronous and synchronous reset, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

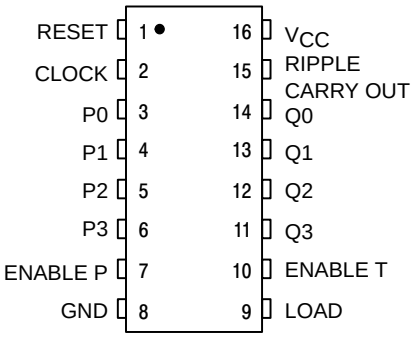

Figure 1. Pin Assignment

FUNCTION TABLE

Inputs					Output
Clock	Reset*	Load	Enable P	Enable T	Q
↗	L	X	X	X	Reset
↗	H	L	X	X	Load Preset Data
↗	H	H	H	H	Count
↗	H	H	L	X	No Count
↗	H	H	X	L	No Count

*HC163A only. HC161A is an Asynchronous Reset Device
H = high level, L = low level, X = don't care

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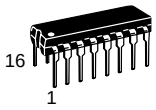
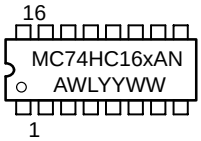
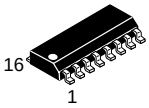
MARKING DIAGRAMS

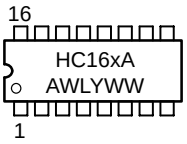


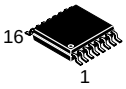
PDIP−16
N SUFFIX
CASE 648



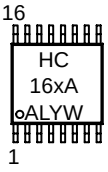


SO−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



x = 1 or 3
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC161AN	PDIP−16	2000/Box
MC74HC161AD	SOIC−16	48/Rail
MC74HC161ADR2	SOIC−16	2500/Reel
MC74HC161ADT	TSSOP−16	96/Rail
MC74HC161ADTR2	TSSOP−16	2500/Reel
MC74HC163AN	PDIP−16	2000/Box
MC74HC163AD	SOIC−16	48/Rail
MC74HC163ADR2	SOIC−16	2500/Reel
MC74HC163ADT	TSSOP−16	96/Rail
MC74HC163ADTR2	TSSOP−16	2500/Reel

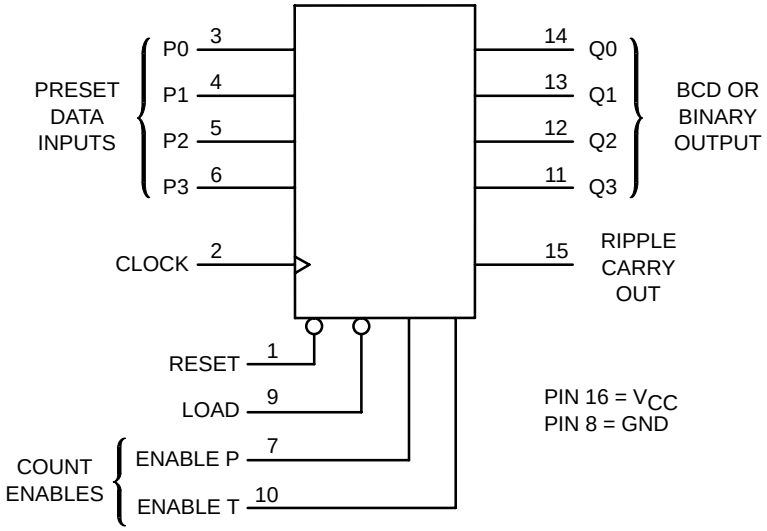


Figure 2. Logic Diagram

DEVICE/MODE TABLE

Device	Count Mode	Reset Mode
HC161A	Binary	Asynchronous
HC163A	Binary	Synchronous

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to V_{CC} +0.5	V
V_O	DC Output Voltage	(Note 2)	−0.5 ≤ V_O ≤ V_{CC} +0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±25	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
I_{GND}	DC Ground Current per Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	C
T_J	Junction Temperature Under Bias		+150	C
θ_{JA}	Thermal Resistance	PDIP SOIC TSSOP	78 112 148	C/W
P_D	Power Dissipation in Still Air at 85 C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL−94−VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 >1000	V
$I_{LATCH-UP}$	Latch−Up Performance	Above V_{CC} and Below GND at 85 C (Note 6)	±300	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage	(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	C
t_r, t_f	Input Rise and Fall Time (Figure 4)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

7. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25 C	≤ 85 C	≤ 125 C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 3.6$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 3.6$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

8. Information on typical parametric values can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Figure	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25 C	≤ 85 C	≤ 125 C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Note 9)	4, 10	2.0 3.0 4.5 6.0	6 15 30 35	5 12 24 28	4 10 20 24	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	4, 10	2.0 3.0 4.5 6.0	120 75 20 16	160 120 23 20	200 150 28 22	ns
t_{PHL}		4, 10	2.0 3.0 4.5 6.0	145 100 22 18	185 135 25 20	220 150 30 23	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC161A Only)	5, 10	2.0 3.0 4.5 6.0	145 100 20 17	185 135 22 19	220 150 25 21	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out	6, 10	2.0 3.0 4.5 6.0	110 60 16 14	150 115 18 15	190 140 20 17	ns
t_{PHL}		6, 10	2.0 3.0 4.5 6.0	135 100 18 15	175 130 20 16	210 160 22 20	ns
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out	4, 10	2.0 3.0 4.5 6.0	120 75 22 18	160 135 27 22	200 150 30 25	ns
t_{PHL}		4, 10	2.0 3.0 4.5 6.0	145 100 22 20	185 135 28 24	220 150 35 28	ns
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC161A Only)	5, 10	2.0 3.0 4.5 6.0	155 120 22 18	190 140 26 22	230 155 30 25	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	5, 10	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	4, 10	—	10	10	10	pF

9. Applies to noncascaded/nonsynchronous clocked configurations only with synchronously cascaded counters. (1) Clock to Ripple Carry Out propagation delays. (2) Enable T or Enable P to Clock setup times and (3) Clock to Enable T or Enable P hold times determine f_{max}. However, if Ripple Carry out of each stage is tied to the Clock of the next stage (nonsynchronously clocked) the f_{max} in the table above is applicable. See Applications information in this data sheet.
10. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate) (Note 11)	45	pF

11. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Figure	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25 C	≤ 85 C	≤ 125 C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock	8	2.0 3.0 4.5 6.0	40 20 15 12	60 30 20 18	80 40 30 20	ns
t_{su}	Minimum Setup Time, Load to Clock	8	2.0 3.0 4.5 6.0	60 25 15 12	75 30 20 18	90 40 30 20	ns
t_{su}	Minimum Setup Time, Reset to Clock (HC163A Only)	7	2.0 3.0 4.5 6.0	60 25 20 17	75 30 25 23	90 40 35 25	ns
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock	9	2.0 3.0 4.5 6.0	80 35 20 17	95 40 25 23	110 50 35 25	ns
t_h	Minimum Hold Time, Clock to Load or Preset Data Inputs	8	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_h	Minimum Hold Time, Clock to Reset (HC163A Only)	7	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_h	Minimum Hold Time, Clock to Enable T or Enable P	9	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (HC161A Only)	5	2.0 3.0 4.5 6.0	80 35 15 12	95 40 20 17	110 50 26 23	ns
t_{rec}	Minimum Recovery Time, Load Inactive to Clock	8	2.0 3.0 4.5 6.0	80 35 15 12	95 40 20 17	110 50 26 23	ns
t_w	Minimum Pulse Width, Clock	4	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_w	Minimum Pulse Width, Reset (HC161A Only)	5	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_r, t_f	Maximum Input Rise and Fall Times		2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

FUNCTION DESCRIPTION

The HC161A/163A are programmable 4−bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count−enable controls.

The HC161A and HC163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2)

The internal flip−flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading, occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip−flops and appear at the counter outputs. P0 (Pin 3) is the least−significant bit and P3 (Pin 6) is the most−significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least−significant bit and Q3 (Pin 11) is the most−significant bit.

Ripple Carry Out (Pin 15)

When the counter is in its maximum state, 1111, this output goes high, providing an external look−ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \bullet Q0 \bullet Q1 \bullet Q2 \bullet Q3$$

OUTPUT STATE DIAGRAMS

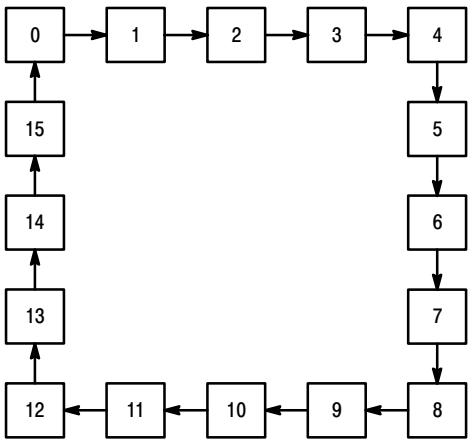


Figure 3. Binary Counters

CONTROL FUNCTIONS

Resetting

A low level on the Reset pin (Pin 1) resets the internal flip−flops and sets the outputs (Q0 through Q3) to a low level. The HC161A resets asynchronously, and the HC163A resets with the rising edge of the Clock input (synchronous reset).

Loading

With the rising edge of the Clock, a low level on Load (Pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip−flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Count Enable/Disable

These devices have two count−enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \bullet \text{Enable T} \bullet \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count−enable control: Enable T is both a count−enable and a Ripple−Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	**Enable P**	**Enable T**	**Q0 − Q3**	**Ripple Carry Out**
H	H	H	Count	High when Q0−Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0−Q3 are maximum*
X	X	L	No Count	L

*Q0 through Q3 are maximum when Q3, Q2, Q1, Q0 = 1111.

SWITCHING WAVEFORMS

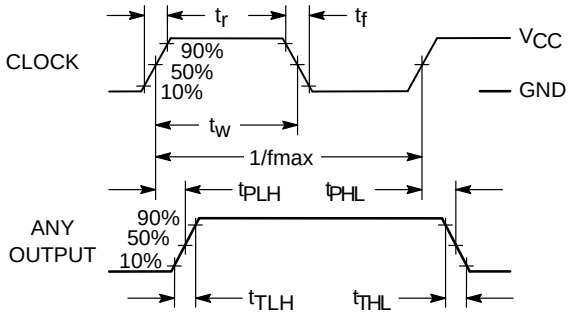


Figure 4.

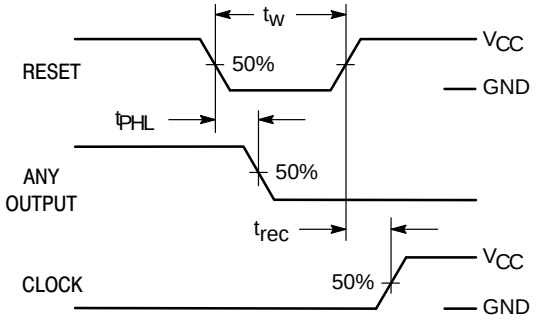


Figure 5.

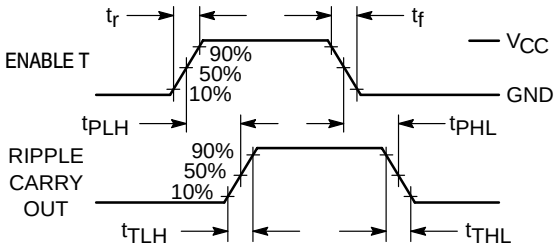


Figure 6.

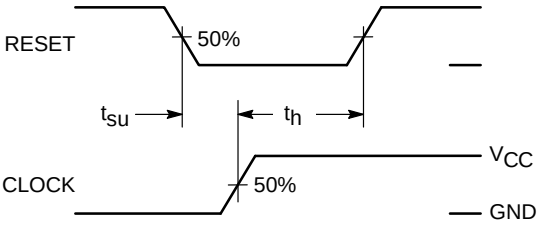


Figure 7. HC163A Only

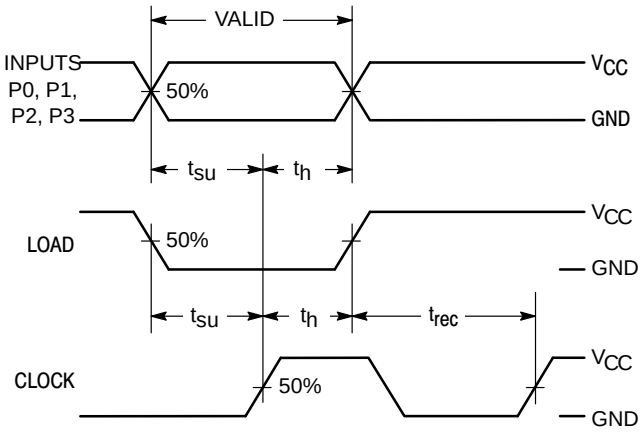


Figure 8.

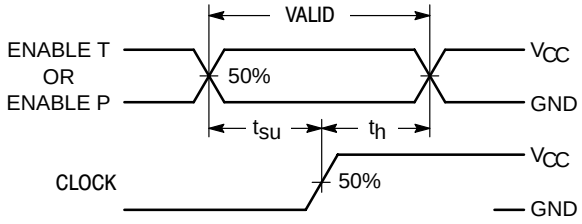
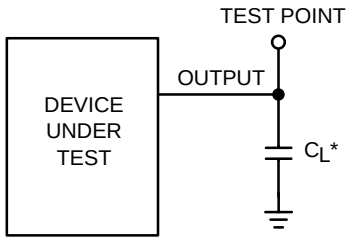


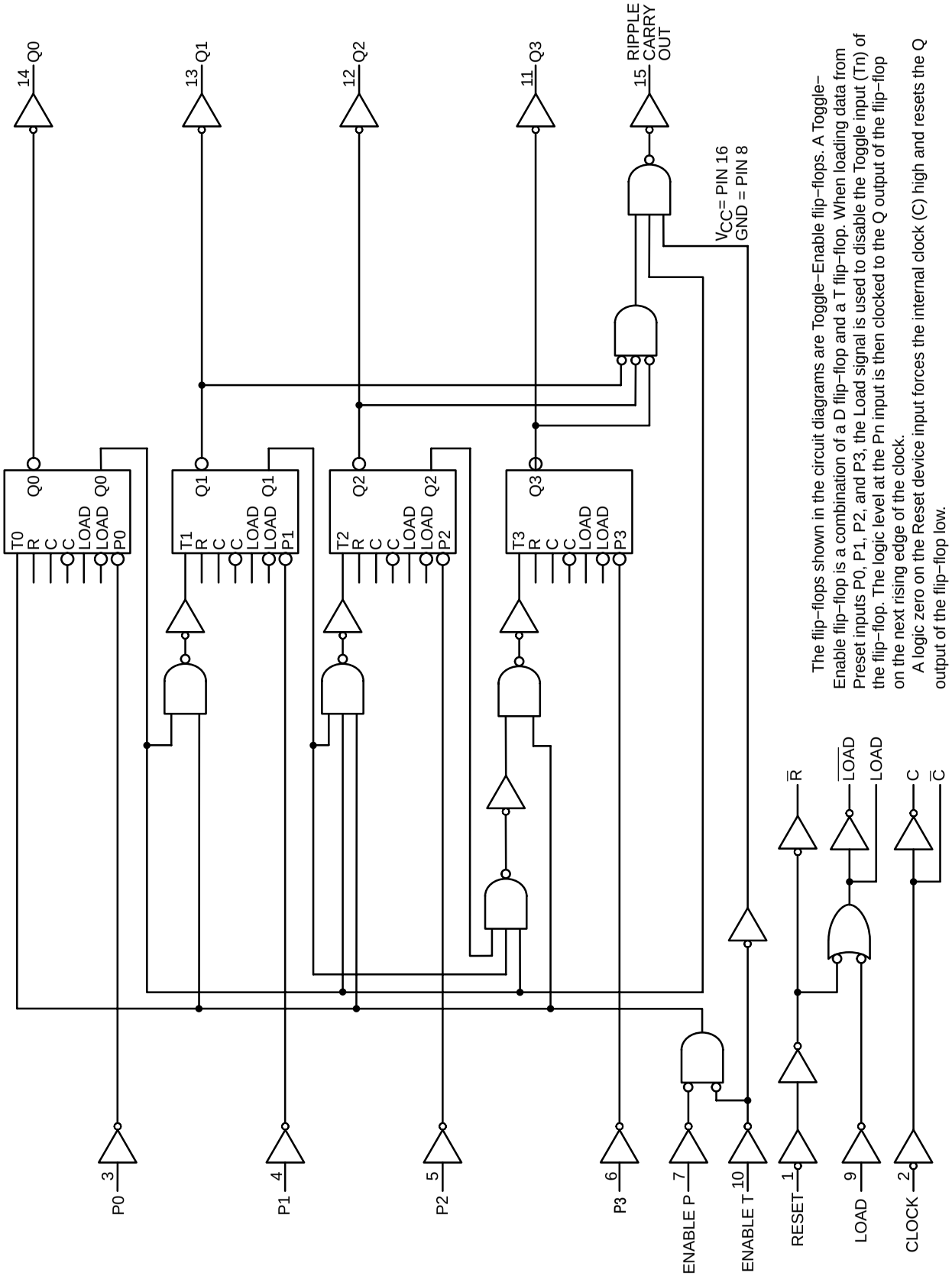
Figure 9.

TEST CIRCUIT



*Includes all probe and jig capacitance

Figure 10.



The flip−flops shown in the circuit diagrams are Toggle−Enable flip−flops. A Toggle−Enable flip−flop is a combination of a D flip−flop and a T flip−flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip−flop. The logic level at the Pn input is then clocked to the Q output of the flip−flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip−flop low.

Figure 11. 4−Bit Binary Counter with Asynchronous Reset (MC74HC161A)

Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.

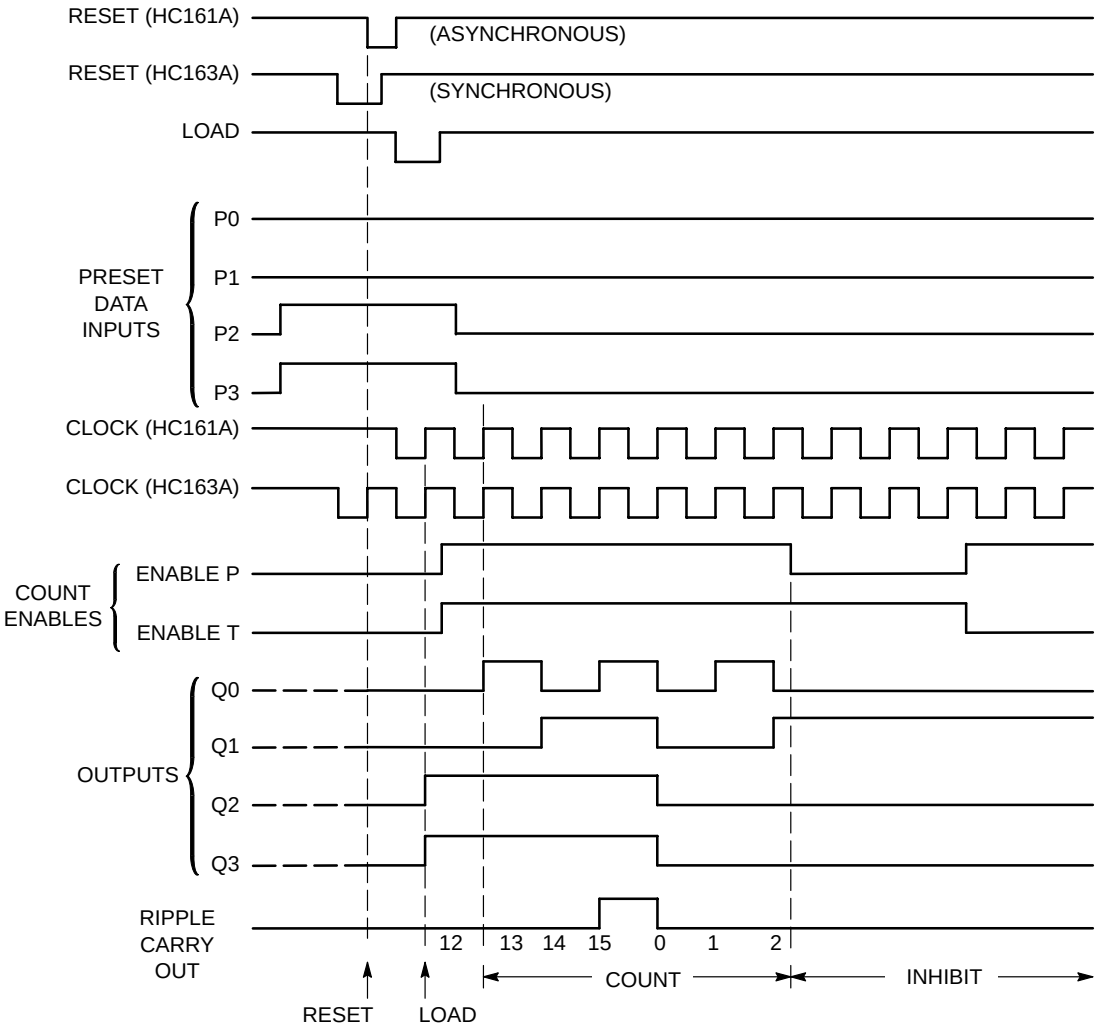


Figure 12. Timing Diagram

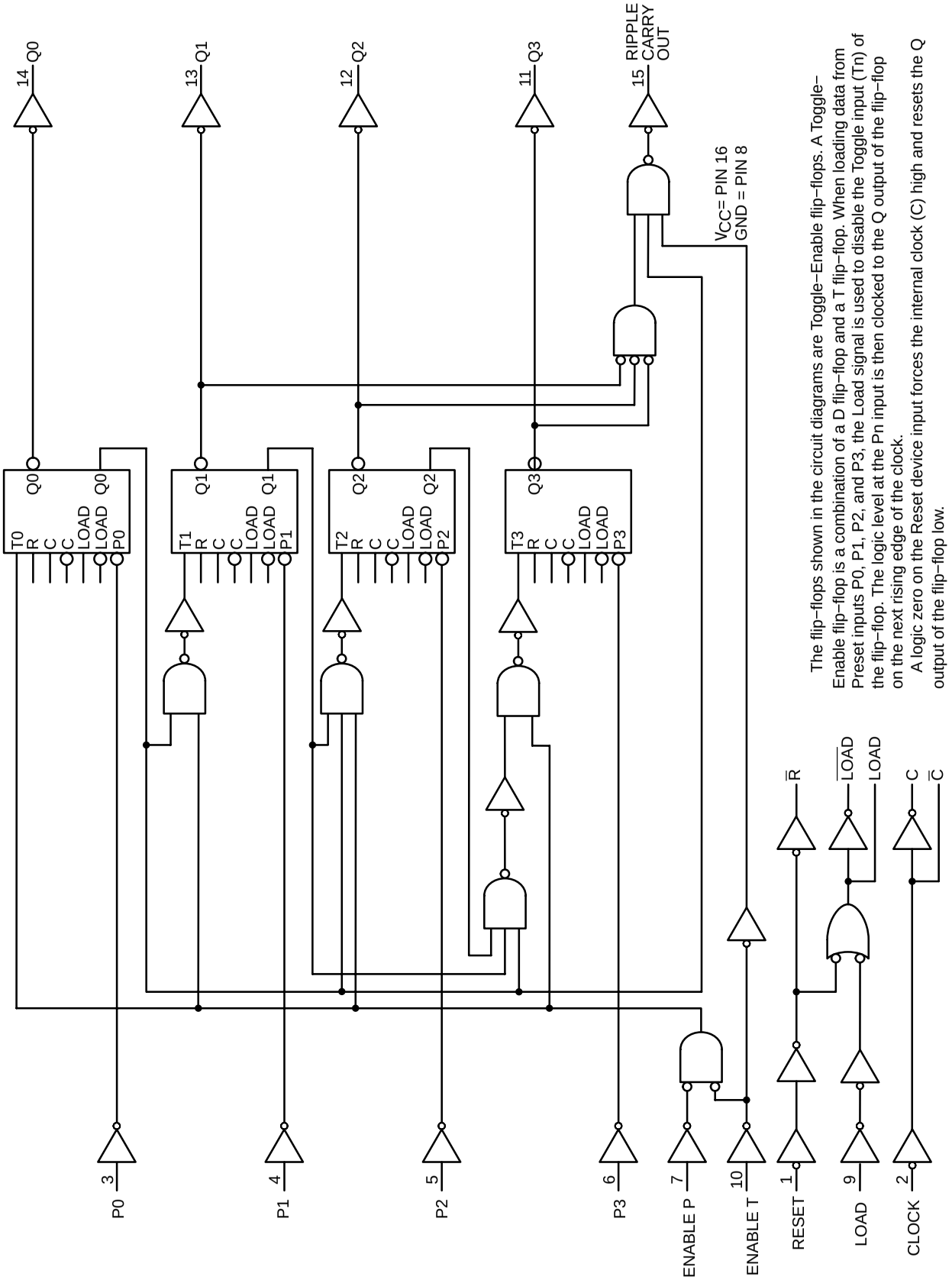
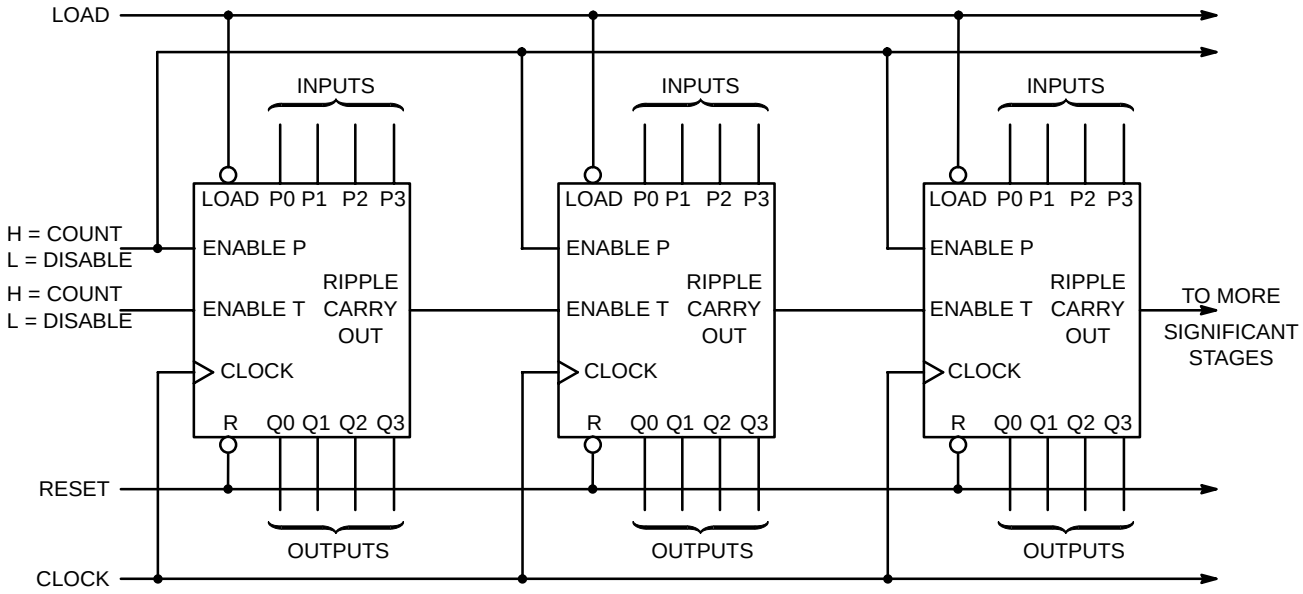


Figure 13. 4−Bit Binary Counter with Synchronous Reset (MC74HC163A)

TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Figure 14. N−Bit Synchronous Counters

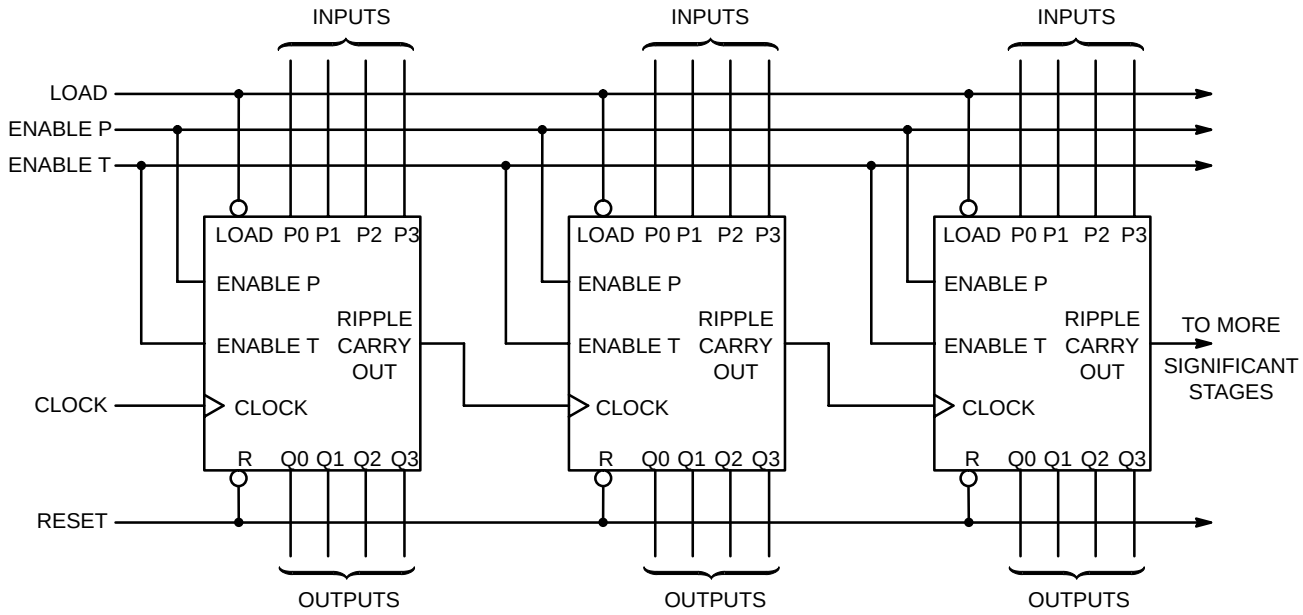


Figure 15. Nibble Ripple Counter

TYPICAL APPLICATIONS VARYING THE MODULUS

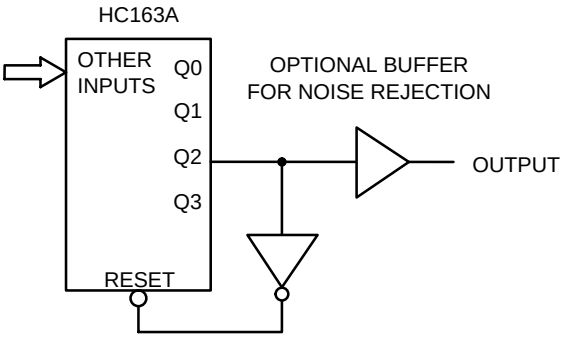


Figure 16. Modulo−5 Counter

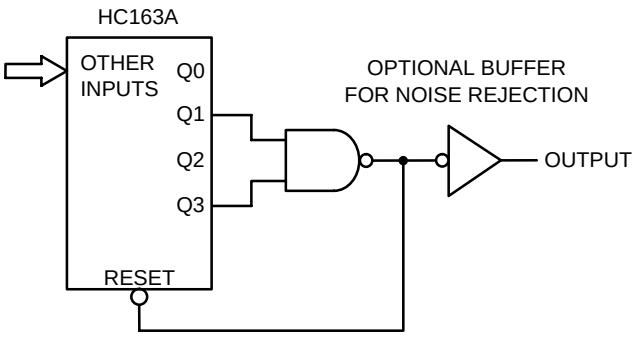


Figure 17. Modulo−11 Counter

The HC163A facilitates designing counters of any modulus with minimal external logic. The output is glitch−free due to the synchronous Reset.