

74F579 8-Bit Bidirectional Binary Counter with 3-STATE Outputs

General Description

The 74F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-STATE I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/\bar{D} input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Features

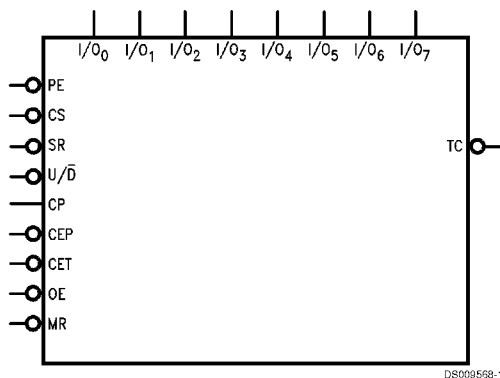
- Multiplexed 3-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typical
- Supply current 75 mA typical
- Guaranteed 4000V minimum ESD protection

Ordering Code:

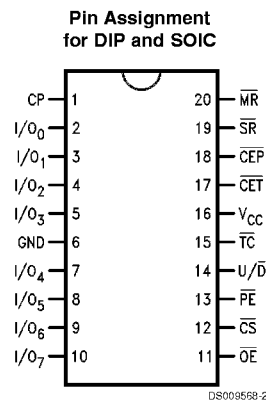
Commercial	Package Number	Package Description
74F579PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F579SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F579SJ (Note 1)	M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

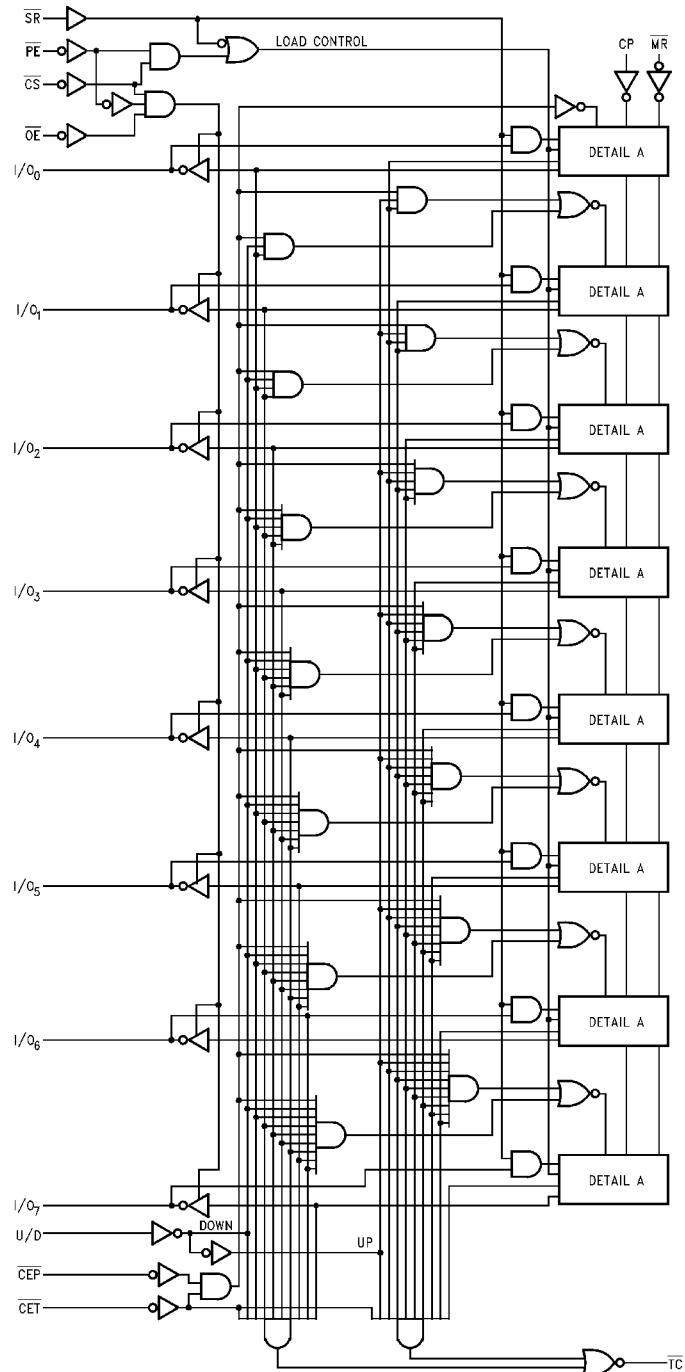
Logic Symbol



Connection Diagram

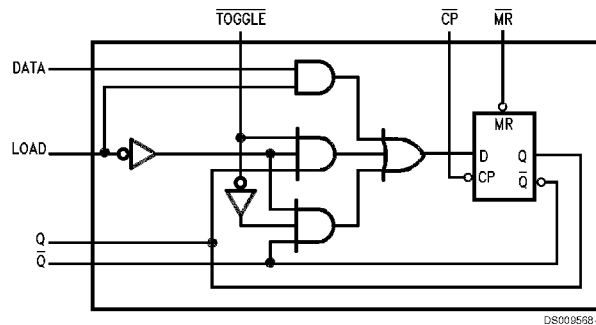


Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram (Continued)



V_{CC} = Pin 16
 GND = Pin 6
 () = Pin Numbers

Detail A

Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
I/O ₀ –I/O ₇	Data Inputs or 3-STATE Outputs	3.5/0.333 75/15	70 μA/–0.2 mA –3 mA/24 mA
\overline{PE}	Parallel Enable Input (Active LOW)	0.25/0.333	5 μA/–0.2 mA
U/ \overline{D}	Up-Down Count Control Input	0.25/0.333	5 μA/–0.2 mA
\overline{MR}	Master Reset Input (Active LOW)	0.25/0.333	5 μA/–0.2 mA
\overline{SR}	Synchronous Reset Input (Active LOW)	0.25/0.333	5 μA/–0.2 mA
\overline{CEP}	Count Enable Parallel Input (Active LOW)	0.25/0.333	5 μA/–0.2 mA
\overline{CET}	Count Enable Trickle Input (Active LOW)	0.25/0.333	5 μA/–0.2 mA
\overline{CS}	Chip Select Input Active (Active LOW)	0.25/0.333	5 μA/–0.2 mA
\overline{OE}	Output Enable Input (Active LOW)	0.25/0.333	5 μA/–0.2 mA
CP	Clock Pulse Input (Active Rising Edge)	0.25/0.333	5 μA/–0.2 mA
\overline{TC}	Terminal Count Output (Active LOW)	25/12.5	–1 mA/5 mA

Unit Loading/Fan Out (Continued)

Function Table

\overline{MR}	\overline{SR}	\overline{CS}	\overline{PE}	\overline{CEP}	\overline{CET}	U/\overline{D}	\overline{OE}	CP	Function
X	X	H	X	X	X	X	X	X	I/O _a to I/O _h in High Z (\overline{PE} Disabled)
X	X	L	H	X	X	X	H	X	I/O _a to I/O _h in High Z
X	X	L	H	X	X	X	L	X	Flip-Flop Outputs Appear on I/O Lines
L	X	X	X	X	X	X	X	X	Asynchronous Reset for all Flip-Flops
H	L	X	X	X	X	X	X	↘	Synchronous Reset for all Flip-Flops
H	H	L	L	X	X	X	X	↘	Parallel Load all Flip-Flops
H	H	(Not LL)		H	X	X	X	↘	Hold
H	H	(Not LL)		X	H	X	X	↘	Hold (\overline{TC} Held HIGH)
H	H	(Not LL)		L	L	H	X	↘	Count Up
H	H	(Not LL)		L	L	L	X	↘	Count Down

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↘ = LOW to HIGH Clock Transition

Not LL = \overline{CS} and \overline{PE} should never both be LOW voltage level at the same time.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max) twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min) 4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage	-1.2			V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.4		V	Min	I _{OH} = -3 mA
		74F 5% V _{CC}	2.7				
V _{OL}	Output LOW Voltage	74F 10% V _{CC}	0.5		V	Min	I _{OL} = 20 mA (\overline{TC}), I _{OL} = 24 mA (I/O _n)
		74F 5% V _{CC}	0.5				
I _{IH}	Input HIGH Current	74F	5.0		μA	Max	V _{IN} = 2.7V (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test	74F	7.0		μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	74F	0.5		mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current	74F	50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Control	3.75			μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
		500					
I _{ZZ}	Bus Drainage Test	500			μA	0.0	V _{OUT} = 5.25V
I _{IL}	Input LOW Current	-0.2			mA	Max	V _{IN} = 0.5V (Non-I/O Pins)
I _{IH} & I _{OZH}	Output Leakage Current	70			μA	Max	V _{OUT} = 2.7V (I/O _n)
I _{IL} & I _{OZL}	Output Leakage Current	-200			μA	Max	V _{OUT} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current	-60	-150		mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current	70	110		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current	85	120		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current	85	125		mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Comm}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	70	85		80		
t_{PLH}	Propagation Delay	3.0	5.0	7.5	3.0	8.0	ns
t_{PHL}	CP to I/O_n	5.0	8.0	11.5	5.0	11.5	
t_{PLH}	Propagation Delay	5.0	7.5	11.5	5.0	12.0	ns
t_{PHL}	CP to \overline{TC}	5.0	7.0	11.5	5.0	12.0	
t_{PLH}	Propagation Delay	4.5	7.0	9.0	4.5	10.0	ns
t_{PHL}	U/\overline{D} to \overline{TC}	4.5	8.0	9.5	4.5	10.0	
t_{PLH}	Propagation Delay	2.5	3.8	6.0	2.5	6.5	ns
t_{PHL}	\overline{CEP} or \overline{CET} to \overline{TC}	3.5	6.0	8.0	3.5	8.5	
t_{PHL}	Propagation Delay	5.0	7.5	10.0	5.0	10.0	ns
	\overline{MR} to I/O_n						
t_{PHL}	Propagation Delay	6.5	10.0	13.0	6.5	13.5	ns
	\overline{MR} to TC						
t_{PZH}	Output Enable Time	3.0	5.0	8.5	3.0	9.0	ns
t_{PZL}	\overline{CS} or \overline{PE} to I/O	5.5	8.0	10.5	5.5	11.5	
t_{PHZ}	Output Disable Time	2.0	5.0	8.5	2.0	9.0	ns
t_{PLZ}	\overline{CS} or \overline{PE} to I/O	2.0	4.5	8.0	2.0	8.5	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	3.0	8.5	ns
t_{PZL}	\overline{OE} to I/O_n	5.0	8.0	11.0	5.0	12.0	
t_{PHZ}	Output Disable Time	2.0	4.0	6.5	2.0	6.5	ns
t_{PLZ}	\overline{OE} to I/O_n	2.0	4.0	6.0	2.0	6.5	

AC Operating Requirements

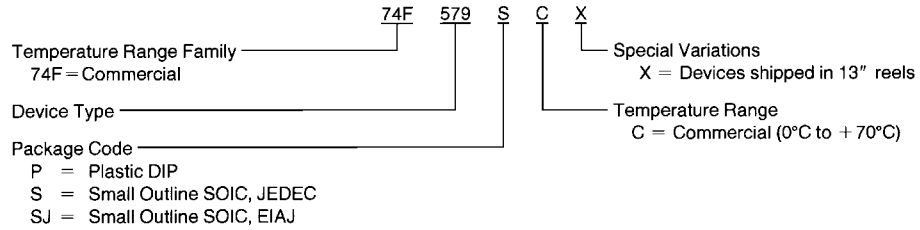
Symbol	Parameter	74F			74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$			$T_A, V_{CC} = \text{Comm}$		
		Min	Typ	Max	Min	Max	
$t_s(\text{H})$	Setup Time	4.0			4.0		ns
$t_s(\text{L})$	I/O_n to CP	4.0			4.0		
$t_h(\text{H})$	Hold Time	0.0			0.0		ns
$t_h(\text{L})$	I/O_n to CP	0.0			0.0		
$t_s(\text{H})$	Setup Time	9.5			9.5		ns
$t_s(\text{L})$	\overline{PE} , \overline{CS} or \overline{SR} to CP	9.5			9.5		
$t_h(\text{H})$	Hold Time	0.0			0.0		ns
$t_h(\text{L})$	\overline{PE} , \overline{CS} or \overline{SR} to CP	0.0			0.0		
$t_s(\text{H})$	Setup Time	6.5			6.5		ns
$t_s(\text{L})$	\overline{CET} or \overline{CEP} to CP	9.5			9.5		
$t_h(\text{H})$	Hold Time	0.0			0.0		ns
$t_h(\text{L})$	\overline{CET} or \overline{CEP} to CP	0.0			0.0		
$t_s(\text{H})$	Setup Time	9.0			9.5		ns
$t_s(\text{L})$	U/\overline{D} to CP	9.0			9.5		
$t_h(\text{H})$	Hold Time	0.0			0.0		ns
$t_h(\text{L})$	U/\overline{D} to CP	0.0			0.0		

AC Operating Requirements (Continued)

Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V			T _A , V _{CC} = Comm		
		Min	Typ	Max	Min	Max	
t _w (H)	Clock Pulse Width	4.5			4.5		ns
t _w (L)	High or Low	4.5			4.5		
t _w (L)	$\overline{\text{MR}}$ Pulse Width	3.0			3.0		ns
t _{rec}	Recovery Time $\overline{\text{MR}}$ to CP	4.0			4.0		ns

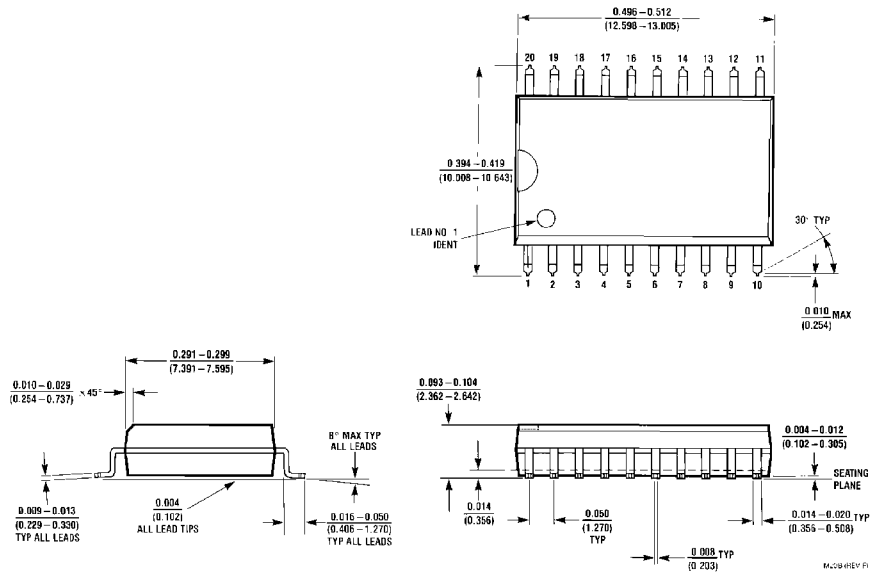
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



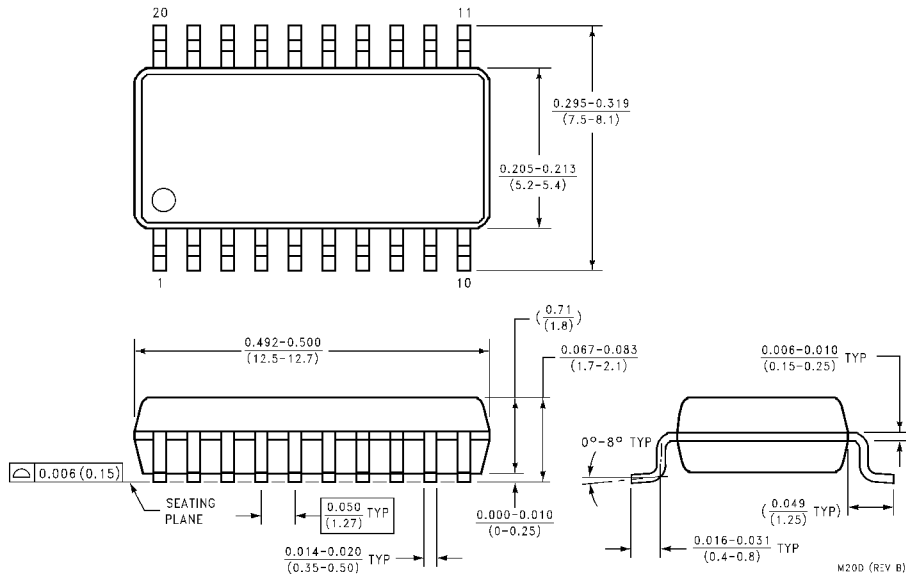
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Physical Dimensions inches (millimeters) unless otherwise noted

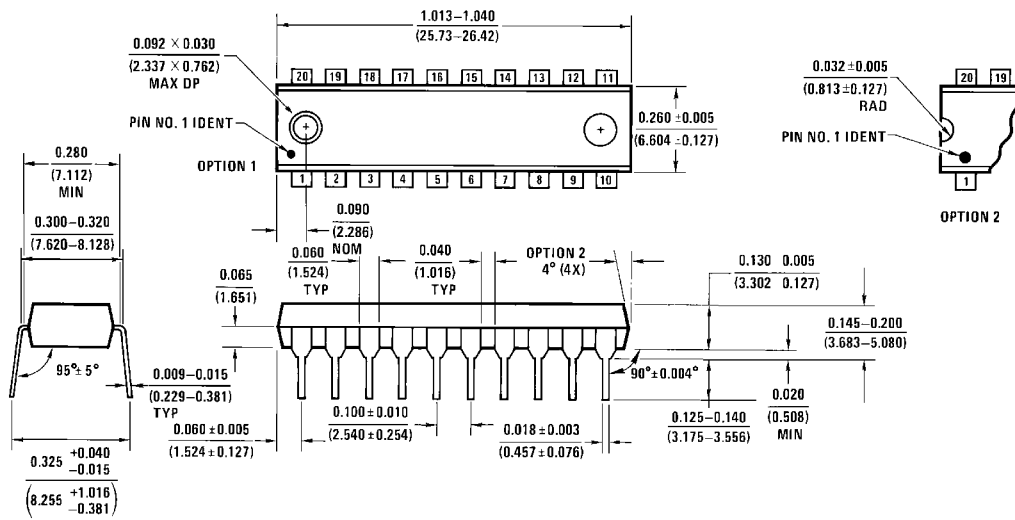


20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M20D**



**20-Lead (0.300" Wide) Molded Dual In-Line Package (P)
Package Number N20A**

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