

NC7SZ374

TinyLogic™ UHS D-Type Flip-Flop with 3-STATE Output

General Description

The NC7SZ374 is a single positive edge-triggered D-type CMOS Flip-Flop with 3-STATE output from Fairchild's Ultra High Speed Series of TinyLogic™ in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.8V–5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage. This single flip-flop will store the state of the D input that meets the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition.

The output tolerates voltages above V_{CC} in the 3-STATE condition.

Features

- Space saving SC70 6-lead package
- Ultra High Speed; t_{PD} 2.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive; ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V – 3V translation

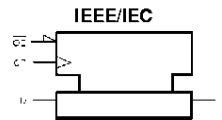
Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7SZ374P6	MAA06A	Z74	6-Lead SC70, EIAJ SC88, 1.25mm Wide	250 Units on Tape and Reel
NC7SZ374P6X	MAA06A	Z74	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel

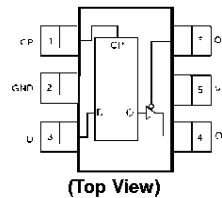
Pin Descriptions

Pin Names	Description
D	Data Input
CP	Clock Pulse Input
\overline{OE}	Output Enable Input
Q	Flip-Flop Output

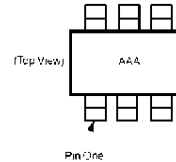
Logic Symbol



Connection Diagrams



Pin One Orientation Diagram



AAA represents Package Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top package mark left to right. Pin One is the lower left pin (see diagram)

Function Table

Inputs			Output
CP	D	\overline{OE}	Q
—	L	L	L
—	H	L	H
—	X	L	Q_n
X	X	H	Z

H = HIGH Logic Level Z = High Impedance X = Immaterial
L = LOW Logic Level Q_n = No change in data

TinyLogic™ is a trademark of Fairchild Semiconductor Corporation

NC7SZ374 TinyLogic™ UHS D-Type Flip-Flop with 3-STATE Output

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Supply Voltage (V_{CC})	0.5V to +7.0V	Power Supply	
DC Input Voltage (V_{IN})	-0.5V to +7.0V	Operating (V_{CC})	1.8V to 5.5V
DC Output Voltage (V_{OUT})	-0.5V to +7.0V	Data Retention	1.5V to 5.5V
DC Input Diode Current (I_{IK})		Input Voltage (V_{IN})	0V to 5.5V
$V_{IN} < 0V$	-50 mA	Output Voltage (V_{OUT})	
DC Output Diode Current (I_{OK})		Active State	0V to V_{CC}
$V_{OUT} < 0V$	-50 mA	3-STATE	0V to 5.5V
DC Output (I_{OUT}) Source/Sink Current	± 50 mA	Input Rise and Fall Time (t_r, t_f)	
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 50 mA	$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 to 20 ns/V
Storage Temperature Range (T_{STG})	-65°C to +150°C	$V_{CC} = 3.3V \pm 0.3V$	0 to 10 ns/V
Junction Temperature under Bias (T_J)	150°C	$V_{CC} = 5.5V \pm 0.5V$	0 to 5 ns/V
Junction Lead Temperature (T_L)		Operating Temperature (T_A)	-40°C to +85°C
(Soldering, 10 seconds)	260°C	Thermal Resistance (θ_{JA})	350° C/W
Power Dissipation (P_D) @ +85°C	180 mW		

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Control Input Voltage	1.8	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.75 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Control Input Voltage	1.8	0.25 V_{CC}			0.25 V_{CC}		V		
		2.3 to 5.5	0.3 V_{CC}			0.3 V_{CC}				
V_{OH}	HIGH Level Control Output Voltage	1.8	1.7	1.8		1.7	V	$V_{IN} = V_{IH}$	$I_{OH} = -100 \mu A$	
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		2.3	1.9	2.15		1.9			$I_{OH} = -8 \text{ mA}$ $I_{OH} = -16 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$	
		3.0	2.4	2.8		2.4				
		3.0	2.3	2.68		2.3				
		4.5	3.8	4.2		3.8				
V_{OL}	LOW Level Control Output Voltage	1.8		0.0	0.1		V	$V_{IN} = V_{IH}$	$I_{OL} = 100 \mu A$	
		2.3		0.0	0.1					$I_{OL} = 8 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 32 \text{ mA}$
		3.0		0.0	0.1					
		4.5		0.0	0.1					
		2.3		0.10	0.3					
		3.0		0.15	0.4					
		3.0		0.22	0.55					
		4.5		0.22	0.55					
I_{IN}	Input Leakage Current	0 to 5.5		± 0.1		± 1.0	μA	$0 \leq V_{IN} \leq 5.5V$		
I_{OZ}	3-STATE Output Leakage	1.8 to 5.5		± 0.5		± 5.0	μA	$V_{IN} = V_{IL}$ or V_{IH} $0 \leq V_{OUT} \leq 5.5V$		
I_{OFF}	Power Off Leakage Current	0.0		1.0		10	μA	V_{IN} or $V_{OUT} = 5.5V$		
I_{CC}	Quiescent Supply Current	1.8 to 5.5		1.0		10.0	μA	$V_{IN} = 5.5V, GND$		

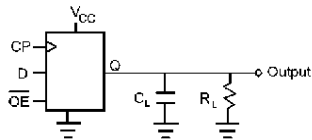
AC Electrical Characteristics										
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
f _{MAX}	Maximum Clock Frequency	1.8					100	MHz	C _L = 50 pF R _L = 500Ω, S ₁ = Open	Figure 1
		2.5 ± 0.2					125			Figure 3
		3.3 ± 0.3					150			
		5.0 ± 0.5					175			
t _{PLH} t _{PHL}	Propagation Delay CP to Q	1.8	2.5	6.5	10.0	2.5	11.0	ns	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	Figure 1
		2.5 ± 0.2	2.0	3.8	6.5	2.0	7.0			Figure 3
		3.3 ± 0.3	1.5	2.8	4.5	1.4	5.0			
		5.0 ± 0.5	1.0	2.2	3.5	1.0	3.8			
		3.3 ± 0.3	2.0	3.4	5.5	1.6	6.2			Figure 1
		5.0 ± 0.5	1.5	2.6	4.0	1.4	4.7			Figure 3
t _{PZL} t _{PZH}	Output Enable Time	1.8	2.0	6.0	9.0	2.0	9.5	ns	C _L = 50 pF, V _I = 2x V _{CC} R _U , R _D = 500 Ω S ₁ = GND for t _{PZH} S ₁ = V _I for t _{PZL}	Figure 1
		2.5 ± 0.2	2.0	3.7	6.0	1.8	6.6			Figure 4
		3.3 ± 0.3	1.5	2.8	5.0	1.4	5.3			
		5.0 ± 0.5	1.0	2.2	3.7	1.0	3.9			
t _{PLZ} t _{PHZ}	Output Disable Time	1.8	2.0	5.1	8.0	2.0	8.5	ns	C _L = 50 pF, V _I = 2x V _{CC} R _U , R _D = 500 Ω S ₁ = GND for t _{PHZ} S ₁ = V _I for t _{PLZ}	Figure 1
		2.5 ± 0.2	2.0	3.5	6.0	1.8	6.3			Figure 4
		3.3 ± 0.3	1.5	2.8	4.5	1.4	4.7			
		5.0 ± 0.5	1.0	2.3	3.7	1.0	3.9			
t _S	Setup Time, CP to D	2.5 ± 0.2					2.5	ns	C _L = 50 pF R _L = 500 Ω, S ₁ = Open	Figure 1
		3.3 ± 0.3					2.0			Figure 5
		5.0 ± 0.5					1.5			
t _H	Hold Time, CP to D	2.5 ± 0.2					1.5	ns	C _L = 50 pF R _L = 500 Ω, S ₁ = Open	Figure 1
		3.3 ± 0.3					1.5			Figure 5
		5.0 ± 0.5					1.5			
t _W	Pulse Width, CP	2.5 ± 0.2					3.0	ns	C _L = 50 pF R _L = 500 Ω, S ₁ = Open	Figure 1
		3.3 ± 0.3					2.8			Figure 5
		5.0 ± 0.5					2.5			

Capacitance (Note 2)					
Symbol	Parameter	Typ	Max	Units	Conditions
C _{IN}	Input Capacitance	3		pF	V _{CC} = Open, V _{IN} 0V or V _{CC}
C _{OUT}	Output Capacitance	4		pF	V _{CC} = 3.3V, V _{IN} = 0V or V _{CC}
C _{PD}	Power Dissipation Capacitance (Note 3)	10		pF	V _{CC} = 3.3V
		12		pF	V _{CC} = 5.0V

Note 2: T_A = +25°C f = 1MHz

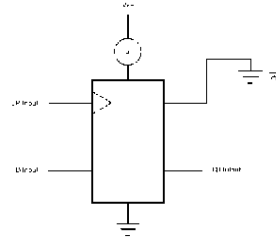
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2) C_{PD} is related to I_{CCD} dynamic operating current by the expression I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static)

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz, $t_w = 500$ ns

FIGURE 1. AC Test Circuit



CP Input = AC Waveform, $t_r = t_f = 1.8$ ns,
 CP Input PRR = 10 MHz, Duty Cycle = 50%
 D Input PRR = 5MHz, Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

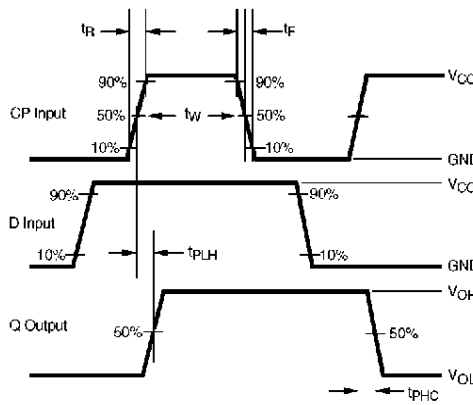


FIGURE 3. AC Waveforms

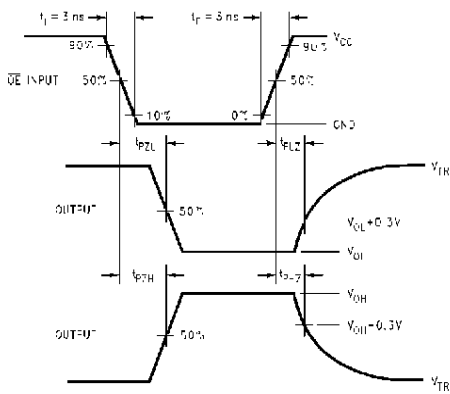


FIGURE 4. AC Waveforms

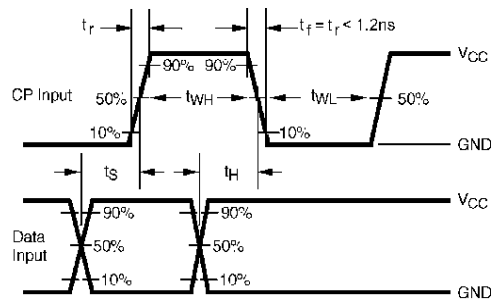


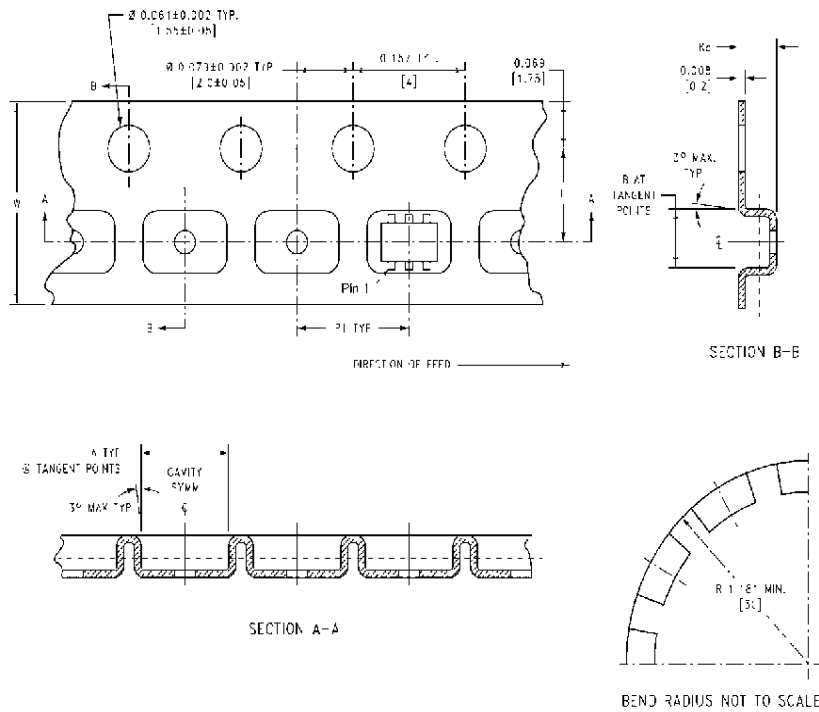
FIGURE 5. AC Waveforms

Tape and Reel Specification

TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

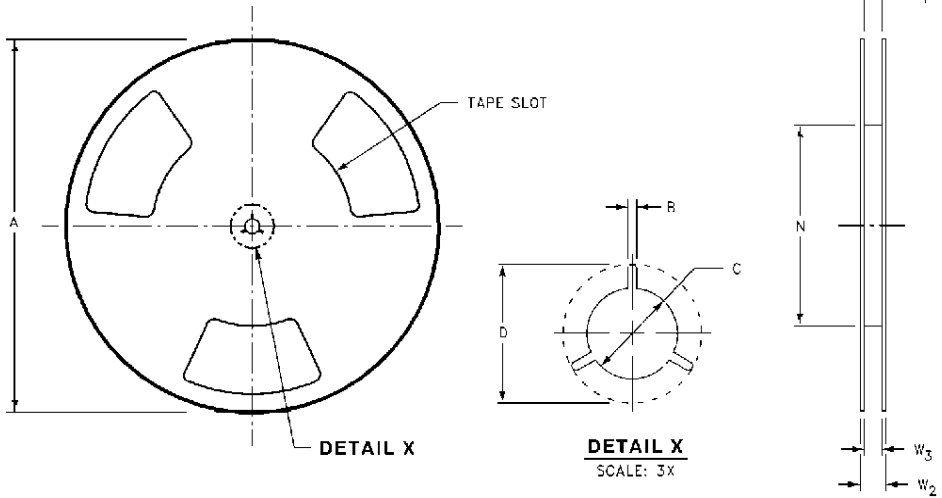
TAPE DIMENSIONS inches (millimeters)



Package	Tape Size	DIM A	DIM B	DIM F	DIM K ₀	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

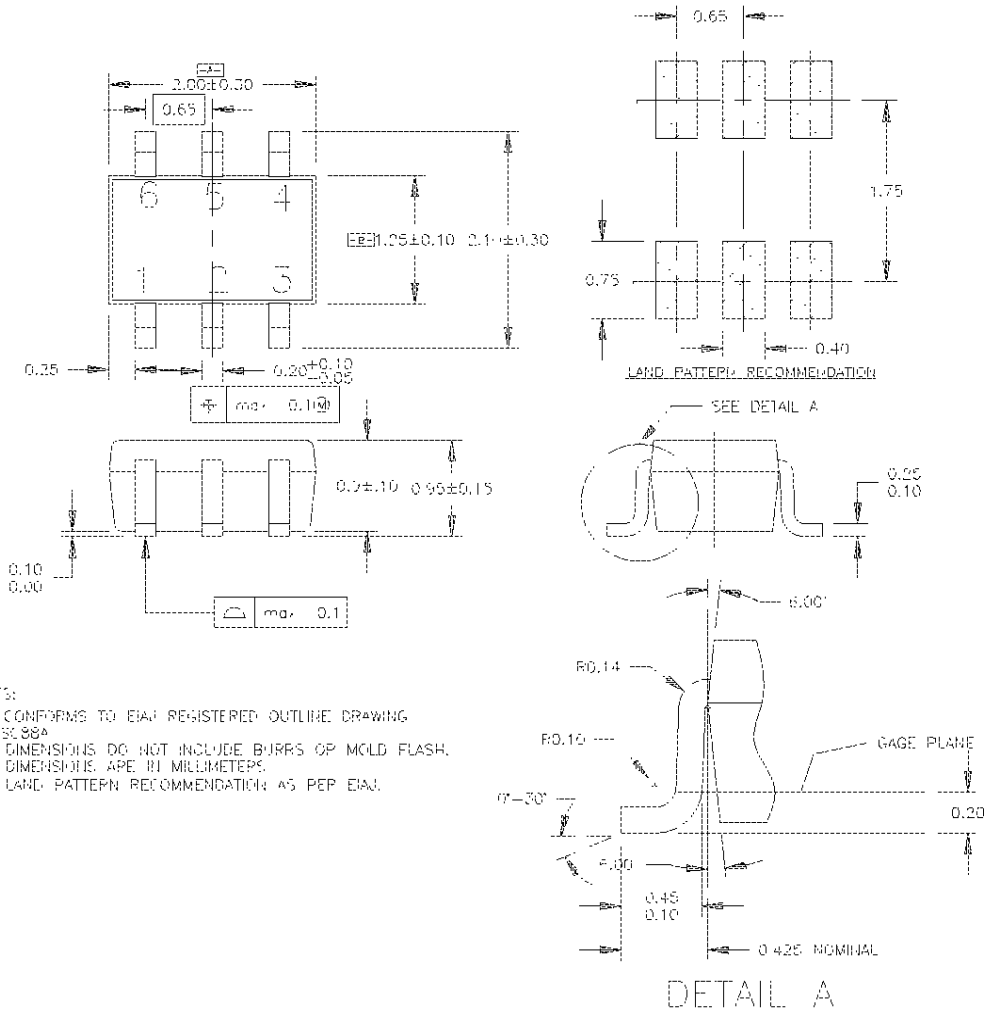
NC7SZ374

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	$0.331 + 0.059/-0.000$ ($8.40 + 1.50/-0.00$)	0.567 (14.40)	$W1 + 0.078/-0.039$ ($W1 + 2.00/-1.00$)

Physical Dimensions inches (millimeters) unless otherwise noted



- NOTES:
- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A
 - B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
 - C. DIMENSIONS ARE IN MILLIMETERS.
 - D. LAND PATTERN RECOMMENDATION AS PER EIAJ.

**6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com