Rochester Electronics®

Datasheet

DM74LS174

Hex/Quad D-Type Flip-Flops with Clear

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time require-ments is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

FAIRCHILD SEMICONDUCTOR™

August 1992
Revised April 2000

DM74LS174 • DM74LS175
Hex/Quad D-Type Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

Features

- DM74LS174 contains six flip-flops with single-rail outputs
- DM74LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW

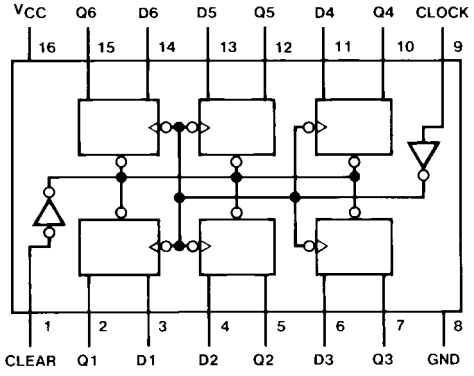
Ordering Code:

Order Number	Package Number	Package Description
DM74LS174M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS175M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS175N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

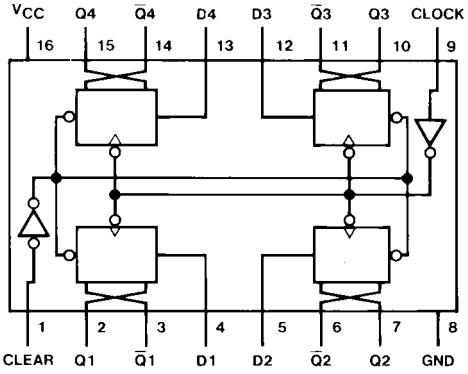
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

DM74LS174



DM74LS175



Function Table

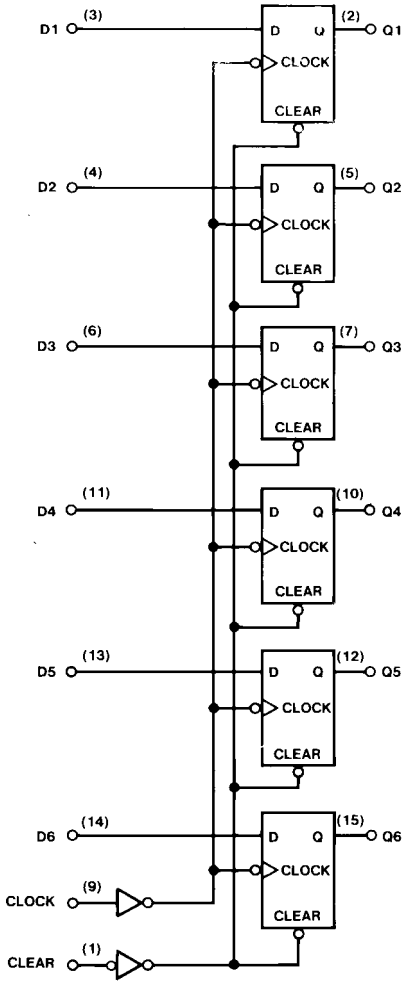
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

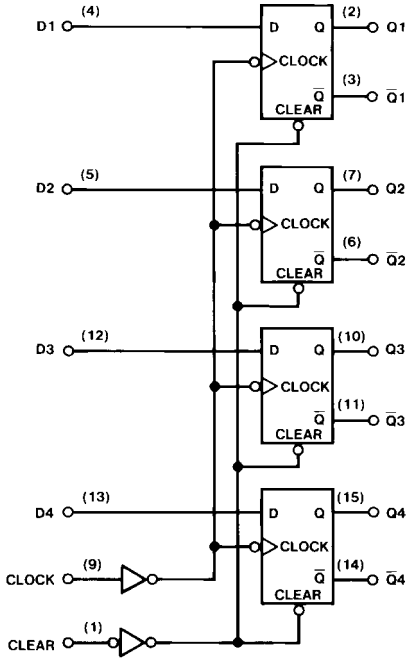
H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care
↑ = Transition from LOW-to-HIGH level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = DM74LS175 only

Logic Diagrams

DM74LS174



DM74LS175



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS174 Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	MHz
t_W	Pulse Width	Clock	20			ns
	(Note 4)	Clear	20			
t_{SU}	Data Setup Time (Note 4)		20			ns
t_H	Data Hold Time (Note 4)		0			ns
t_{REL}	Clear Release Time (Note 4)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

DM74LS174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			16	26	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs OPEN and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

DM74LS174 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Output		30		32	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Output		30		36	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Output		35		42	ns

DM74LS175 Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				–0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 8)		0		30	MHz
f_{CLK}	Clock Frequency (Note 9)		0		25	MHz
t_W	Pulse Width	Clock	20			ns
	(Note 10)	Clear	20			
t_{SU}	Data Setup Time (Note 10)		20			ns
t_H	Data Hold Time (Note 10)		0			ns
t_{REL}	Clear Release Time (Note 10)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 10: T_A = 25°C and V_{CC} = 5V.

DM74LS175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 11)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA				–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	Clock			–0.4	mA
			Clear			–0.4	
			Data			–0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 12)		–20		–100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 13)			11	18	mA

Note 11: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 12: Not more than one output should be shorted at a time, and the duration should not exceed one second.

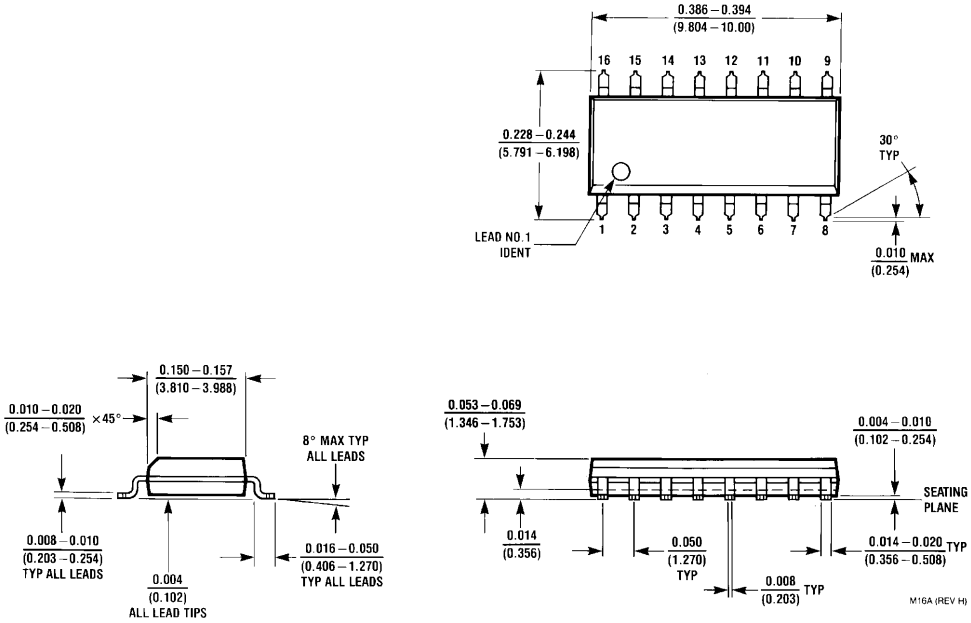
Note 13: With all outputs OPEN and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock input.

DM74LS175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

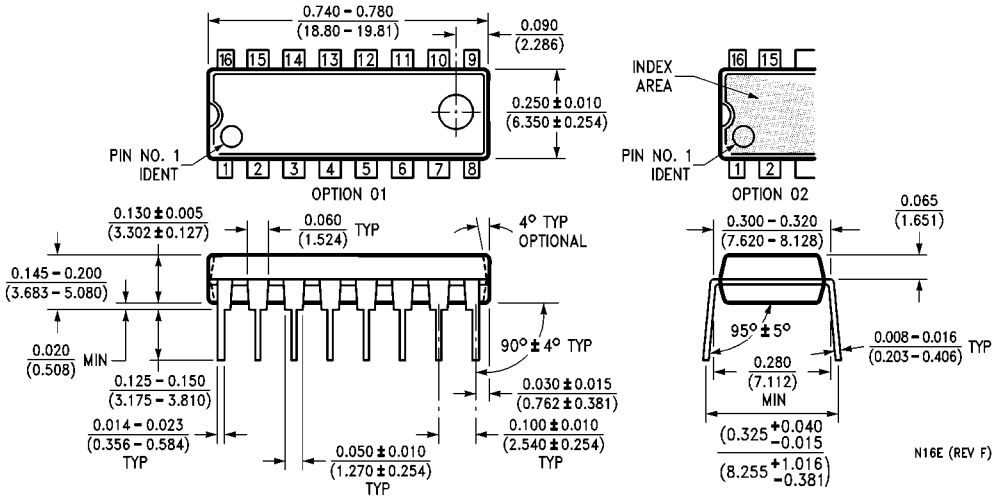
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		30		32	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		30		36	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25		29	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		35		42	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

[Information as of 1-Aug-2000]

DM74LS174

Hex D Flip-Flop with Clear

Generic P/N 74LS174

Contents

General Description
Features
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Availability, Models, Samples & Pricing

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- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:

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  Shift registers

Pattern generators

- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW

Datasheet

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DM74LS174/DM74LS175 D Flip-Flop with Clear (73 Kbytes; 29-JUL-00)

Availability, Models, Samples & Pricing

Part Number	Grade	Package		Status	Models		Budgetary Pricing		Std Pack Size	Packag Marki
		Type	# pins		SPICE	IBIS	Quantity	$US ea		
DM74LS174M	Comm	SOIC	16	Full Production	N/A	N/A	1-24 25-99 100-1000	$0.5560 $0.4170 $0.3330	N/A	$Y&Z DM74
DM74LS174MX	Comm	SOIC	16	Full Production	N/A	N/A	1-24 25-99 100-1000	$0.8890 $0.6670 $0.5330	N/A	$Y&Z DM74
DM74LS174SJ	Comm	SOIC	16	Full Production	N/A	N/A		N/A	N/A	$Y&Z LS1
DM74LS174SJX	Comm	SOIC	16	Full Production	N/A	N/A		N/A	N/A	$Y&Z LS1
DM74LS174N	Comm	MDIP	16	Full Production	N/A	N/A	1-24 25-99 100-1000	$0.4670 $0.35 $0.28	N/A	$Y&Z& DM74
DM74LS174CW	Comm	wafer		Preliminary	N/A	N/A		N/A	N/A	