

March 1992 Revised February 2004

74FR74 **Dual D-Type Flip-Flop**

General Description

The 74FR74 is a dual D-type flip-flops with true and complement (Q/\overline{Q}) outputs. On the 74FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CPn). Both parts feature asynchronous clear $(C_{\mbox{\scriptsize Dn}})$ and set $(S_{\mbox{\scriptsize Dn}})$ inputs which are low level enabled.

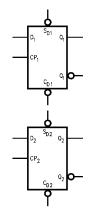
Features

- 74FR74 is pin-for-pin compatible with the 74F74
- True 150 MHz f_{MAX} capability on 74FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

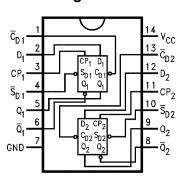
Ordering Code:

Order Number	Package Number Package Description				
74FR74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow			
74FR74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

Logic Symbols



Connection Diagram



Pin Descriptions

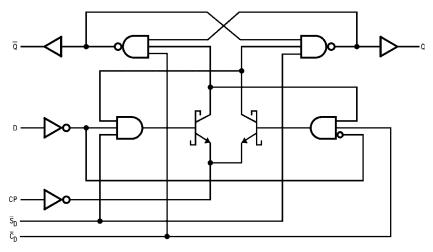
Pin Names	Description
D _n	Data Inputs
CP _n	Clock Inputs
S _{Dn}	Asynchronous Set Inputs
C _{Dn}	Asynchronous Clear Inputs
Q _n	True Output
\overline{Q}_n	Complementary Output

Truth Table

	Inp	Outputs			
SD	CD	CP	D	Q	Ø
L	Н	Х	Х	Н	L
Н	L	Χ	Χ	L	Н
L	L	X	Χ	Н	Н
Н	Н	~	Н	Н	L
Н	Н	~	L	L	Н
Н	Н	L	X	Q_0	\overline{Q}_0

- H = HIGH Voltage Level
- L = LOW Voltage Level
- Z = High Impedance X = Immaterial
- \nearrow = Rising Edge Q₀ = Previous Q(\overline{Q}) before LOW-to-HIGH Clock Transition

Logic Diagram



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$

 $\begin{array}{lll} \mbox{Junction Temperature under Bias} & -55^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{V}_{\mbox{CC}} \mbox{ Pin Potential to Ground Pin} & -0.5\mbox{V to } +7.0\mbox{V} \end{array}$

Input Voltage (Note 2) -0.5V to +7.0V Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC}

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 2000V

Recommended Operating Conditions

Free Air Ambient Temperature 0° C to $+70^{\circ}$ C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Тур	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	2.5			V	Min	I _{OH} = -1 mA
	Voltage	2.4			V	Min	$I_{OH} = -3 \text{ mA}$
		2.0			V	Min	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage			0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5	μΑ	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7	μА	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-150	μА	Max	$V_{IN} = 0.5V (D_n, CP_n)$
				-1.8	mA	Max	$V_{IN} = 0.5V (C_{Dn}, S_{Dn})$
V _{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9 \mu A,$ All Other Pins Grounded
I _{OD}	Output Circuit			3.75	V	0.0	$V_{IOD} = 150 \text{ mV},$
	Leakage Test						All Other Pins Grounded
os	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
CEX	Output HIGH Leakage Current			50	μА	Max	V _{OUT} = V _{CC}
I _{CC}	Power Supply Current			24	mA	Max	

AC Electrical Characteristics

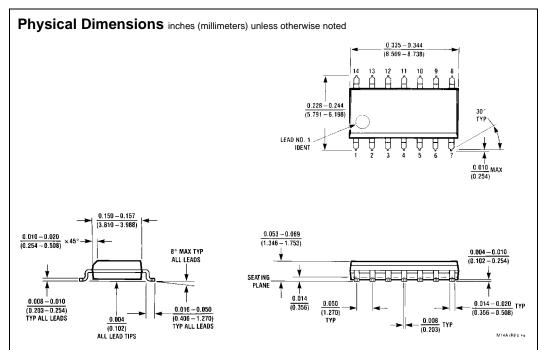
Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_1 = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0$ V $C_1 = 50 \text{ pF}$		Units
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	150	190		150		MHz
t _{PLH}	Propagation Delay	2.5	3.5	5.0	2.5	5.0	
t _{PHL}	CP_n to Q_n or \overline{Q}_n	2.5	4.5	6.0	2.5	6.0	ns
t _{PLH}	Propagation Delay	1.5	3.5	5.5	1.5	5.5	ns
t _{PHL}	\overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n	2.0	5.5	7.0	2.0	7.0	
toshl	Pin to Pin Skew					1.0	ns
(Note 3)	for HL Transitions					1.0	115
t _{OSLH}	Pin to Pin Skew					1.0	ns
(Note 3)	for LH Transitions					1.0	115
tost	Pin to Pin Skew					3.0	ns
(Note 3)	for HL/LH Transitions					3.0	115
t _{Q/Q}	True/Complement						
(Note 3)	Output Skew					1.8	ns
t _{PS}	Pin (Signal)					4.0	
(Note 3)	Transition Variation					1.8	ns

Note 3: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements

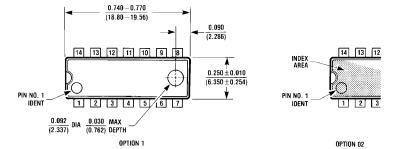
		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units	
Symbol	Parameter						
Syllibol	Farameter	$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$			
		Min	Max	Min	Max		
t _S (H)	Setup Time, HIGH or LOW	2.5		2.5		ns	
t _S (L)	D _n to CP _n	2.5		2.5		115	
t _H (H)	Hold Time, HIGH or LOW	0		0		no	
t _H (L)	D _n to CP _n	0		0		ns	
t _W (H)	CP _n Pulse Width	3.3		3.3		no	
t _W (L)	HIGH or LOW	3.3		3.3		ns	
(Note 4)							
t _W (L)	\overline{S}_{Dn} or \overline{C}_{Dn} Pulse Width	4.0		4.0		ns	
t _{REC}	Recovery Time	2.0		2.0		ns	
	\overline{S}_{Dn} or \overline{C}_{Dn} to CP_n						

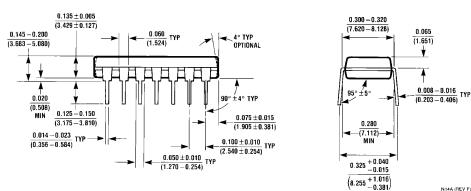
Note 4: This specification is guaranteed by design.



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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