MC100LVEL40

3.3/5V ECL Differential Phase-Frequency Detector

The MC100LVEL40 is a three state phase frequency–detector intended for phase–locked loop applications which require a minimum amount of phase and frequency difference at lock. Advanced design significantly reduces the dead zone of the detector. For proper operation, the input edge rate of the R and V inputs should be less than 5 ns. The device is designed to work with a 3.3 V power supply.

When the reference (R) and the feedback (FB) inputs are unequal in frequency and/or phase the differential up (U) and down (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

For application information, refer to AND8040/D, "Phase Lock Loop Operation."

The 100 Series Contains Temperature Compensation

- 250 MHz Typical Bandwidth
- ESD Protection: >2 kV HBM
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V
  with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V
  with V_{EE} = −3.0 V to −5.5 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, refer to Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in,
  Oxygen Index: 28 to 34
- Transistor Count = 356 devices

MARKING DIAGRAM


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100LVEL40
AWLYYWW
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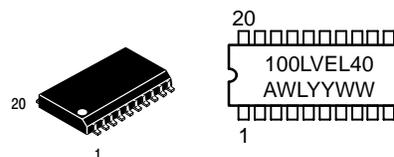
SO−20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL40DW	SO−20	38 Units/Rail
MC100LVEL40DWR2	SO−20	1000 Tape &Reel

MC100LVEL40

NC V$_{CCO}$ U $\overline{U}$ V$_{EE}$ D $\overline{D}$ V$_{CCO}$ NC NC

| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

NC NC R $\overline{R}$ V$_{BB}$ FB $\overline{FB}$ V$_{CC}$ NC NC

Figure 1. 20–Lead Pinout (Top View)
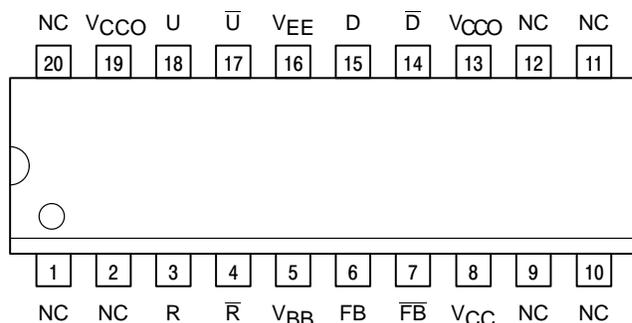
PIN DESCRIPTION

PIN	FUNCTION
U, $\overline{U}$	ECL Up Differential Outputs
D, $\overline{D}$	ECL Down Differential Outputs
FB, $\overline{FB}$	ECL Feedback Differential Inputs
R, $\overline{R}$	ECL Reference Differential Inputs
V$_{BB}$	Reference Voltage Output
V$_{CC}$, V$_{CCO}$	Positive Supply
V$_{EE}$	Negative Supply
NC	No Connect

Warning: All V$_{CC}$, V$_{CCO}$, and V$_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.
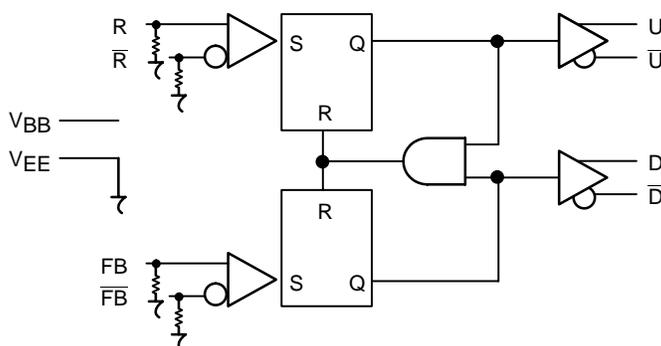
Figure 2. Logic Diagram

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V$_{CC}$	PECL Mode Power Supply	V$_{EE}$ = 0 V		8 to 0	V
V$_{EE}$	NECL Mode Power Supply	V$_{CC}$ = 0 V		−8 to 0	V
V$_I$	PECL Mode Input Voltage NECL Mode Input Voltage	V$_{EE}$ = 0 V V$_{CC}$ = 0 V	V$_I \leq$ V$_{CC}$ V$_I \geq$ V$_{EE}$	6 to 0 −6 to 0	V
I$_{out}$	Output Current	Continuous Surge		50 100	mA mA
I$_{BB}$	V$_{BB}$ Sink/Source			± 0.5	mA
TA	Operating Temperature Range			−40 to +85	°C
T$_{stg}$	Storage Temperature Range			−65 to +150	°C
q$_{JA}$	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ$_{JC}$	Thermal Resistance (Junction–to–Case)	std bd	20 SOIC	30 to 35	°C/W
T$_{sol}$	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

MC100LVEL40

LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0 V (Note 1)

Symbol	Characteristic	−40°C Min	Typ	Max	25°C Min	Typ	Max	85°C Min	Typ	Max	Unit
I_{EE}	Power Supply Current		38	45		38	47		38	47	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1380	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7) Vpp < 500 mV Vpp ≧ 500 mV	1.3 1.5		3.3 3.3	1.2 1.4		3.3 3.3	1.2 1.4		3.3 3.3	V V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current Others $\overline{R}$, $\overline{FB}$	0.5 −300			0.5 −300			0.5 −300			µA µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between Vppmin and 1 V.

LVNECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 5)

Symbol	Characteristic	−40°C Min	Typ	Max	25°C Min	Typ	Max	85°C Min	Typ	Max	Unit
I_{EE}	Power Supply Current		38	45		38	47		38	47	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 6)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7) Vpp < 500 mV Vpp ≧ 500 mV	−2.0 −1.8		−0.4 −0.4	−2.1 −1.9		−0.4 −0.4	−2.1 −1.9		−0.4 −0.4	V V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current Others $\overline{R}$, $\overline{FB}$	0.5 −300			0.5 −300			0.5 −300			µA µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
6. All loading with 50 Ω resistor to V_{CC} − 2 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between Vppmin and 1 V.

**AC CHARACTERISTICS** V_{CC}= 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0 V; V_{EE} = −3.3 V (Note 8)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fmax	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay R to U, FB to D	430 1200		630 1400	450 1250		650 1450	480 1370		680 1590	ps
V_{PP}	Input Swing (Differential) (Note 9)	150		1000	150		1000	150		1000	mV
tJITTER	Cycle−to−Cycle Jitter		TBD			TBD			TBD		ps
t_r, t_f	Output Rise/Fall Times	175		475	175		475	175		475	ps

8. V_{EE} can vary ±0.3 V.
9. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

$$V_{TT} = V_{CC} - 2.0 \text{ V}$$
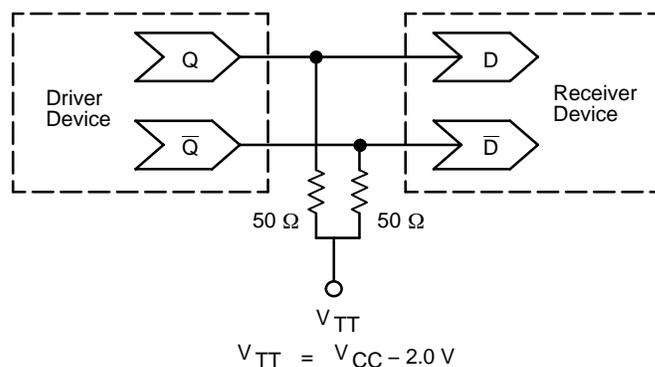
**Figure 3. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020 – Termination of ECL Logic Devices)**

Resource Reference of Application Notes

AN1404   –   ECLinPS Circuit Performance at Non−Standard V_{IH} Levels

AN1405   –   ECL Clock Distribution Techniques

AN1406   –   Designing With PECL (ECL at +5.0 V)

AN1503   –   ECLinPS I/O SPICE Modeling Kit

AN1504   –   Metastability and the ECLinPS Family

AN1560   –   Low Voltage ECLinPS SPICE Modeling Kit

AN1568   –   Interfacing Between LVDS and ECL

AN1596   –   ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650   –   Using Wire−OR Ties in ECLinPS Designs

AN1672   –   The ECL Translator Guide

AND8001   –   Odd Number Counters Design

AND8002   –   Marking and Date Codes

AND8020   –   Termination of ECL Logic Devices