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GTL6C816A LVTTTL-to-GTLP Clock Driver (Preliminary)

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General Description

The GTL6C816A is a clock driver that provides LVTTTL to GTLP signal level translation (and vice versa). The device provides a high speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTL(P) logic levels. High speed backplane operation is a direct result of GTL(P)'s reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTL(P) has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

Features

- Interface between LVTTTL and GTLP logic levels
- Edge Rate Control to minimize noise on the GTLP port
- Power up/down high impedance for live insertion
- 1:6 fanout clock driver for LVTTTL port
- 1:2 fanout clock driver for GTLP port
- LVTTTL compatible driver and control inputs
- Flow through pinout optimizes PCB layout
- Open drain on GTLP to support wired-or connection
- A-Port source/sink -24/+24 mA
- B-Port sink 50 mA
- -40°C to +85°C temperature capability
- Low voltage version of GTL6C816

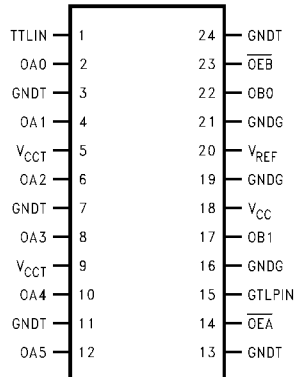
Ordering Code:

Order Number	Package Number	Package Description
GTL6C816AMTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Pin Descriptions

Pin Names	Description
TTLIN, GTLPIN	Clock Inputs (LVTTTL and GTLP respectively)
$\overline{OE}B$	Output Enable (Active LOW) GTLP Port (LVTTTL Levels)
$\overline{OE}A$	Output Enable (Active LOW) TTL Port (LVTTTL Levels)
V_{CC} -GNDT	TTL Output Supplies
V_{CC}	Internal Circuitry V_{CC}
GNDG	OBn GTLP Output Grounds
V_{REF}	Voltage Reference Input
OA0-OA5	TTL Buffered Clock Outputs
OB0-OB1	GTLP Buffered Clock Outputs

Connection Diagram



Functional Description

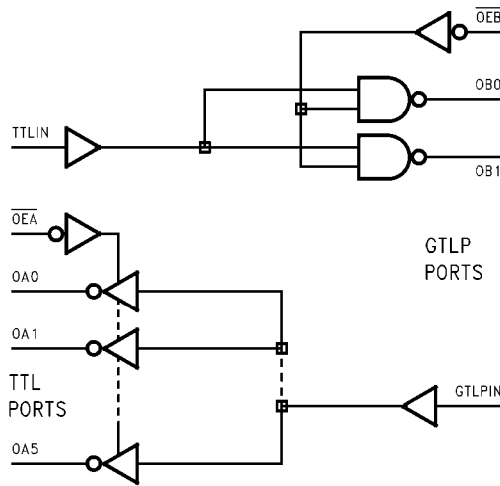
The GTLP6C816A is a clock driver providing LVTTTL-to-GTLP clock translation, and GTLP-to-LVTTTL clock translation in the same package. The LVTTTL-to-GTLP direction is a 1:2 clock driver path with a single Enable pin (\overline{OEB}). For the GTLP-to-LVTTTL direction the clock receiver path is a 1:6 buffer with a single Enable control (\overline{OEA}). Data polarity is inverting for both directions.

Truth Tables

Inputs		Outputs
TTLIN	\overline{OEB}	OBn
H	L	L
L	L	H
X	H	High Z

Inputs		Outputs
GTLPIN	\overline{OEA}	OAn
H	L	L
L	L	H
X	H	High Z

Logic Diagram



Absolute Maximum Ratings <small>(Note 1)</small>		Recommended Operating Conditions <small>(Note 3)</small>	
Supply Voltage (V_{CC})	-0.5V to +4.6V	Supply Voltage V_{CC}	3.15V to 3.45V
DC Input Voltage (V_I)	-0.5V to +4.6V	Bus Termination Voltage (V_{TT})	
DC Output Voltage (V_O)		GTLP	1.47V to 1.53V
Outputs 3-STATE	-0.5V to +4.6V	GTL	1.14V to 1.26V
Outputs Active (Note 2)	-0.5V to +4.6V	V_{REF}	0.98V to 1.02V
DC Output Sink Current into OA-Port I_{OL}	48 mA	Input Voltage (V_I) on INA-Port and Control Pins	0.0V to 3.45V
DC Output Source Current from OA-Port I_{OH}	-48 mA	HIGH Level Output Current (I_{OH})	
DC Output Sink Current into OB-Port in the LOW State I_{OL}	100 mA	OA-Port	-24 mA
DC Input Diode Current (I_{IK})		LOW Level Output Current (I_{OL})	
$V_I < 0V$	-50 mA	OA-Port	+24 mA
DC Output Diode Current (I_{OK})		OB-Port	+50 mA
$V_O < 0V$	-50 mA	Operating Temperature (T_A)	-40°C to +85°C
$V_O > V_{CC}$	+50 mA	Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.	
ESD Rating	> 2000V	Note 2: I_O Absolute Maximum Rating must be observed.	
Storage Temperature (T_{STG})	-65°C to +150°C	Note 3: Unused inputs must be held High or Low.	

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, $V_{REF} = 1.0V$ (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 4)	Max	Units
V_{IH}	GTLPIN			$V_{REF} + 0.05$		V_{TT}	V
	Others			2.0			V
V_{IL}	GTLPIN			0.0		$V_{REF} - 0.05$	V
	Others					0.8	V
V_{REF} (Note 5)	GTLP				1.0		V
V_{TT} (Note 5)	GTLP				1.5		V
V_{IK}		$V_{CC} = 3.15V$	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	OAn-Port	$V_{CC} = 3.15V$	$I_{OH} = -100\ \mu A$	$V_{CC} - 0.2$			V
			$I_{OH} = -18\text{ mA}$	2.4			
			$I_{OH} = -24\text{ mA}$	2.2			
V_{OL}	OAn-Port	$V_{CC} = 3.15V$	$I_{OL} = 100\ \mu A$			0.2	V
			$I_{OL} = 18\text{ mA}$			0.4	
			$I_{OL} = 24\text{ mA}$			0.5	
V_{OL}	OBn-Port	$V_{CC} = 3.15V$	$I_{OL} = 100\ \mu A$			0.2	V
			$I_{OL} = 40\text{ mA}$			0.4	
			$I_{OL} = 50\text{ mA}$			0.55	
I_I	TTLIN/ Control Pins	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0V$			10 -10	μA
	GTLPIN	$V_{CC} = 3.45V$	$V_I = V_{TT}$ $V_I = 0$			10 -10	μA
I_{OFF}	TTLIN	$V_{CC} = 0$	V_I or $V_O = 0V$ to 5.25V			100	μA
	GTLPIN	$V_{CC} = 0$	V_I or $V_O = 0V$ to V_{TT}			100	μA
I_{OZH}	OAn-Port	$V_{CC} = 3.45V$	$V_O = 3.45V$			5	μA
	OBn-Port		$V_O = 1.5V$			5	
I_{OZL}	OAn-Port	$V_{CC} = 3.45V$	$V_O = 0$			-5	μA
I_{CC}	OAn or OBn Ports	$V_{CC} = 3.45V$	Outputs HIGH		5.5	10	mA
			Outputs LOW		5	10	
			Outputs Disabled		5.5	10	

DC Electrical Characteristics (Continued)						
Symbol	Test Conditions		Min	Typ (Note 4)	Max	Units
ΔI_{CC}	TTLIN	$V_{CC} = 3.45V$	$V_I = V_{CC} - 0.6$		1	mA
C_I	Control Pins/ GTLPIN/TTLIN		$V_I = V_{CC}$ or 0	4.5		pF
C_O	OAn-Port		$V_I = V_{CC}$ or 0	6.0		
	OBn-Port		$V_I = V_{CC}$ or 0	8.0		

Note 4: All typical values are at $V_{CC} = 3.3V$ and $T_A = 25^\circ C$.

Note 5: GTLP V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and R_{TERM} can be adjusted to accommodate backplane impedances other than 50Ω , within the boundaries of not exceeding the DC Absolute I_{OL} ratings. Similarly V_{REF} can be adjusted to compensate for changes in V_{TT} .

AC Electrical Characteristics

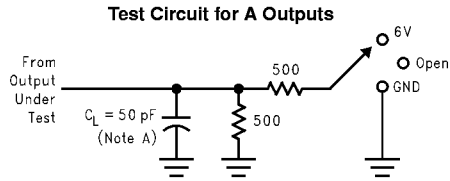
Over recommended range of supply voltage and operating free air temperature. $V_{REF} = 1.0V$ (unless otherwise noted).
 $C_L = 30$ pF for OBn-Port and $C_L = 50$ pF for OAn-Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 6)	Max	Units
f_{TOGGLE}	TTLIN	OBn	175			MHz
	GTLPIN	OAn	175			
t_{PLH}	TTLIN	OBn	1.5	2.6	5.2	ns
t_{PHL}			0.9	1.9	3.9	
t_{PLH}	\overline{OEB}	OBn	1.8	2.6	5.2	ns
t_{PHL}			1.2	2.2	4.1	
t_{RISE}	Transition Time, OB Outputs (20% to 80%)			1.3		ns
t_{FALL}	Transition Time, OB outputs (20% to 80%)			1.5		
t_{RISE}	Transition Time, OA outputs (10% to 90%)			1.7		ns
t_{FALL}	Transition Time, OA outputs (10% to 90%)			1.6		
t_{PZH}, t_{PZL}	\overline{OEA}	OAn	0.5	3.1	4.8	ns
t_{PLZ}, t_{PHZ}			0.0	2.4	4.4	
t_{PLH}	GTLPIN	OAn	2.7	3.9	6.5	ns
t_{PHL}			2.4	3.5	5.3	
t_{OSHL}, t_{OSLH} (Note 7)	Common Edge Skew (OA Drivers)			0.1	0.75	ns
t_{OSHL}, t_{OSLH} (Note 7)	Common Edge Skew (OB Drivers)			0.15	0.75	ns

Note 6: All typical values are at $V_{CC} = 3.3V$ and $T_A = 25^\circ C$.

Note 7: Output to Output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). This parameter guaranteed by design and statistical process distribution. Actual skew values between the GTLP (OBn) outputs could vary on the backplane due to the loading and impedance seen by the device.

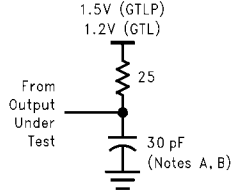
Test Circuit and Timing Waveforms



Test	S
t_{plh}/t_{phl}	Open
t_{plz}/t_{pzl}	6V
t_{phz}/t_{pzh}	GND

Note A: C_L includes probes and jig capacitance.

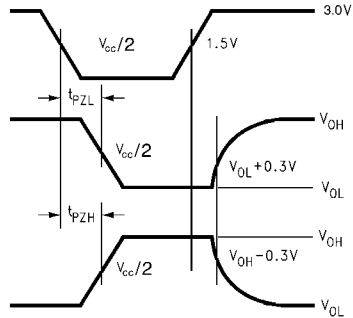
Test Circuit for B Outputs



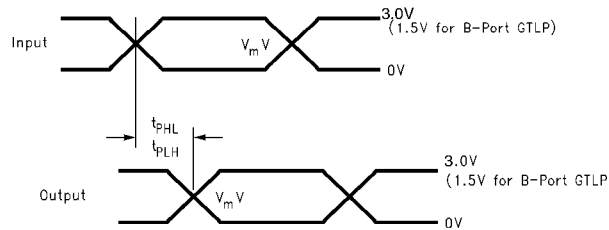
Note A: C_L includes probes and jig capacitance.

Note B: For B-Port $C_L = 30 \text{ pF}$ is used for worst case.

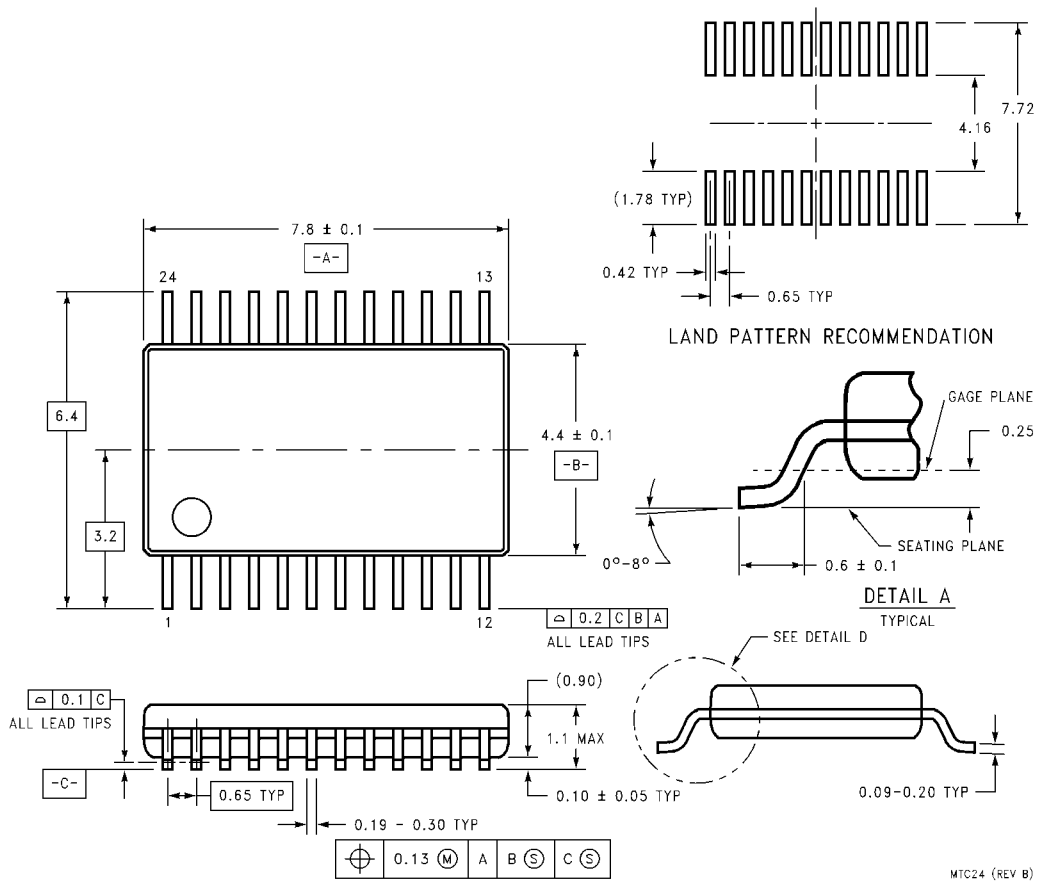
Voltage Waveforms Enable and Disable Times A-Port



Voltage Waveforms Propagation Delay ($V_m = V_{CC}/2$ for A-Port and 1.0 for B-Port)



Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24**

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