

8-Bit Static Shift Register

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------------------------------|--|--------------------------------|------|
| V _{DD} | DC Supply Voltage | - 0.5 to + 18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | - 0.5 to V _{DD} + 0.5 | V |
| I _{in} , I _{out} | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| P _D | Power Dissipation, per Package† | 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature (8-Second Soldering) | 260 | °C |

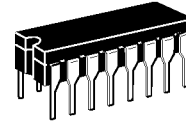
* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

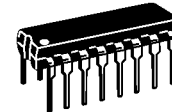
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

MC14014B MC14021B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = - 55° to 125°C for all packages.

TRUTH TABLE

SERIAL OPERATION:

| t | Clock | D _S | P/S | Q6 t=n+6 | Q7 t=n+7 | Q8 t=n+8 |
|-----|-------|----------------|-----|-------------|-------------|-------------|
| n | ↗ | 0 | 0 | 0 | ? | ? |
| n+1 | ↗ | 1 | 0 | 1 | 0 | ? |
| n+2 | ↗ | 0 | 0 | 0 | 1 | 0 |
| n+3 | ↗ | 1 | 0 | 1 | 0 | 1 |
| | ↘ | X | 0 | Q6 | Q7 | Q8 |

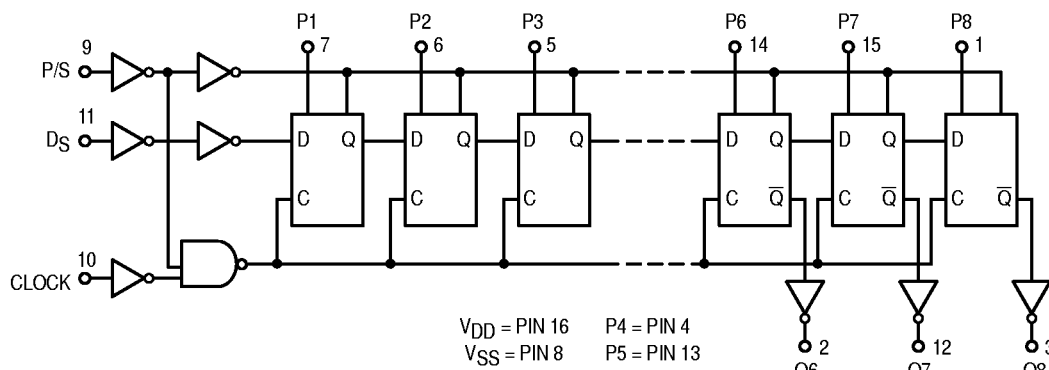
PARALLEL OPERATION:

| Clock | | D _S | P/S | P _n | *Q _n |
|----------|----------|----------------|-----|----------------|-----------------|
| MC14014B | MC14021B | | | | |
| ↗ | X | X | 1 | 0 | 0 |
| ↗ | X | X | 1 | 1 | 1 |

* Q6, Q7, & Q8 are available externally

X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit | |
|--|--|-----------------|-------------------------------------|-----------|-------|---------------|-----------|-------|-----------|-----------|-----|
| | | | Min | Max | Min | Typ # | Max | Min | Max | | |
| Output Voltage "0" Level $V_{in} = V_{DD}$ or 0 | V_{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| $V_{in} = 0$ or V_{DD} "1" Level | V_{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc | |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | | |
| Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) | V_{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | |
| | (“1” Level $V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc) | V_{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc) | Source I_{OH} | 5.0 | -3.0 | — | -2.4 | -4.2 | — | -1.7 | — | mAdc | |
| | | 10 | -0.64 | — | -0.51 | -0.88 | — | -0.36 | — | | |
| | | 15 | -1.6 | — | -1.3 | -2.25 | — | -0.9 | — | | |
| | Sink I_{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc | |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | | |
| | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | | |
| Input Current | I_{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μ Adc | |
| Input Capacitance ($V_{in} = 0$) | C_{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF | |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μ Adc | |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | | |
| | | 15 | — | 15 | — | 0.015 | 15 | — | 600 | | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching) | I_T | 5.0 | $I_T = (0.75 \mu A/kHz) f + I_{DD}$ | | | | | | | μ Adc | |
| | | 10 | $I_T = (1.50 \mu A/kHz) f + I_{DD}$ | | | | | | | | |
| | | 15 | $I_T = (2.25 \mu A/kHz) f + I_{DD}$ | | | | | | | | |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

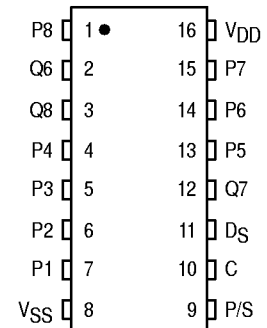
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.0015$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

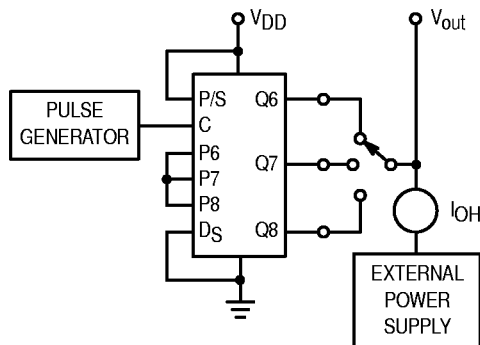


SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V _{DD} Vdc | Min | Typ # | Max | Unit |
|--|-------------------------|------------------------|-------------------|-------------------|-------------------|---------------|
| Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | $t_{TLH},$ t_{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time (Clock to Q, P/S to Q) $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 5.0 10 15 | — — — | 400 170 115 | 800 340 230 | ns |
| Clock Pulse Width | t_{WH} | 5.0 10 15 | 400 175 135 | 150 75 40 | — — — | ns |
| Clock Frequency | f_{cl} | 5.0 10 15 | — — — | 3.0 6.0 8.0 | 1.5 3.0 4.0 | MHz |
| Parallel/Serial Control Pulse Width | t_{WH} | 5.0 10 15 | 400 175 135 | 150 75 40 | — — — | ns |
| Setup Time P/S to Clock | t_{su} | 5.0 10 15 | 200 100 80 | 100 50 40 | — — — | ns |
| Hold Time Clock to P/S | t_h | 5.0 10 15 | 20 20 25 | -2.5 -10 0 | — — — | ns |
| Setup Time Data (Parallel or Serial) to Clock or P/S | t_{su} | 5.0 10 15 | 350 80 60 | 150 50 30 | — — — | ns |
| Hold Time Clock to D _S | t_h | 5.0 10 15 | 45 35 35 | 0 0 5 | — — — | ns |
| Hold Time Clock to P _n | t_h | 5.0 10 15 | 50 45 45 | 25 20 20 | — — — | ns |
| Input Clock Rise Time | $t_{r(cl)}$ | 5.0 10 15 | — — — | — — — | 15 5 4 | μs |

* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Preset output under test to a logic "1" level.

Figure 1. Output Source Current Test Circuit

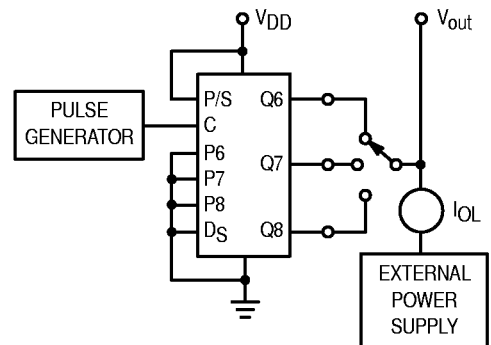


Figure 2. Output Sink Current Test Circuit

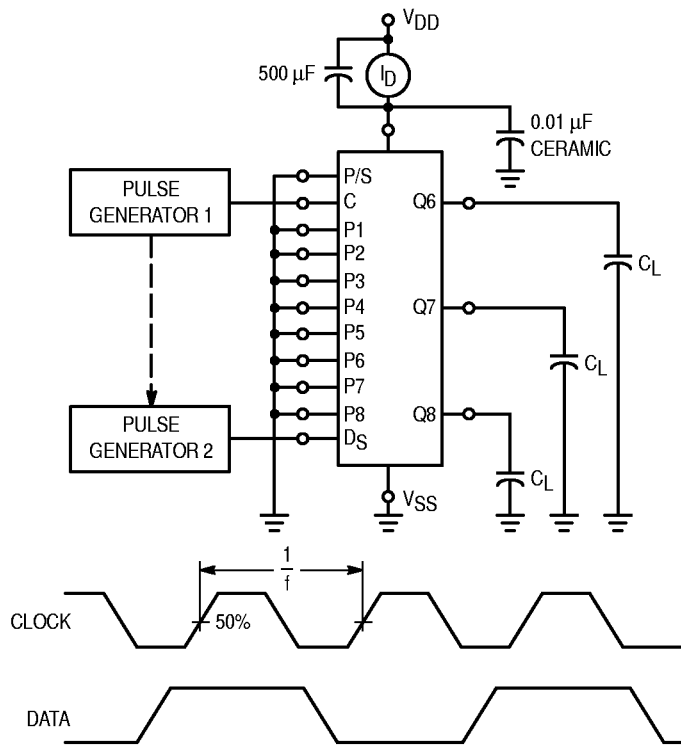


Figure 3. Power Dissipation Test Circuit and Waveform

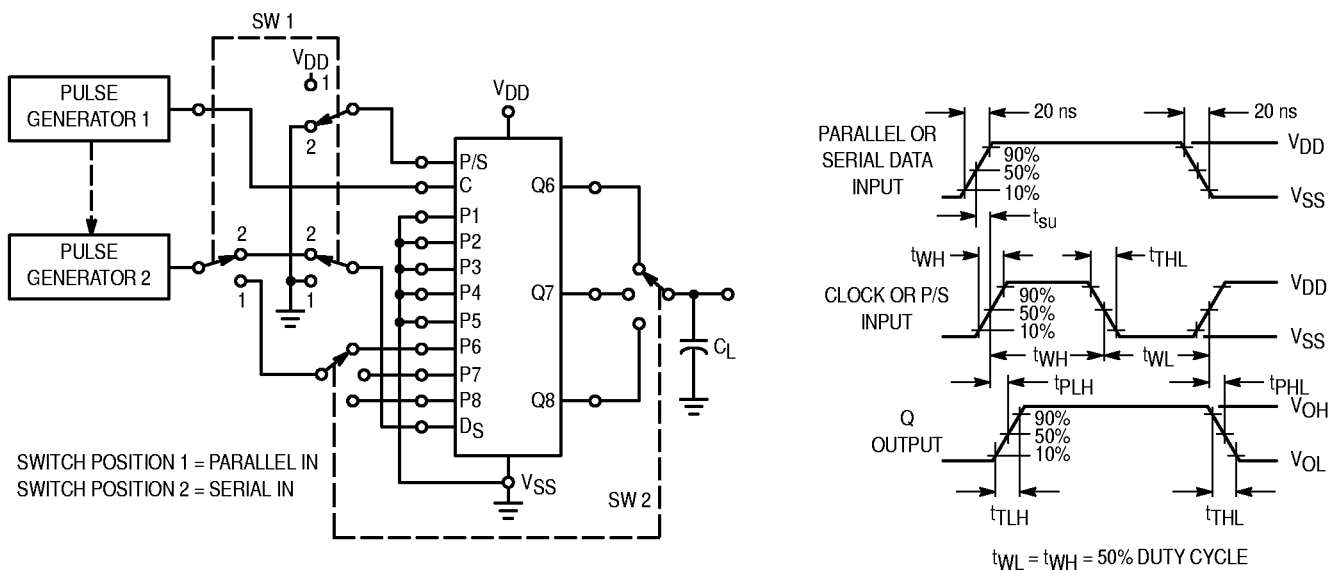
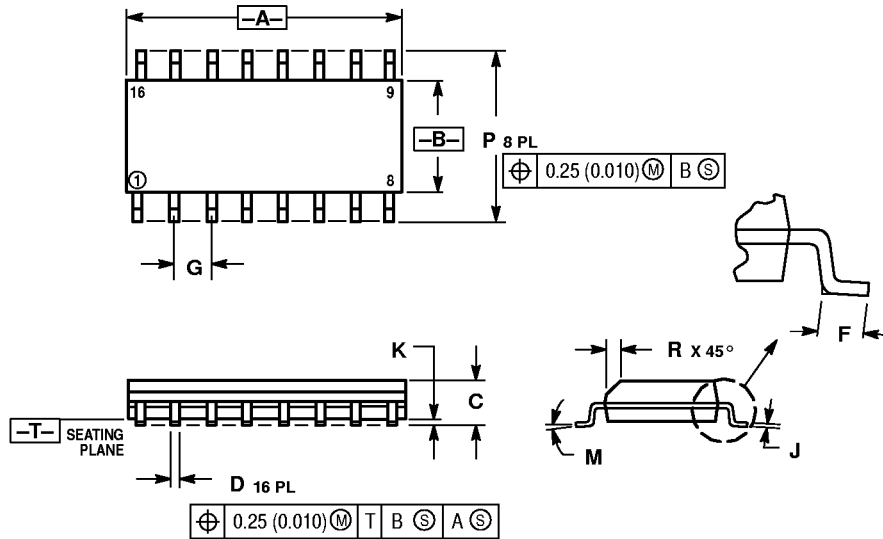


Figure 4. Switching Time Test Circuit and Waveforms

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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MC14014B/D

