NSB1010XV5T5

Preferred Device

Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

ON Semiconductor®

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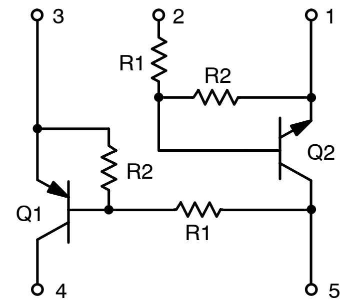
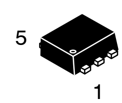
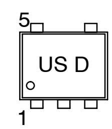




SOT−553
CASE 463B

MARKING DIAGRAM



US = Specific Device Code
D = Date Code

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB1010XV5T5, two complementary BRT devices are housed in the SOT−553 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- This device is manufactured with a Pb−Free external lead finish only.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−4 @ Minimum Pad.

ORDERING INFORMATION

Device	Package	Shipping†
NSB1010XV5T5	SOT−553 (Pb−Free)	2 mm pitch 8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

January, 2005 − Rev. 0

Publication Order Number:
NSB1010XV5/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Q1 TRANSISTOR: PNP					
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = −50 V, I_E = 0)	I_{CBO}	–	–	−100	nAdc
Collector-Emitter Cutoff Current (V_{CB} = −50 V, I_B = 0)	I_{CEO}	–	–	−500	nAdc
Emitter-Base Cutoff Current (V_{EB} = −6.0 V, I_C = 0)	I_{EBO}	–	–	−1.5	mAdc
Collector-Base Breakdown Voltage (I_C = −10 μA, I_E = 0)	$V_{(BR)CBO}$	−50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 2) (I_C = −2.0 mA, I_B = 0)	$V_{(BR)CEO}$	−50	–	–	Vdc
ON CHARACTERISTICS (Note 2)					
Collector-Emitter Saturation Voltage (I_C = −10 mA, I_B = −1.0 mA)	$V_{CE(sat)}$	–	–	−0.25	Vdc
DC Current Gain (V_{CE} = −10 V, I_C = −5.0 mA)	h_{FE}	15	27	–	–
Output Voltage (on) (V_{CC} = −5.0 V, V_B = −2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	−0.2	Vdc
Output Voltage (off) (V_{CC} = −5.0 V, V_B = −0.5 V, R_L = 1.0 kΩ)	V_{OH}	−4.9	–	–	Vdc
Input Resistor	R_1	3.3	4.7	6.1	kΩ
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	–
Q2 TRANSISTOR: NPN					
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CB} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0, I_C = 5.0 mA)	I_{EBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	h_{FE}	35	60	–	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)	$V_{CE(SAT)}$	–	–	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	7.0	10	13	kΩ
Resistor Ratio	R1/R2	0.8	1.0	1.2	–

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

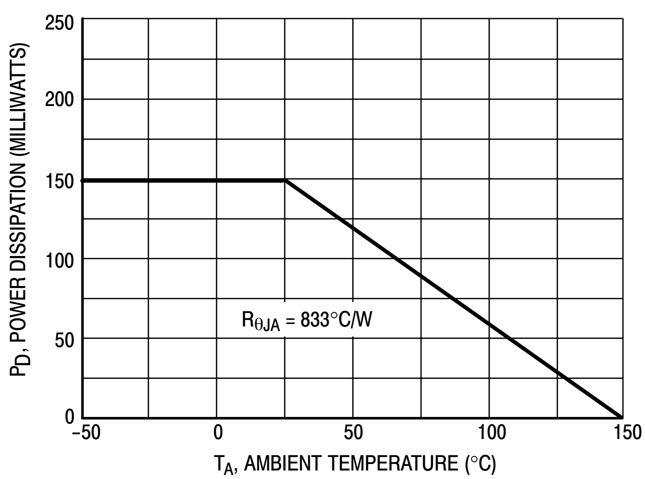


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS — PNP TRANSISTOR

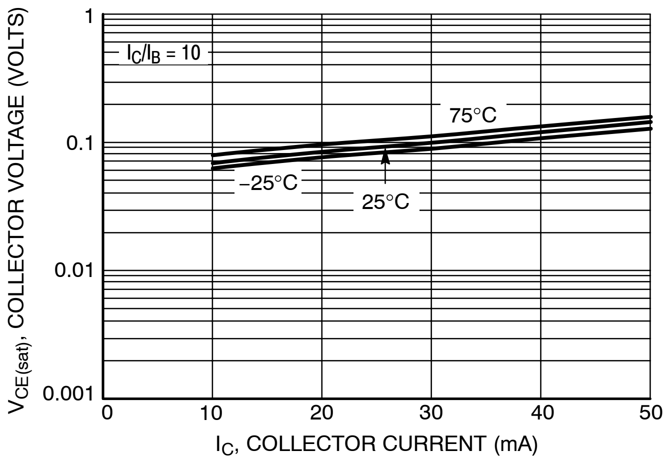


Figure 2. $V_{CE(sat)}$ versus I_C

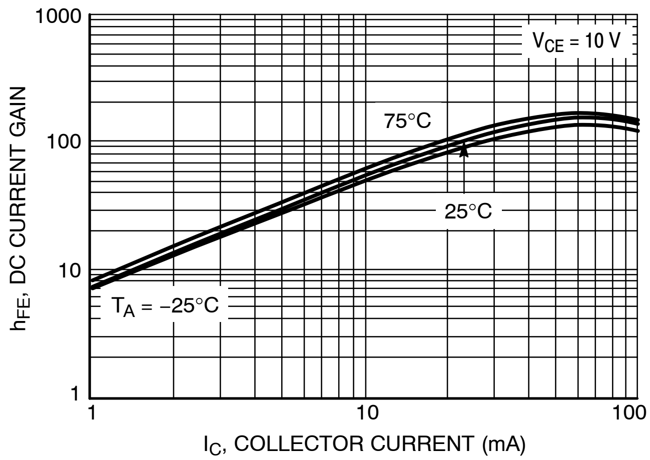


Figure 3. DC Current Gain

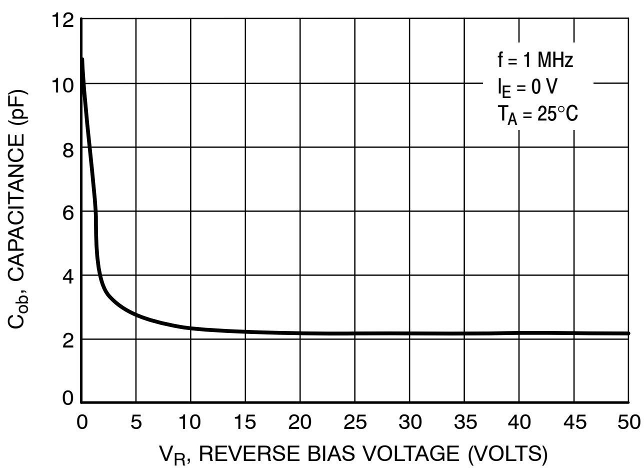


Figure 4. Output Capacitance

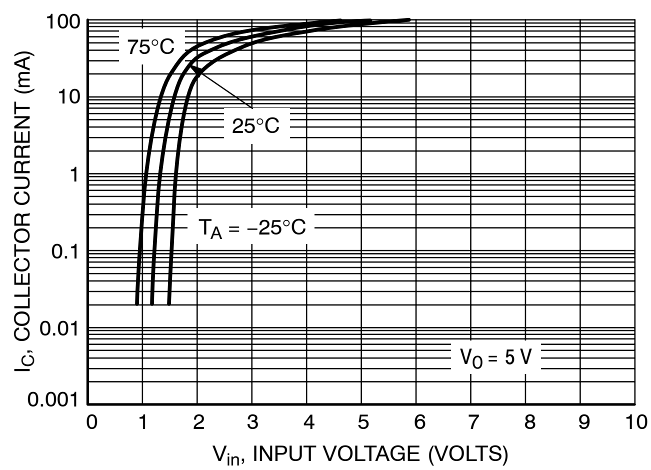


Figure 5. Output Current versus Input Voltage

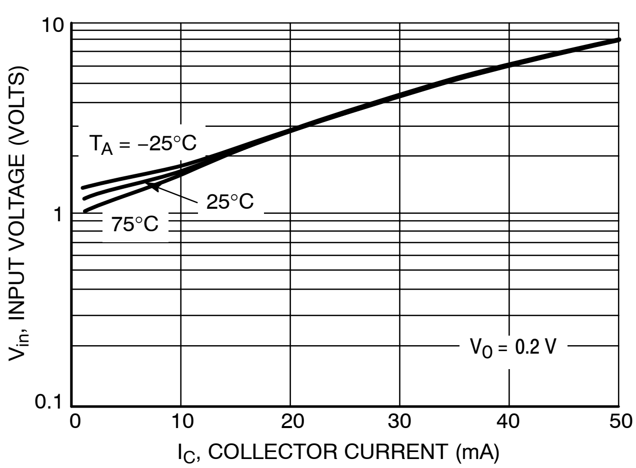


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

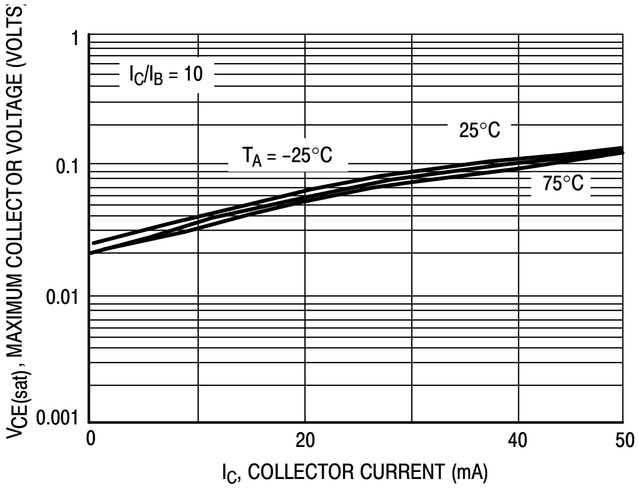


Figure 7. $V_{CE(sat)}$ versus I_C

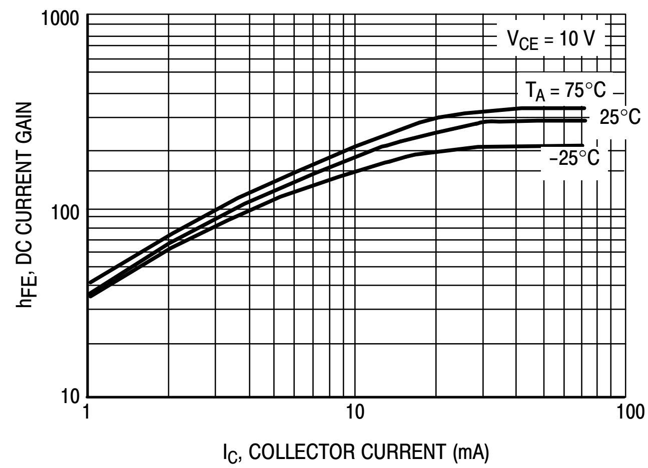


Figure 8. DC Current Gain

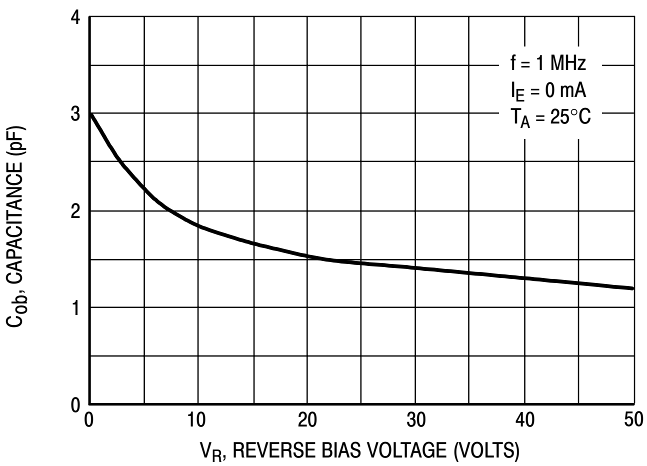


Figure 9. Output Capacitance

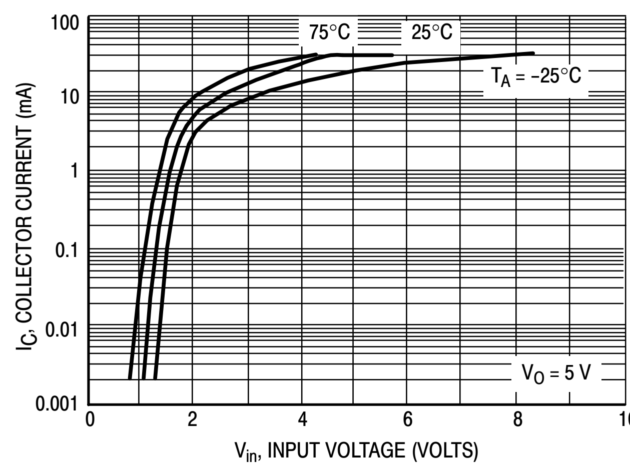


Figure 10. Output Current versus Input Voltage

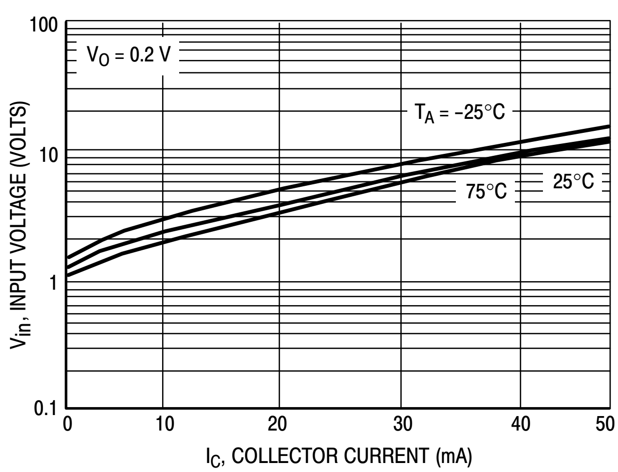
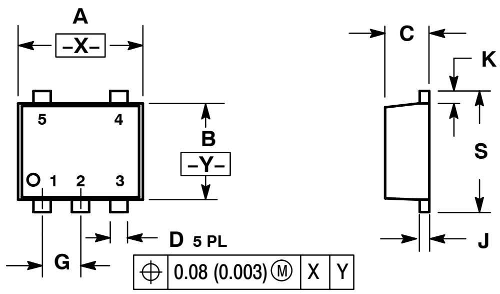


Figure 11. Input Voltage versus Output Current

PACKAGE DIMENSIONS

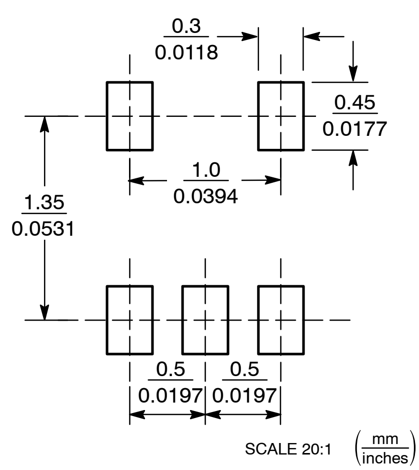
SOT−553
5−LEAD PACKAGE
CASE 463B−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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