FAIRCHILD
SEMICONDUCTOR™

ML4895

Synchronous Buck Controller

GENERAL DESCRIPTION

The ML4895 synchronous buck controller has been designed to provide high efficiency DC/DC conversion for portable products. The ML4895 can deliver a user programmable 2.5V to 4V output from input voltages of 5.9V to 15V.

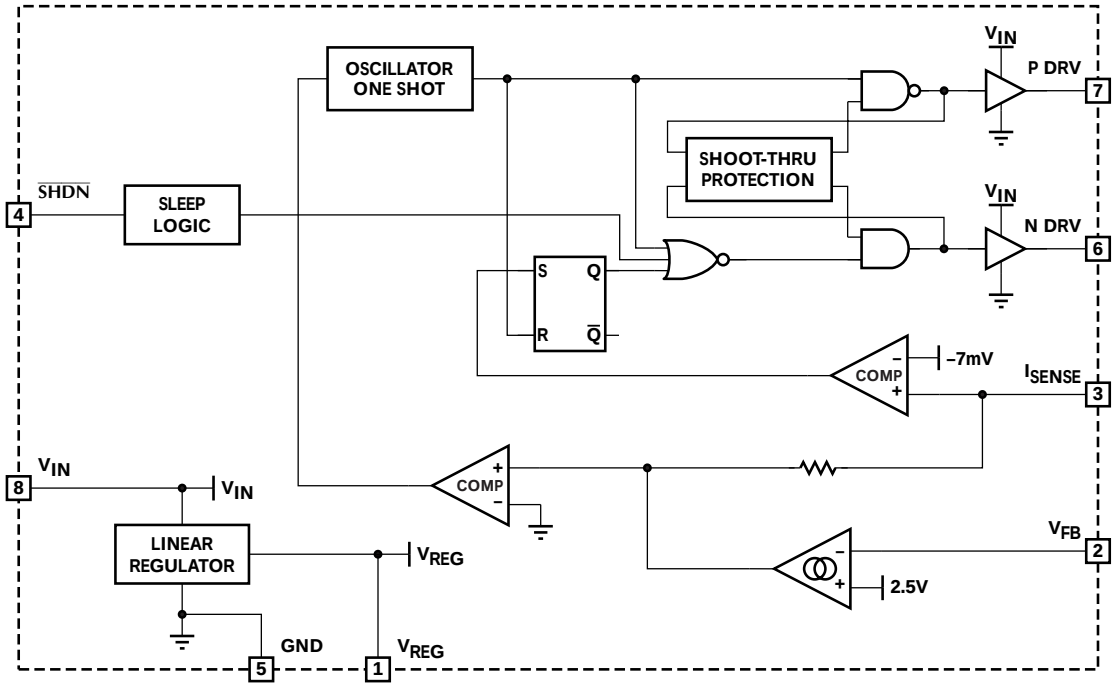
The ML4895 drives external P- and N-channel MOSFETs in a synchronous buck topology, allowing an overall conversion efficiency of greater than 90% over an output current range exceeding three decades, with an output current capability of up to 5A.

The regulator can be disabled via the $\overline{\text{SHDN}}$ pin. While disabled, the output of the regulator is completely isolated from the circuit's input supply, and the supply current is reduced to less than 5µA to help extend battery life.

FEATURES

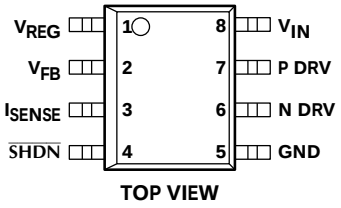
- Regulation to ±3% maximum
- Adjustable output synchronous buck (2.5V to 4V)
- Wide input voltage range (5.9V to 15V)
- Power conversion efficiencies of >90% over 3 decades of output current
- Integrated antishoot-through logic
- Shutdown control provides load isolation and minimum sleep mode power consumption

BLOCK DIAGRAM



PIN CONFIGURATION

ML4895
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{REG}	Connection point for internal linear regulator bypass capacitor
2	V_{FB}	Programming pin for setting the output voltage
3	I_{SENSE}	Current sense input
4	$\overline{SHDN}$	a logic low on this pin shuts down the regulator and all internal bias circuitry for minimum power consumption
5	GND	Analog signal ground
6	N DRV	NMOS driver output
7	P DRV	PMOS driver output
8	V_{IN}	Battery input voltage

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{IN} 16.5V
Peak Driver Output Current ..... ±2A
V_{FB} Voltage ..... GND - 0.3V to 6V
I_{SENSE} Voltage ..... ±500mV
All Other Inputs ..... GND - 0.3V to V_{IN} + 0.3V
$\overline{SHDN}$ Input Current 100µA
Junction Temperature 150ºC
Storage Temperature Range ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 150ºC
Thermal Resistance (θ_{JA}) 160ºC/W

OPERATING CONDITIONS

V_{IN} Range ..... 5.9V to 15V
V_{OUT} Range ..... 2.5V to 4V
Temperature Range ..... -20ºC to 70ºC

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 10V, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR						
	Output Voltage	T_A = 25ºC	3.29	3.33	3.37	V
	Line Regulation	5.9V < V_{IN} < 15V		1.7	4	mV/V
	Total Variation	Line, Temp	3.24		3.42	V
SHUTDOWN						
	Input Low Voltage				1.0	V
	Input High Voltage		3.0			V
	Input Low Current	V_{IL} = 0V			100	nA
	Input High Current	V_{IH} = V_{IN}			50	µA
BUCK REGULATOR						
	Duty Cycle Ratio	V_{IN} = 5.9V, I_{SENSE} = V_{FB} = 0V	75		97	%
	V_{FB} Threshold Voltage	5.9V < V_{IN} < 15V	2.425	2.5	2.575	V
	I_{SENSE} Threshold Voltage		-60	-80	-100	mV
	Transition Time	C_L = 1000 pF, GND to V_{IN}		50	100	ns
SUPPLY						
I_{IN}	V_{IN} Current	$\overline{SHDN}$ = 0V		2	5	µA
		$\overline{SHDN}$ = 5V		300	750	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

FUNCTIONAL DESCRIPTION

The ML4895 converts a 5.9V to 15V input to an adjustable 2.5V to 4V output using a unique current mode PFM synchronous buck control architecture. The output current is set by external components, and can exceed 2A. Even at light loads, the PFM architecture maintains high conversion efficiencies over a wide range of input voltages. If it is necessary to further extend battery life, the user can shutdown and fully disconnect the load from the input when the supply is not in use.

BIAS CIRCUITS

The bias circuits are comprised of a linear regulator and a precision 2.5V reference. The V_{REG} pin should be bypassed to GND with a 1µF capacitor. The 2.5V reference is used by the feedback circuit of the controller to maintain an accurate output voltage.

SHUTDOWN LOGIC

The ML4895 is shut down by applying a logic low to the $\overline{SHDN}$ pin. This prevents switching from occurring and disconnects the load from the input. The supply current in shutdown typically ranges from 0.5µA at V_{IN} = 5.9V to 3µA at V_{IN} = 15V

BUCK CONTROLLER

A block diagram of the buck controller is shown in Figure 1. The circuit utilizes a constant ON-time PFM control architecture. The circuit determines the OFF-time by waiting for the inductor current to drop to a level set by the feedback voltage (V_{FB}).

The oscillator/one shot block generates a constant ON-time and a minimum OFF-time. The OFF-time is extended for as long as the output of the current comparator stays low. Note that the inductor current flows in the current sense resistor during the OFF-time. Therefore, a minimum OFF-time is required to allow for the finite circuit delays in sensing the inductor current. The ON-time is triggered when the current comparator's output goes high. However, unlike conventional fixed ON-time controllers, this one shot has an inverse relationship with the input voltage as shown in Figure 2. Figure 3 plots the inductor voltage-ON-time product. Note that the volt-second product is nearly constant over the entire input voltage range. The inductor current is given by:

$$\Delta I_L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{L} \quad (1)$$

This means that the ripple current also remains nearly constant over the entire input voltage range.

The transconductance amplifier generates a current from the voltage difference between the reference and the feedback voltage, V_{FB}. This current produces a voltage across R_{gm} that adds to the negative voltage that is developed across the current sense resistor. When the current level in the inductor drops low enough (a less negative sense voltage) to cause the voltage at the non-inverting input of the current comparator to go positive, the comparator trips and starts a new ON cycle. In other words, the current programming comparator controls the length of the OFF-time by waiting until the inductor current decreases to a value determined by the transconductance amplifier.

This technique allows the feedback transconductance amplifier's output current to steer the current level in the inductor. The higher the transconductance amplifier's output current, the higher the inductor current. For example, when the output voltage drops due to a load increase, the transconductance amplifier will increase its output current and generate a larger voltage across R_{gm}, which in turn raises the inductor current trip level, shortening the OFF-time. At some level of increasing the output load, the transconductance amplifier can no longer continue to increase its output current. When this occurs, the voltage across R_{gm} reaches a maximum and the inductor current cannot increase. If the inductor current tries to increase, the voltage developed across the current sense resistor would become more negative, causing the non-inverting input of the current comparator to be negative, which extends the OFF-time and reduces the inductor current.

If the output voltage is too high, the transconductance amplifier's output current will eventually become negative. However, since the inductor current flows in only one direction (assuming no shoot-through current) the non-inverting input of the current comparator will also stay negative. This extends the OFF-time allowing the inductor current to decrease to zero, causing the converter to stop operation until the output voltage drops enough to increase the output current of the transconductance amp above zero.

In summary, the three operation modes can be defined by the voltage at the I_{SENSE} pin at the end of the OFF-time:

$V_{SENSE} \geq 0V$: Discontinuous current mode

$0V > V_{SENSE} > -60mV$: Continuous current mode

$-60mV > V_{SENSE} > -100mV$: Current limit

The synchronous rectifier comparator, flip-flop, and NOR gate make up the synchronous rectifier control circuit. The synchronous control does not influence the operation of the main control loop, and operation with a Schottky diode in place of the synchronous rectifier is possible, but at a lower conversion efficiency. The synchronous rectifier (N DRV) is turned on during the minimum OFF-time. N DRV will remain on until a new ON-time is started or until the I_{SENSE} pin goes above –7mV. When the I_{SENSE} pin goes above –7mV, the current in the inductor has gone to zero or the buck regulator is operating in discontinuous current mode (DCM). Therefore, the synchronous rectifier comparator is used only for DCM operation. A timing diagram is shown in Figure 4.

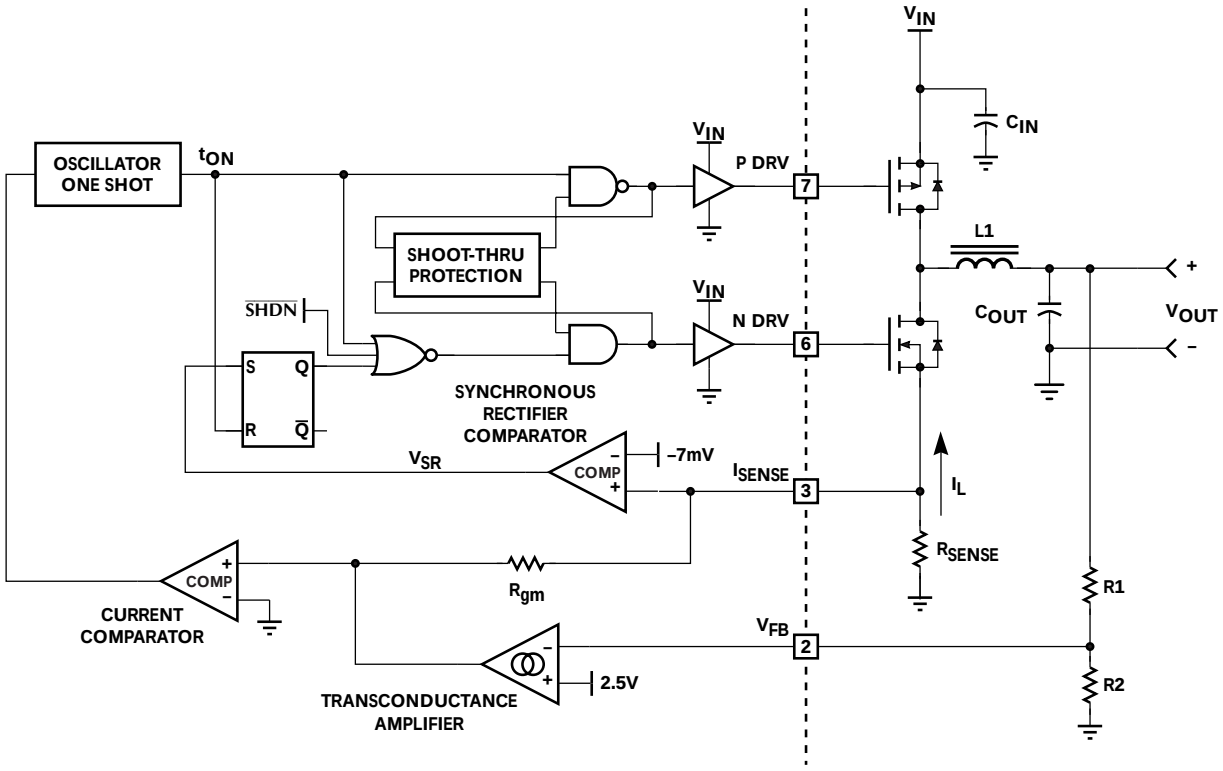


Figure 1. ML4895 Functional Block Diagram

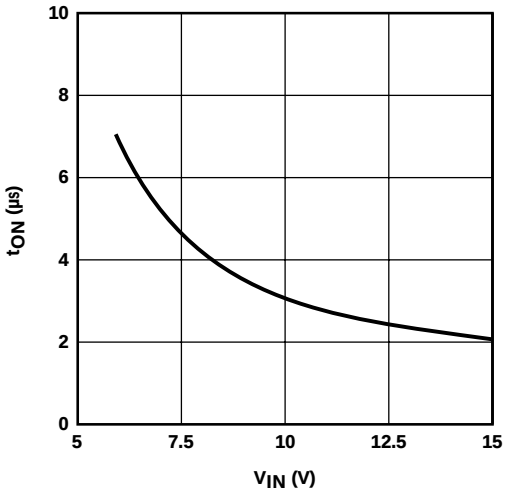


Figure 2. ON-Time vs. Input Voltage

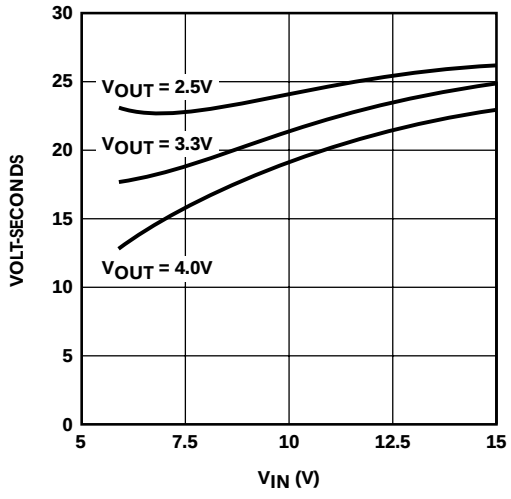


Figure 3. Volt-seconds vs. Input Voltage

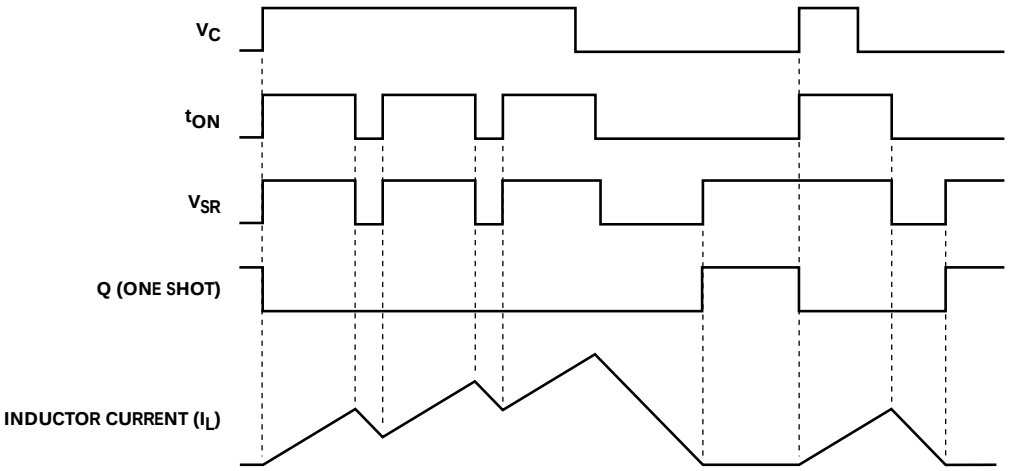


Figure 4. One Shot and Synchronous Rectifier Timing

DESIGN CONSIDERATIONS

A typical design can be implemented by using the following design procedure. Note that this procedure is not intended to give final values, but to give a good starting point, and provide the relationships necessary to make trade-off decisions. Some experimentation will be necessary to optimize values and to verify that the design operates over worst case conditions.

DESIGN SPECIFICATIONS

It is important to start with a clear definition of the design specifications. Make sure the specifications reflect worst case conditions. Key specifications include the minimum and maximum input voltage and the output voltage and load current.

INDUCTOR AND SENSE RESISTOR SELECTION

Figure 5 shows the inductor current of the buck regulator. The inductor current is made up of two components: the DC current level set by the transconductance amplifier, I_{SENSE}, and the inductor ripple current, ΔI_L. The figure also shows that I_{OUT} is the summation of I_{SENSE} and $\frac{1}{2}\Delta I_L$.

$$I_{OUT} = I_{SENSE} + \frac{1}{2} I_L = \frac{V_{SENSE}}{R_{SENSE}} + \frac{t_{ON} \times (V_{IN} - V_{OUT})}{2 \times L} \quad (2)$$

Therefore, the selection of the inductance value determines how much of the output current is made up of the ripple current. Higher inductor ripple current allows smaller inductor values, but results in higher peak currents, lower efficiency, and higher output voltage ripple.

Inductor ripple currents in the range of 30% to 70% of the maximum output current are typical. As a good starting point, set the inductor ripple current to 50% of the maximum output current:

$$\Delta I_L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{L} = F_{IRC} \times I_{OUT(MAX)} \quad (3)$$

where F_{IRC} = ratio of inductor ripple current to the maximum output current, or:

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{0.5 \times I_{OUT(MAX)}} \quad (4)$$

Calculate the inductance using the volt-seconds value given in Figure 3 at the maximum input voltage. Choose the nearest standard value, realizing the trade-offs mentioned before. Then, using the inductance value chosen, determine the actual inductor ripple current at the maximum and minimum input voltage using Equation 4 and Figure 3.

The sense resistor value can be determined using the inductor ripple current value calculated above and Equation 3 rearranged as follows:

$$R_{SENSE} = \frac{V_{SENSE(MIN)}}{I_{OUT(MAX)} - \frac{1}{2}\Delta I_{L(MIN)}} \quad (5)$$

Having determined the values for the inductor and sense resistor, we can now specify the inductor peak current rating. This value is calculated at current limit and at the maximum input voltage, and is given by:

$$I_{L(PEAK(MAX))} = I_{SENSE(MAX)} + \Delta I_{L(MAX)} \quad (6)$$

$$I_{L(PEAK(MAX))} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} + \Delta I_{L(MAX)}$$

$$I_{L(PEAK(MAX))} = \frac{0.1V}{R_{SENSE}} + \Delta I_{L(MAX)}$$

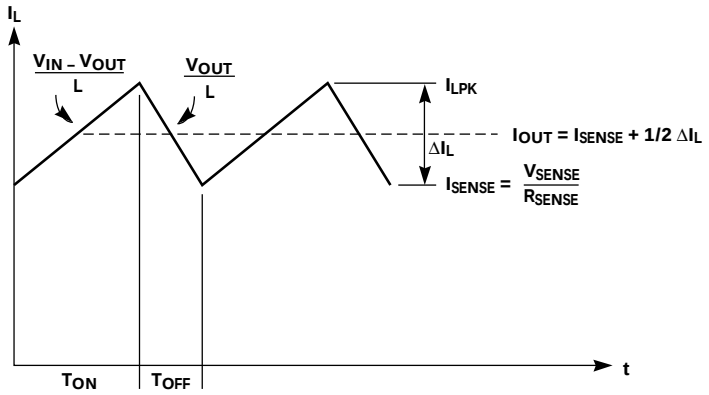


Figure 5. Buck Regulator Inductor Current

DESIGN CONSIDERATIONS (Continued)

For reliable operation, the inductor current rating should exceed the value calculated by 10%-20%.

For future reference, determine the peak inductor current at the minimum input voltage:

$$I_{L(PEAK(MIN))} = I_{SENSE(MIN)} + \Delta I_{L(MIN)} \quad (7)$$

$$I_{L(PEAK(MIN))} = \frac{V_{SENSE(MIN)}}{R_{SENSE}} + \Delta I_{L(MIN)}$$

$$I_{L(PEAK(MIN))} = \frac{0.06V}{R_{SENSE}} + \Delta I_{L(MIN)}$$

Now the sense resistor's power rating can be determined. The sense resistor must be able to carry the peak current in the inductor during the OFF-time:

$$P_{R_{SENSE}} = I_{RMS(OFF)}{}^2 \times R_{SENSE} \quad (8)$$

where:

$$I_{RMS(OFF)}{}^2 = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times \frac{I_{SENSE(MAX)}{}^2 + I_{SENSE(MAX)} \times I_{L(PEAK(MAX))} + I_{L(PEAK(MAX))}{}^2}{3}$$

The final parameter that should be specified is the winding resistance of the inductor. In general, the winding resistance should be as low as possible, preferably in the low mΩ range. Since the inductor is in series with the load at all times, the copper losses can be approximated by:

$$P_{Cu} = I_{OUT}{}^2 \times R_L \quad (9)$$

A good rule of thumb is to allow 2 mΩ of winding resistance per µH of inductance.

MOSFET SELECTION

The switching MOSFETs must be logic level types with the ON resistance specified at V_{GS} = 4.5V. In general, the ON resistance - gate charge product provides a good figure of merit by which to compare various MOSFETs, the lower the figure the better. The internal gate drivers of the ML4895 can drive over 100nC of total gate charge, but 60nC to 70nC is a more practical limit to ensure good switching times.

The drain-source breakdown voltage rating is determined by the input voltage. For input voltages up to 10V, a drain to source rating of 20V is acceptable. For input voltages up to 15V, a drain to source rating of 30V is recommended. For a more reliable design, look for MOSFETs that are avalanche rated.

In high current applications, the MOSFET's power dissipation often becomes a major design factor. The I^2R losses generate the largest portion of heat in the MOSFET package. Make sure that the MOSFETs are within their rated junction temperature at the maximum ambient temperature by calculating the temperature rise using the thermal resistance specifications.

The worst case power dissipation for the P-MOS switch occurs at the minimum input voltage and is determined as follows:

$$P_{P-MOS} = I_{RMS(ON)}{}^2 \times R_{DS(ON)} \quad (10)$$

where:

$$I_{RMS(ON)}{}^2 = \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right) \times \frac{I_{SENSE(MAX)}{}^2 + I_{SENSE(MAX)} \times I_{L(PEAK(MAX))} + I_{L(PEAK(MAX))}{}^2}{3}$$

DESIGN CONSIDERATIONS (Continued)

The worst case power dissipation for the N-MOS switch occurs at the maximum input voltage and is determined using:

$$P_{N-MOS} = I_{RMS(OFF)}^{2} \times R_{DS(ON)} \quad (11)$$

INPUT CAPACITOR SELECTION

The choice of the input capacitor is based on its ripple current and voltage ratings rather than its capacitance value. The input capacitor should be a low ESR type and located as close to the source of the P-MOS switch as possible. The input capacitor's ripple current is determined by the load current and input voltage, with the worst case condition occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS(C_{IN})} \approx (I_{SENSE(MAX)} + \frac{1}{2}\Delta I_{L(MAX)}) \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (12)$$

The capacitor's voltage rating is based on the maximum input voltage, $V_{IN(MAX)}$. Capacitor manufacturers typically recommend derating the capacitor voltage rating by 20% to 50% for aluminum electrolytic types and 50% to 70% for tantalum types.

In high current applications it may necessary to add a small 100nF ceramic capacitor to bypass the V_{IN} pin of the ML4895.

OUTPUT CAPACITOR SELECTION

The output capacitors determine the loop stability and the output ripple voltage. Use only low ESR capacitors intended for switching power supply applications, such as AVX TPS, Sprague 593D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the minimum capacitance value is given by:

$$C_{OUT} \geq \frac{4.3}{V_{OUT}} \times \frac{t_{ON(MAX)}}{R_{SENSE}} \quad (13)$$

The maximum ESR value can be estimated using:

$$ESR \leq \frac{\Delta V_{OUT}}{\Delta I_{L(MAX)}} \quad (14)$$

The selected capacitor must meet both the capacitance and ESR requirements. As a final check, make sure the output capacitor can handle the ripple current, I_{RMS}:

$$I_{RMS} \approx \frac{\Delta I_{L(MAX)}}{\sqrt{12}} \quad (15)$$

OUTPUTVOLTAGE

The output of the buck converter is adjustable and can be set to any voltage between 2.5V and 4V by connecting a resistor divider to the feedback pin as shown in Figure 1. The resistor values R1 and R2 can be calculated using the following equation:

$$V_{OUT} = 2.50V \times \frac{R1+R2}{R2} \quad (16)$$

The value of R2 should be 475kΩ or less to minimize bias current errors.

It is important to note that the accuracy of these resistors directly affects the accuracy of the output. Use precision resistors and set the nominal voltage approximately 1% to 2% high in order to make up for the load regulation. This offset results in the best overall output accuracy over line and load.

DESIGN CONSIDERATIONS (Continued)

LAYOUT

A typical application circuit is shown in Figure 6. Proximity of passive devices and adequate power and ground planes are critical for reliable operation of the circuit. In general, use the top layer for the high current connections and the bottom layer for the quiet connections such as GND, feedback and current sense. Some more specific guidelines follow.

1. The connection from the current sense resistor to the I_{SENSE} pin should be made by a separate trace and located as close to the lead of the resistor as possible. The trace length from the sense resistor to the ML4895 should be kept as short as possible and away from switching components and their traces.

2. The trace lengths from the buck regulator's input capacitor to the switching MOSFET, from the MOSFETs to the inductor, from the synchronous rectifier MOSFET to the sense resistor, and from the inductor to the output capacitor should all be as short as possible.

3. The high current ground paths need to be kept separate from the signal ground paths. The GND connection should be made at a single-point star ground. It is very important that the ground for the ML4895 GND pin be made using a separate trace.

4. Concentrating on keeping the current sense and high current connections short as well as keeping the switching components and traces away from the sensitive analog components and traces during layout will eliminate the majority of problems created by a poor layout.

5. The V_{REG} and bypass capacitor needs to be located close to the ML4895 for adequate filtering of the IC's internal bias voltage.

6. Remote sensing the output for improved load regulation can be implemented with the ML4895. The output can be remote sensed by using the top of the external resistor divider as the remote sense point.

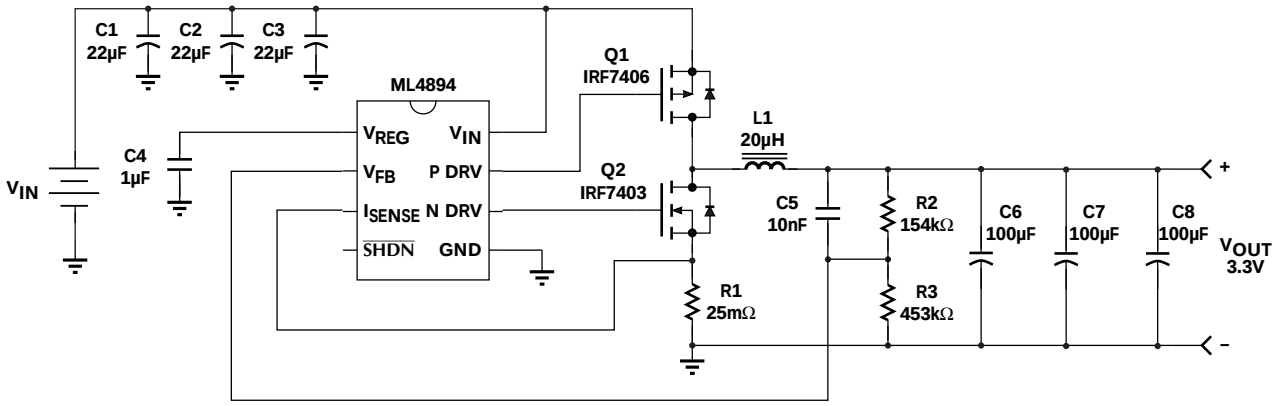
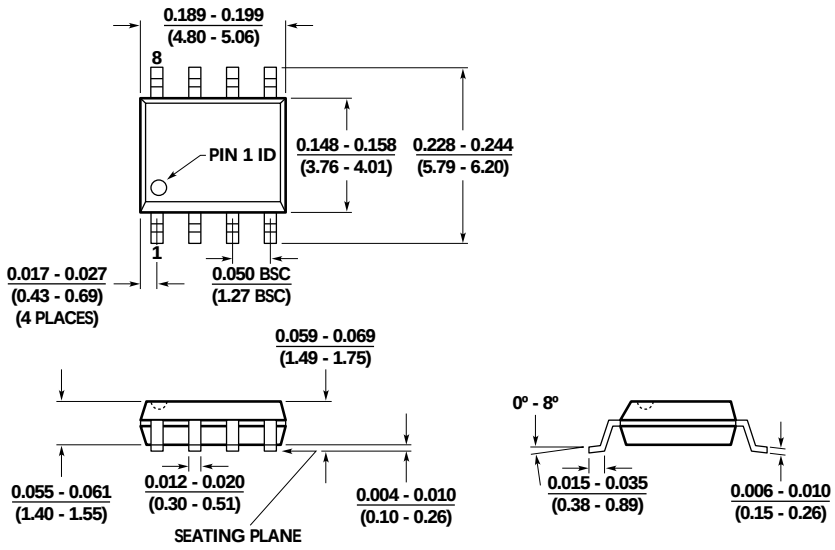


Figure 6. 3.3V, 3A DC/DC Converter Circuit

PHYSICAL DIMENSIONS inches (millimeters)

Package: S08
8-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4895ES	-20ºC to 70ºC	8-Pin SOIC (S08)