May 2014

FDMS7606

Dual N-Channel PowerTrench® MOSFET

Q1: 30 V, 12 A, 12.0 mΩ Q2: 30 V, 22 A, 11.6 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 12.0 mΩ at V_{GS} = 10 V, I_D = 11.5 A
- Max $r_{DS(on)}$ = 16.4 mΩ at V_{GS} = 4.5 V, I_D = 10 A

Q2: N-Channel

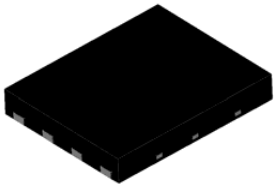
- Max $r_{DS(on)}$ = 11.6 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 17.2 mΩ at V_{GS} = 4.5 V, I_D = 9.5 A
- RoHS Compliant

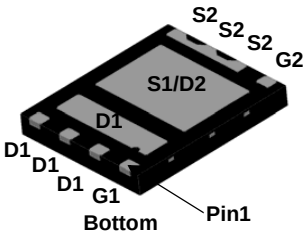
General Description

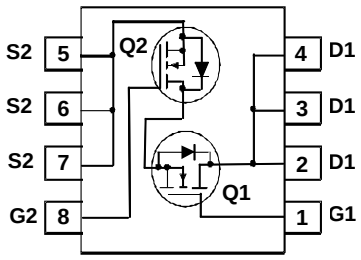
This device includes two specialized N-Channel MOSFETs in a dual MLP package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook Charger







Power 56

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
I_D	Drain Current -Continuous	T_C = 25 °C	12	22	A
	-Continuous	T_A = 25 °C	11.5[1a]	12[1b]	
	-Pulsed		50	60	
E_{AS}	Single Pulse Avalanche Energy	(Note 4)	25	33	mJ
P_D	Power Dissipation for Single Operation	T_A = 25°C	2.2[1a]	2.5[1b]	W
	Power Dissipation for Single Operation	T_A = 25°C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125[1c]	120[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.6	4.7	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7606	FDMS7606	Power 56	13 ”	12 mm	3000 units

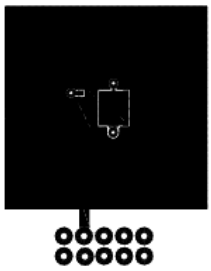
Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	Q1 Q2		16 20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 1	μA
I_{GSS}	Gate to Source Leakage Curent	V_{GS} = 20 V, V_{DS} = 0 V V_{GS} = ±20 V, V_{DS} = 0 V	Q1 Q2			100 ±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	1.0 1.0	2.1 1.9	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	Q1 Q2		-6 -5.5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 11.5 A V_{GS} = 4.5 V, I_D = 10 A V_{GS} = 10 V, I_D = 11.5 A, T_J = 125°C	Q1		9.2 12.6 11.8	12.0 16.4 14.7	mΩ
		V_{GS} = 10 V, I_D = 12 A V_{GS} = 4.5 V, I= 9.5 A V_{GS} = 10 V, I_D = 12 A, T_J = 125°C	Q2		9.7 12.8 12.3	11.6 17.2 15.4	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 11.5 A V_{DD} = 5 V, I_D = 12 A	Q1 Q2		53 47		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1050 947	1400 1260	pF
C_{oss}	Output Capacitance	Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		295 191	395 255	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		32 131	50 200	pF
R_g	Gate Resistance		Q1 Q2	0.2 0.2	1.6 1.0	4.0 2.5	Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 11.5 A, R_{GEN} = 6 Ω	Q1 Q2		7 6	14 12	ns
t_r	Rise Time		Q1 Q2		3 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 V_{DD} = 15 V, I_D = 12 A, R_{GEN} = 6 Ω	Q1 Q2		18 19	33 34	ns
t_f	Fall Time		Q1 Q2		3 3	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 10 V; Q1 V_{DD} = 15 V, I_D = 11.5 A	Q1 Q2		16 19	22 27	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 5 V; Q1 V_{DD} = 15 V, I_D = 11.5 A	Q1 Q2		8 10	11 15	nC
Q_{gs}	Gate to Source Charge	Q2 V_{DD} = 15 V, I_D = 12 A	Q1 Q2		3.2 2.6		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		2.0 4.2		nC

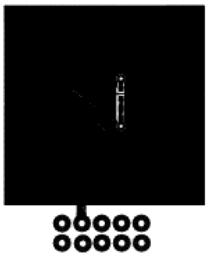
Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	Q1		0.76	1.2	V
		V_{GS} = 0 V, I_S = 11.5 A (Note 2)	Q1		0.87	1.2	
		V_{GS} = 0 V, I_S = 2 A (Note 2)	Q2		0.75	1.2	
		V_{GS} = 0 V, I_S = 12 A (Note 2)	Q2		0.85	1.2	
t_{rr}	Reverse Recovery Time	Q1 I_F = 11.5 A, di/dt = 100 A/s	Q1		22	35	ns
			Q2		18	33	
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 12 A, di/dt = 100 A/s	Q1		7	13	nC
			Q2		6	12	

Notes:
1.$R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

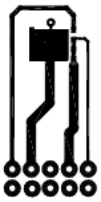


a. 57 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper

c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied

4. Q1: E_{AS} of 25 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 13 A, V_{DD} = 27 V, V_{GS} = 10 V.

Q2: E_{AS} of 33 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 15 A, V_{DD} = 27 V, V_{GS} = 10 V.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

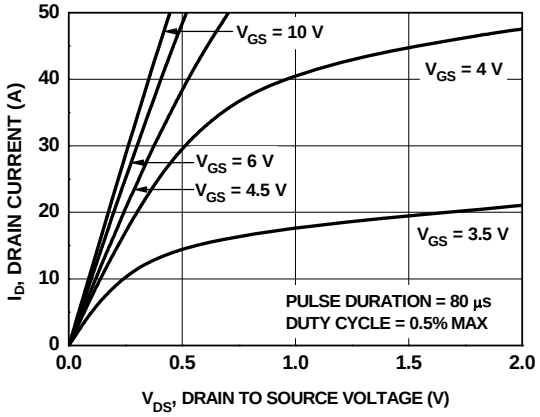


Figure 1. On Region Characteristics

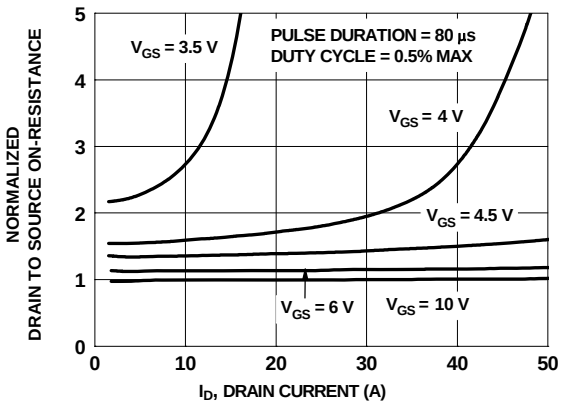


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

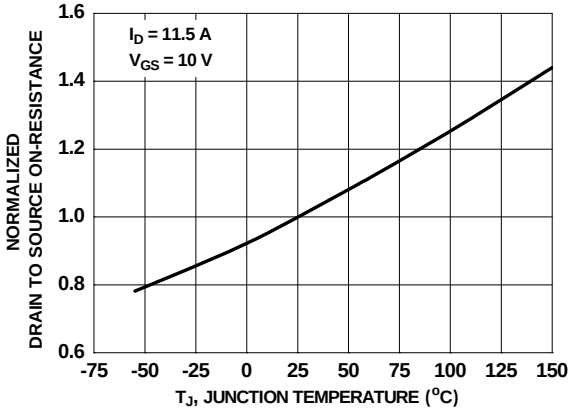


Figure 3. Normalized On Resistance vs Junction Temperature

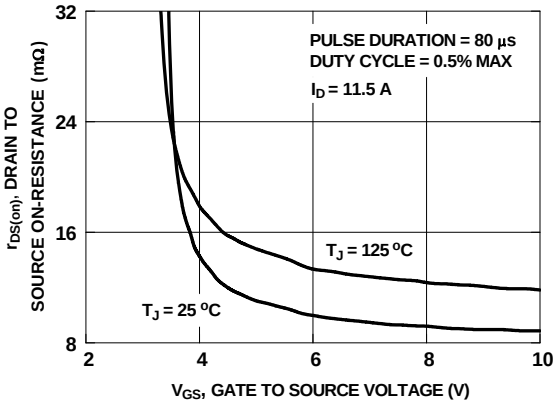


Figure 4. On-Resistance vs Gate to Source Voltage

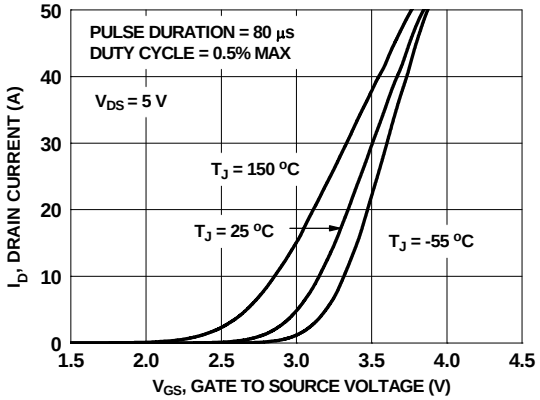


Figure 5. Transfer Characteristics

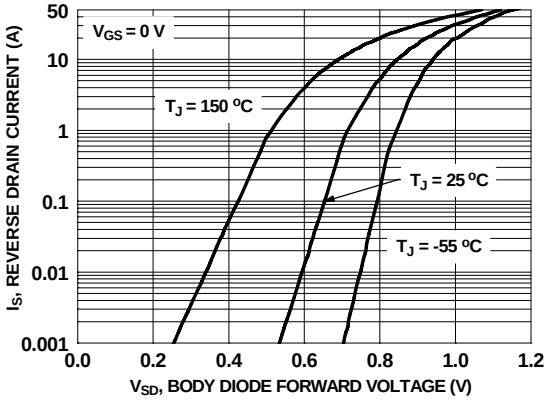


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

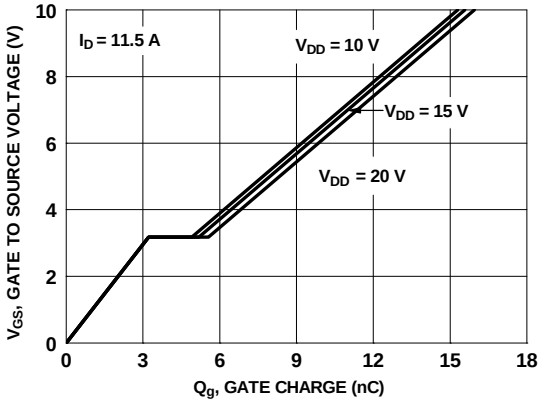


Figure 7. Gate Charge Characteristics

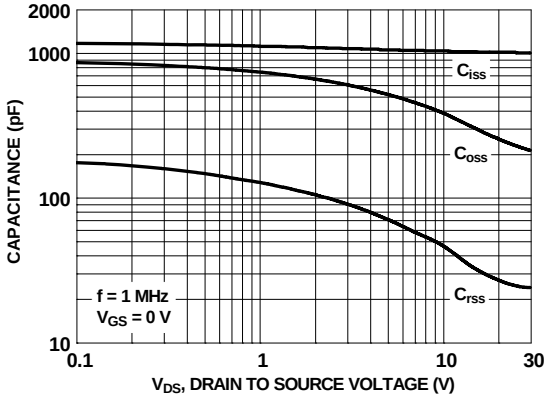


Figure 8. Capacitance vs Drain to Source Voltage

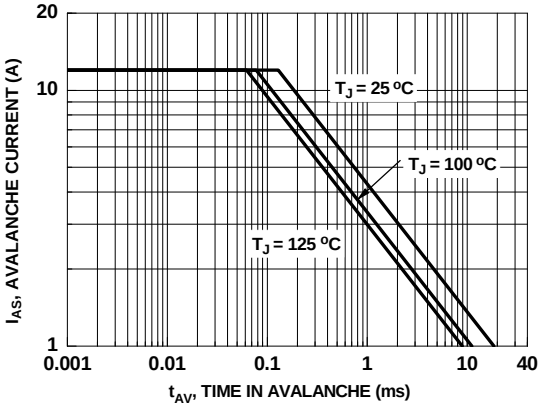


Figure 9. Unclamped Inductive Switching Capability

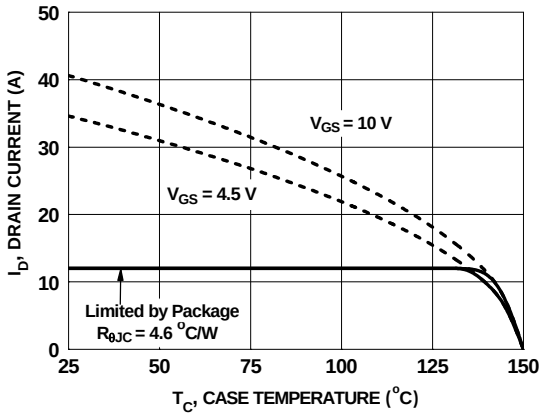


Figure 10. Maximum Continuous Drain Current vs Case Temperature

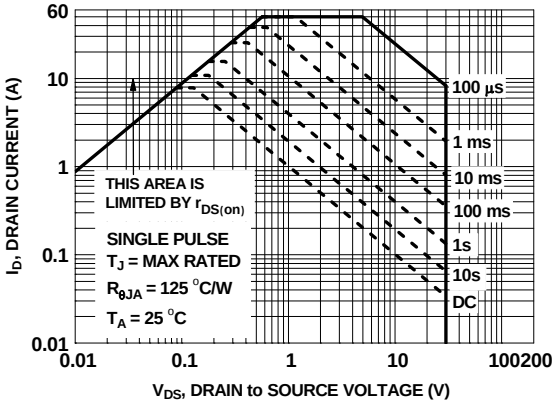


Figure 11. Forward Bias Safe Operating Area

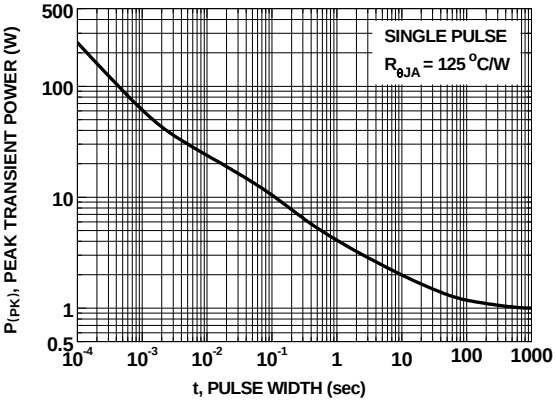


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

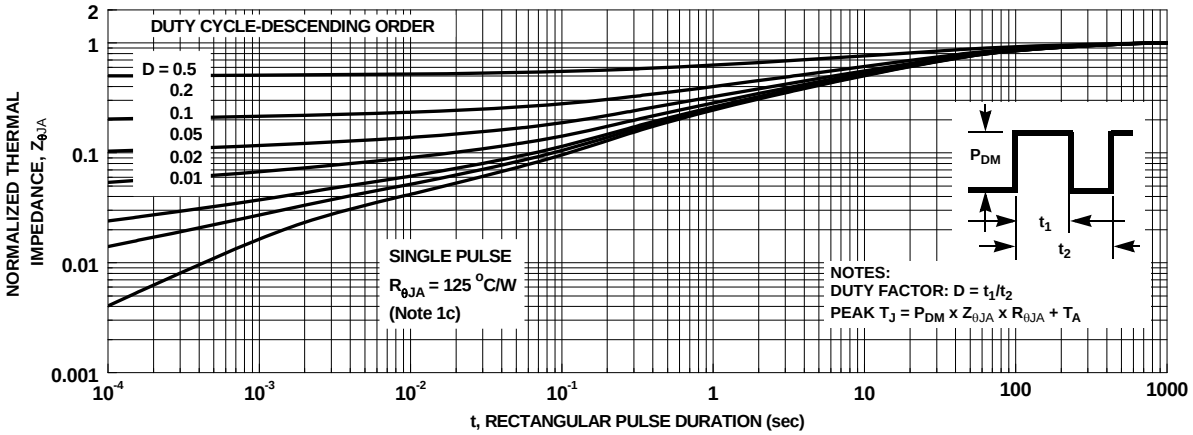


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

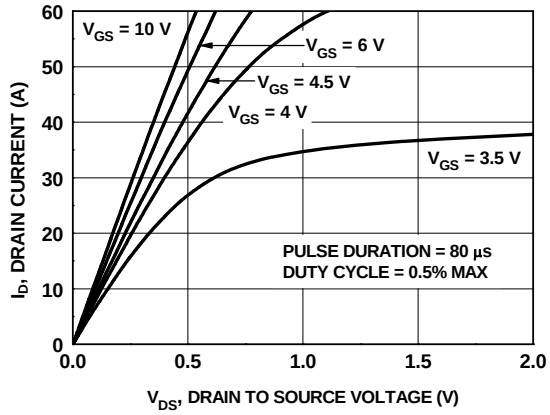


Figure 14. On-Region Characteristics

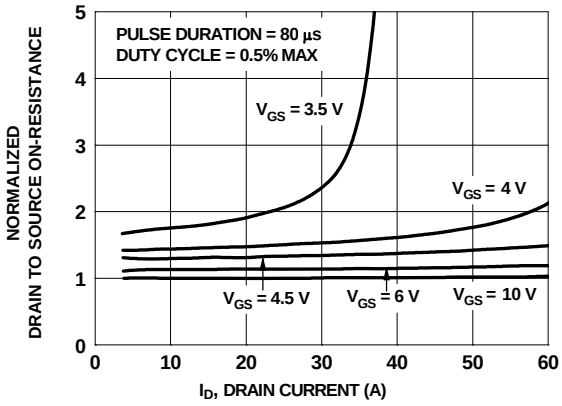


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

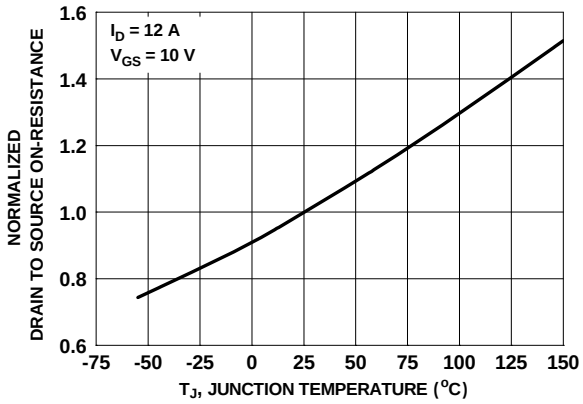


Figure 16. Normalized On-Resistance vs Junction Temperature

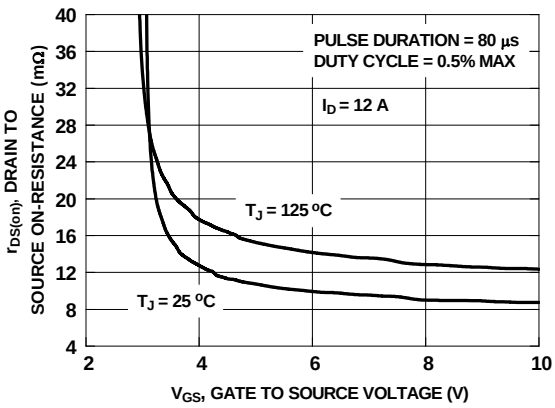


Figure 17. On-Resistance vs Gate to Source Voltage

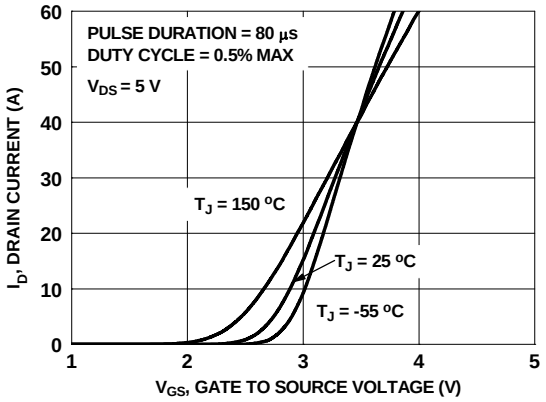


Figure 18. Transfer Characteristics

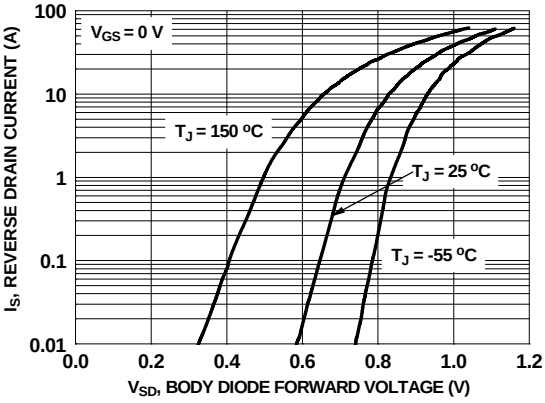


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted

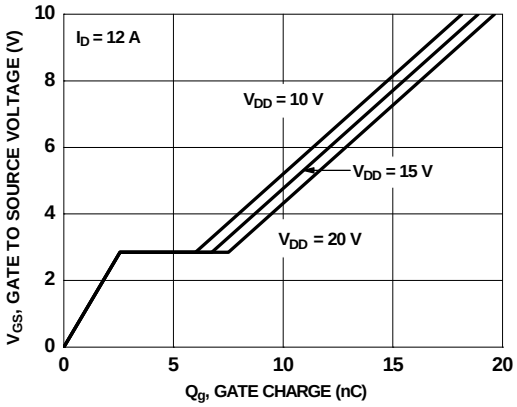


Figure 20. Gate Charge Characteristics

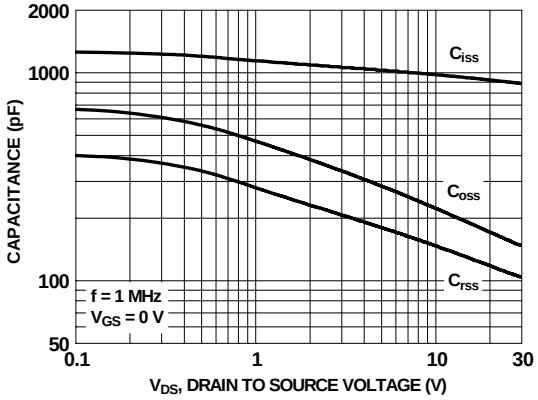


Figure 21. Capacitance vs Drain to Source Voltage

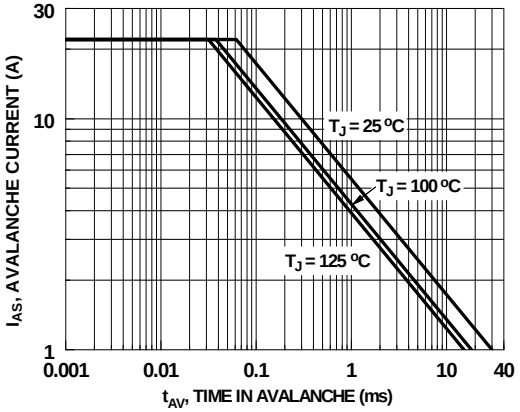


Figure 22. Unclamped Inductive Switching Capability

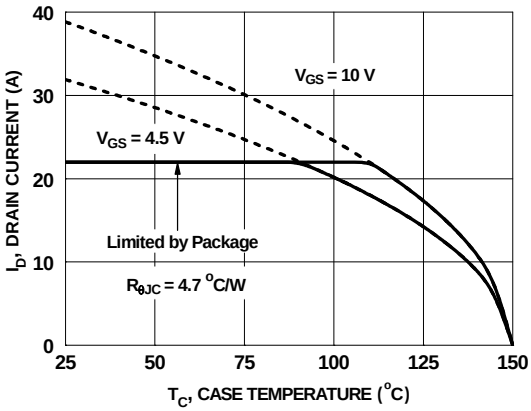


Figure 23. Maximum Continuous Drain Current vs Case Temperature

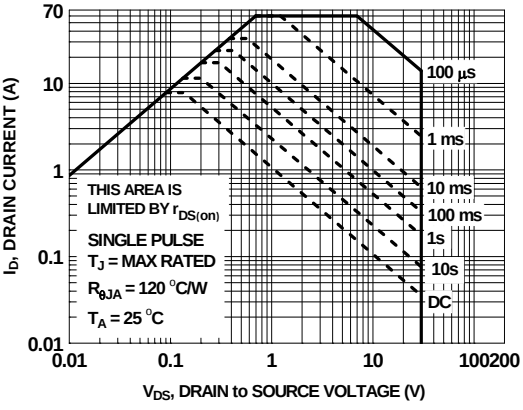


Figure 24. Forward Bias Safe Operating Area

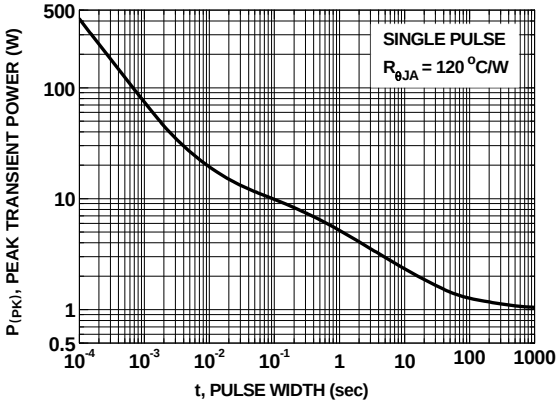


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

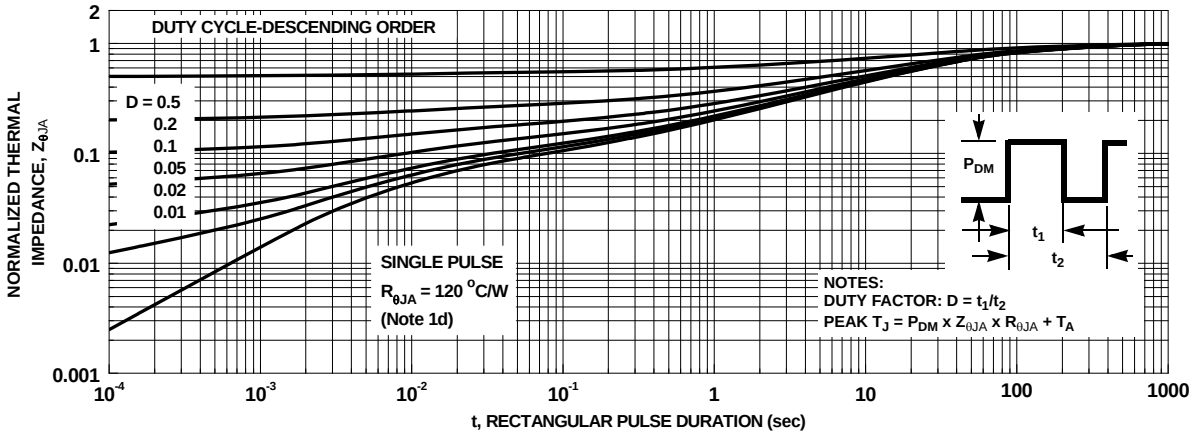


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

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SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
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SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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