FAIRCHILD SEMICONDUCTOR®

October 2009

SPM™

FSB67508

Smart Power Module (SPM®)

Features

- $R_{DS(ON).MAX}$=11mΩ @ I_D=38A,T_J=25°C a half-bridge FRFET inverter including high voltage integrated circuit (HVIC)
- Negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and protection functions
- 3/5V CMOS/TTL compatible, active-high interface
- Isolation voltage rating of 1500Vrms for 1min.
- Embedded bootstrap diode in the package

General Description

FSB67508 is a smart power module (SPM®) as a compact solution for small power motor drive applications such as E-bike. It is composed of 2 MOSFET, and 1 half-bridge HVIC for gate driving. This offers an extremely compact, high performance half-bridge inverter in a single isolated package . The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned.

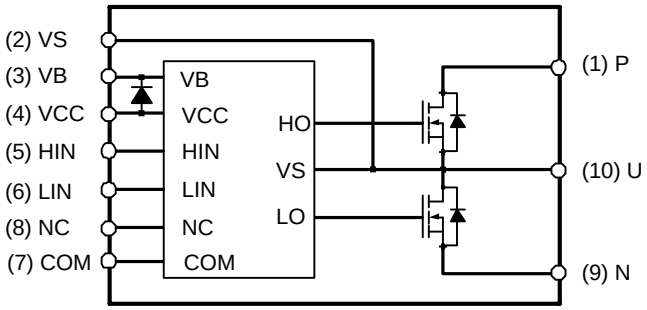
Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FET		75	V
I_{D25}	Each FET Drain Current, Continuous	T_C = 25°C	38	A
I_{D80}	Each FET Drain Current, Continuous	T_C = 80°C	28	A
I_{DP}	Each FET Drain Current, Peak	T_C = 25°C, Pulsed*	95	A
P_D	Maximum Power Dissipation	T_C = 25°C, Each	32	W
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between V_B and U	20	V
V_{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC	V
T_J	Operating Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-50 ~ 150	°C
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each under inverter operating condition (Note 1)	3.9	°C/W

*Repetitive rating : Pulse width limited by maximum junction temperature

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	P	Positive DC–Link Input
2	VS	Bias Voltage Ground for High Side MOSFET Driving
3	VB	High-side Bias Voltage for MOSFET Driving
4	VCC	Bias Voltage for IC and Low side MOSFET Driving
5	HIN	Signal Input for High-side
6	LIN	Signal Input for Low-side
7	COM	Common Supply Ground
8	NC	No connection
9	N	Negative DC-Link Input
10	U	Output



Note:
Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside SPM®. External connections should be made as indicated in Figure2.

Figure 1. Internal Block Diagram

Electrical Characteristics (T_J = 25°C, V_{CC}=V_{BS}=15V Unless Otherwise Specified)

Inverter Part (Each MOSFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{IN}= 0V, I_D = 250μA (Note 2)	75	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.6	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN}= 0V, V_{DS} = 75V	-	-	250	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{CC} = V_{BS} = 15V, V_{IN} = 5V, I_D = 15A	-	9.4	11	mΩ
V_{SD}	Drain-Source Diode Forward Voltage	V_{CC} = V_{BS} = 15V, V_{IN} = 0V, I_D = 15A	-	-	1.2	V
t_{ON}	Switching Times	V_{PN} = 48V, V_{CC} = V_{BS} = 15V, I_D = 15A V_{IN} = 0V ↔ 5V Inductive load L=3mH High- and low-side FET switching (Note 3)	-	550	-	ns
t_{OFF}			-	2000	-	ns
t_{rr}			-	100	-	ns
E_{ON}			-	40	-	μJ
E_{OFF}			-	190	-	μJ
RBSOA	Reverse-bias Safe Operating Area	V_{PN} = 55V, V_{CC} = V_{BS} = 15V, I_D = I_{DP}, V_{DS}=BV_{DSS}, T_J = 150°C High- and low-side FET switching (Note 3)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{QCC}	Quiescent V_{CC} Current	V_{CC}=15V, V_{IN}=0V	Applied between V_{CC} and COM	-	-	160	μA
I_{QBS}	Quiescent V_{BS} Current	V_{BS}=15V, V_{IN}=0V	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	-	-	100	μA
UV_{CCD}	Low-side Undervoltage Protection (Figure 6)	V_{CC} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV_{CCR}		V_{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV_{BSD}	High-side Undervoltage Protection (Figure 7)	V_{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV_{BSR}		V_{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V_{IH}	ON Threshold Voltage	Logic High Level	Applied between IN and COM	3.0	-	-	V
V_{IL}	OFF Threshold Voltage	Logic Low Level		-	-	0.8	V
I_{IH}	Input Bias Current	V_{IN} = 5V	Applied between IN and COM	-	10	20	μA
I_{IL}		V_{IN} = 0V		-	-	2	μA

Note:

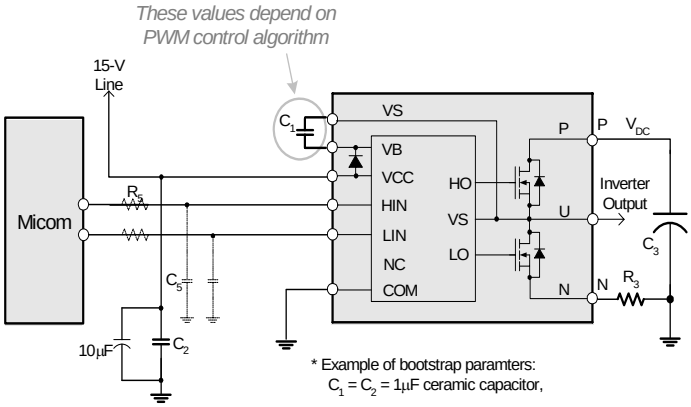
1. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FET inside SPM®. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.
2. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applcations due to the effect of different printed circuit boards and wirings. Please see Figure 3 for the switching time definition with the switching test circuit of Figure 4.
3. The peak current and voltage of each FET during the switching operation should be included in the safe operating area (SOA). Please see Figure 4 for the RBSOA test circuit that is same as the switching test circuit.

Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FSB67508	FSB67508	SPM10-AA	_	_	19

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P and N	-	48	60	V
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between V_B and output	13	15	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between IN and COM	3.0	-	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	Blanking Time for Preventing Arm-short	V_{CC}=V_{BS}=13.5 ~ 20V, $T_J \leq 150°C$	1.0	-	-	μs
f_{PWM}	PWM Switching Frequency	$T_J \leq 150°C$	-	15	-	kHz



FO	HIN	LIN	Output	Note
1	0	0	Z	Both FET Off
1	0	1	0	Low-side FET On
1	1	0	V_{DC}	High-side FET On
1	1	1	Forbidden	Shoot-through
1	Open	Open	Z	Same as (0, 0)
0	x	x	Z	Same as (0, 0)

Note:

(1) The snubber capacitor, C3, should be placed near SPM®

(2) Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.

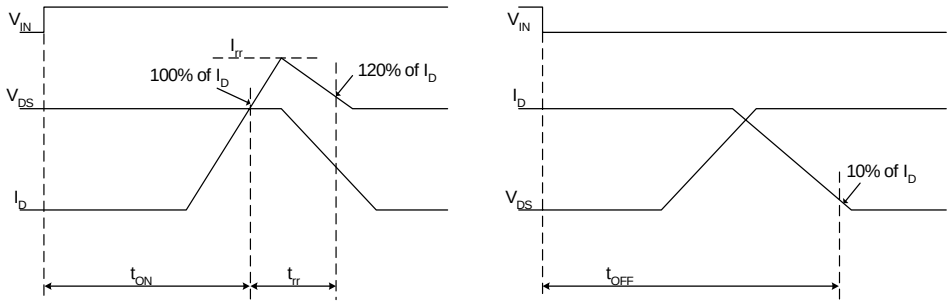
(3) RC coupling(R_5 and C_5) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM® is compatible with standard CMOS or LSTTL outptus.

(4) Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C_1, C_2 and C_3 should have good high-frequency characteristics to absorb high-frequency ripple current.

Figure 2. Recommended CPU Interface and Bootstrap Circuit with Parameters

Bootstrap Diode Part

Symbol	Parameter	Conditions	Rating	Units
V_{RRM}	Maixmum Repetitive Reverse Voltage		75	V
I_F	Forward Current	T_C = 25°C	0.5	A
I_{FP}	Forward Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	2	A
T_J	Operating Junction Temperature		-40 ~ 150	°C
R_B	Equivalent Bootstrap Resistance	T_C = 25°C	15	Ω



(a) Turn-on **(b) Turn-off**

Figure 3. Switching Time Definition

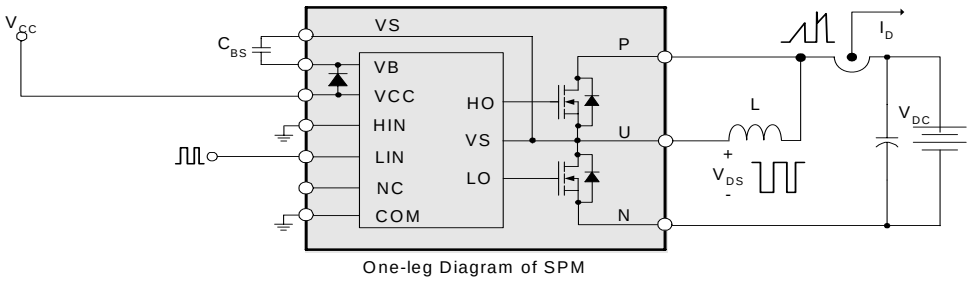


Figure 4. Switching and RBSOA(Single-pulse) Test Circuit (Low-side)

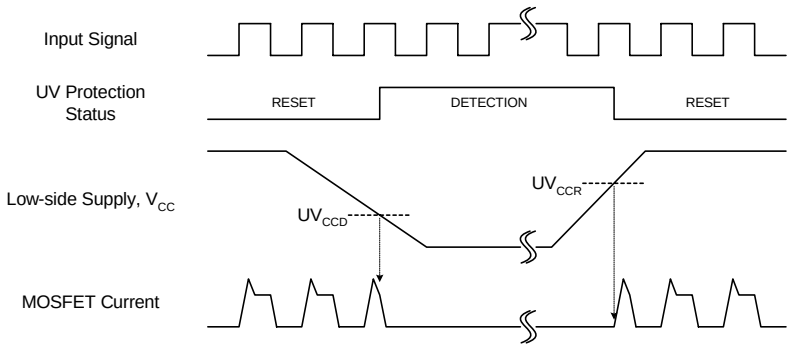


Figure 5. Undervoltage Protection (Low-side)

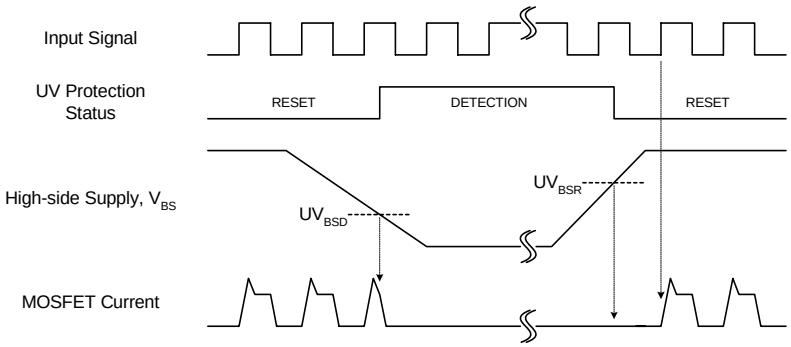


Figure 6. Undervoltage Protection (High-side)

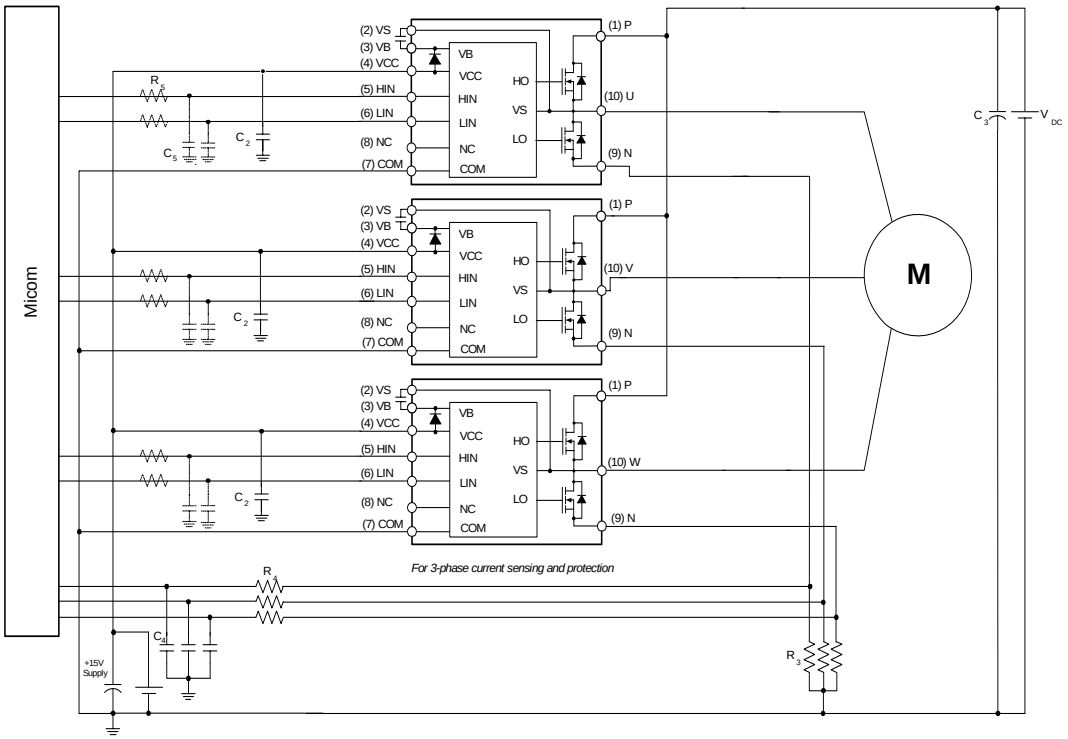
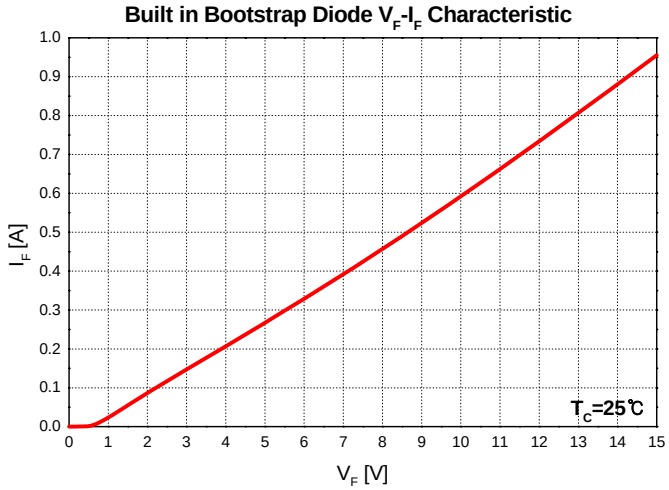


Fig. 7. Example of Application Circuit

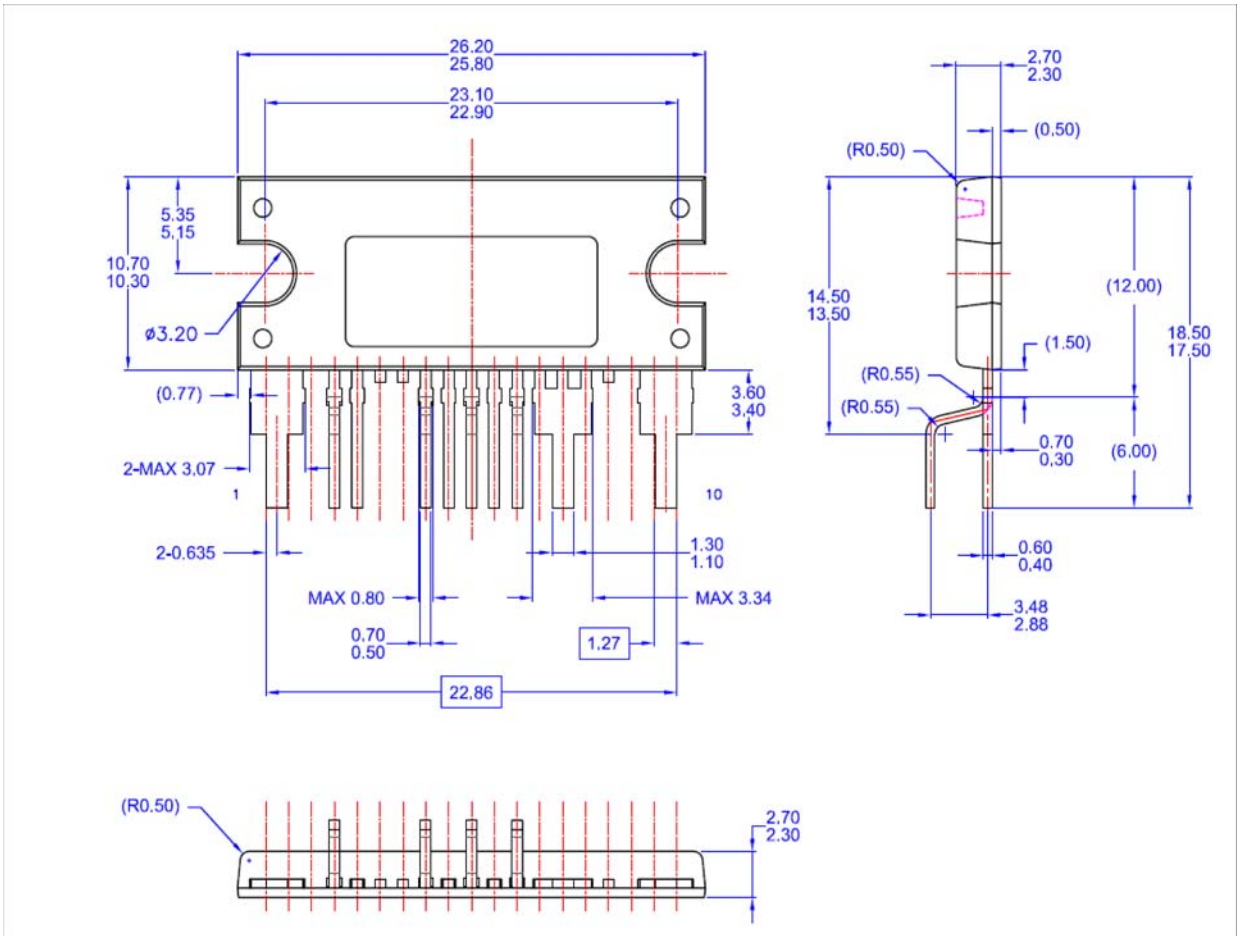


Note:

Built in bootstrap diode includes around 15Ω resistance characteristic.

Figure 8. Built in Bootstrap Diode Characteristics

Detailed Package Outline Drawings



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