FAIRCHILD SEMICONDUCTOR®

April 2013

FDD5N50U

N-Channel UniFET™ Ultra FRFET™ MOSFET

500 V, 3 A, 2.0 Ω

Features

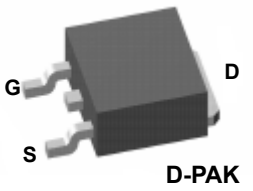
- $R_{DS(on)}$ = 1.65 Ω (Typ.) @ V_{GS} = 10 V, I_D = 1.5 A
- Low gate charge (Typ. 11 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% avalanche tested
- RoHS compliant

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. UniFET™ Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its t_{rr} is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



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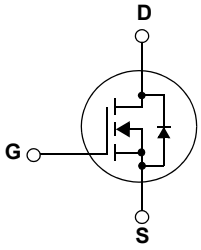


MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			FDD5N50U	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)		3	A
		- Continuous (T_C = 100°C)		1.8	
I_{DM}	Drain Current	- Pulsed	(Note 1)	12	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	275	mJ
I_{AR}	Avalanche Current		(Note 1)	3	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		40	W
		- Derate above 25°C		0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDD5N50U	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5N50U	FDD5N50UTM	D-PAK	380mm	16mm	2500
FDD5N50U	FDD5N50UTM_WS	D-PAK	380mm	16mm	2500
FDD5N50U	FDD5N50UTF	D-PAK	380mm	16mm	2000

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BVDSS	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_J = 25°C	500	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.6	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 400V, T_C = 125°C	-	-	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 1.5A	-	1.65	2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 1.5A	-	4	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	485	650	pF
C_{oss}	Output Capacitance		-	65	90	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400V, I_D = 5A, V_{GS} = 10V (Note 4)	-	11	15	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 5A, R_G = 25Ω (Note 4)	-	14	38	ns
t_r	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	27	64	ns
t_f	Turn-Off Fall Time		-	20	50	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	12	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 3A	-	-	1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 5A, dI_F/dt = 100A/μs	-	36	-	ns
Q_{rr}	Reverse Recovery Charge		-	33	-	nC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: L = 61mH, I_{AS} = 3A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3: I_{SD} ≤ 3A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

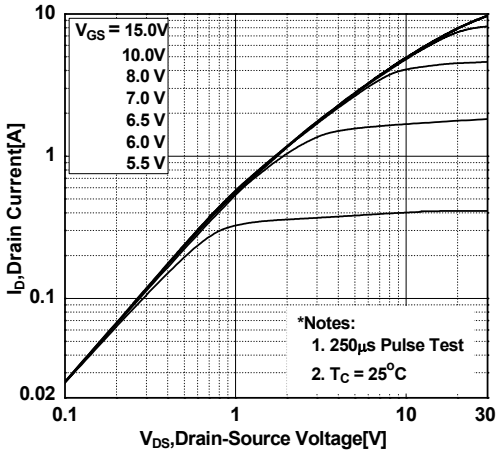


Figure 2. Transfer Characteristics

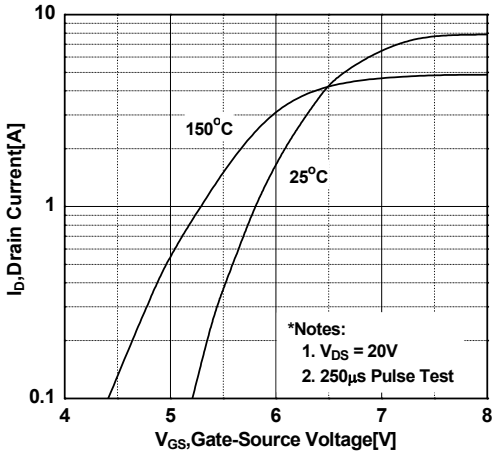


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

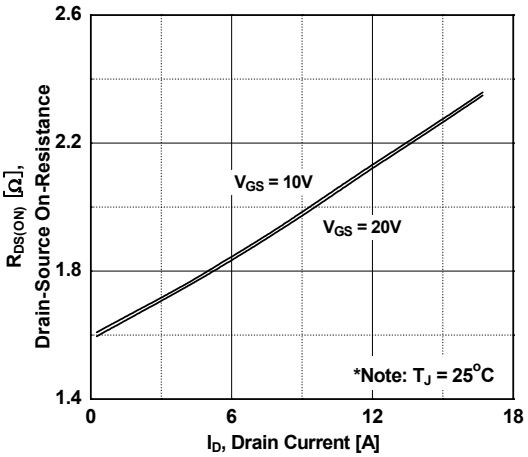


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

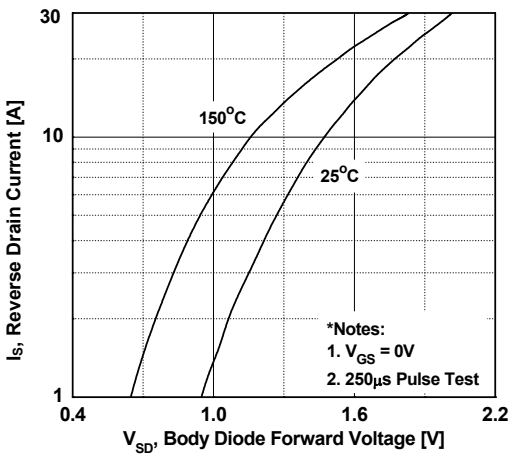


Figure 5. Capacitance Characteristics

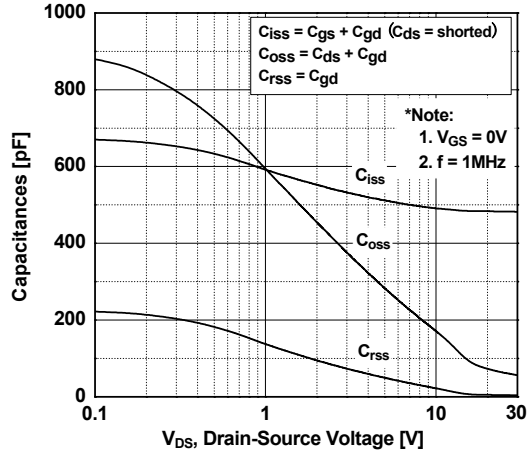
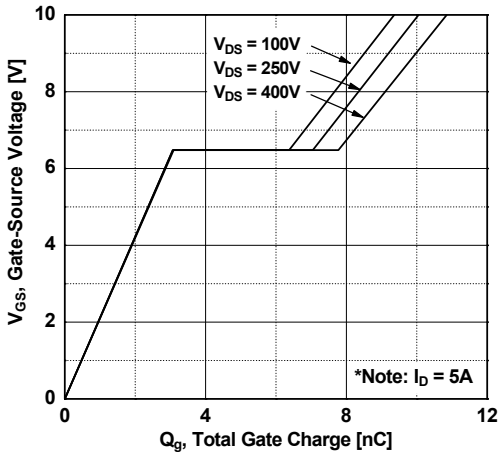


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

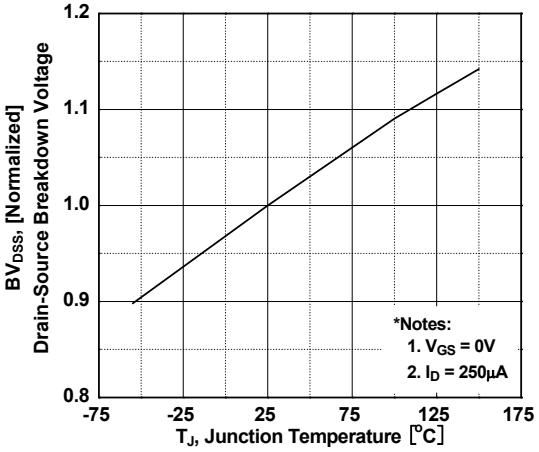


Figure 8. Maximum Safe Operating Area

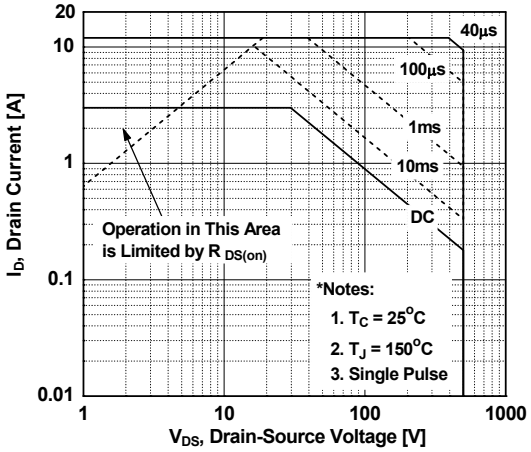


Figure 9. Maximum Drain Current vs. Case Temperature

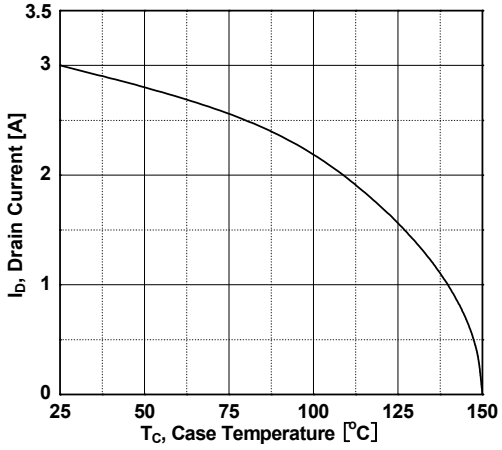
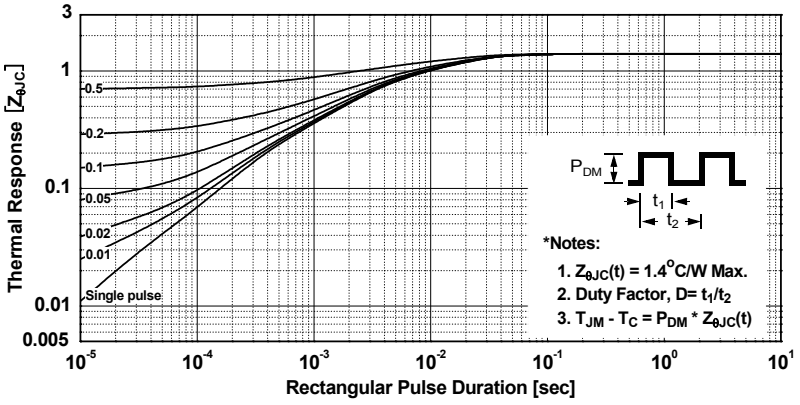
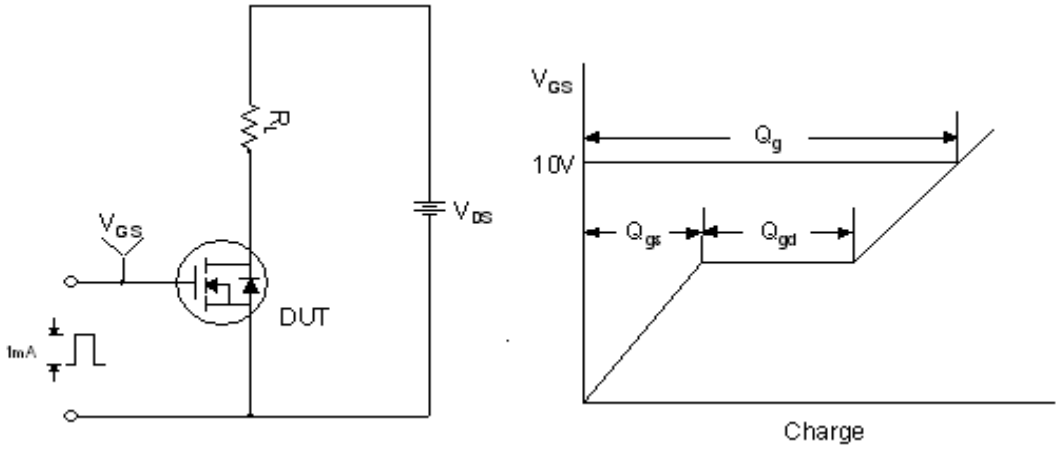


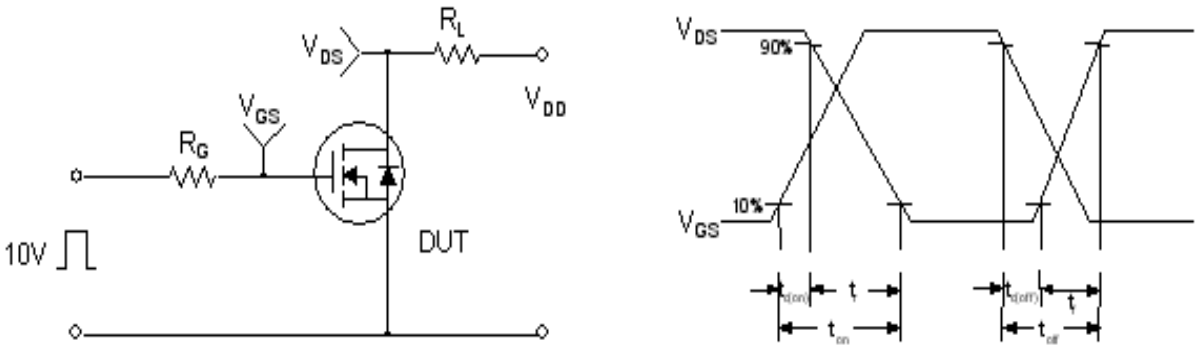
Figure 10. Transient Thermal Response Curve



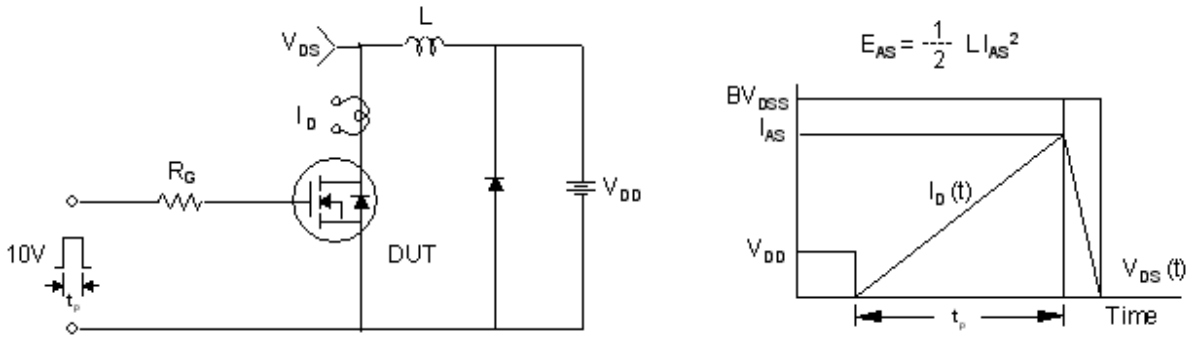
Gate Charge Test Circuit & Waveform



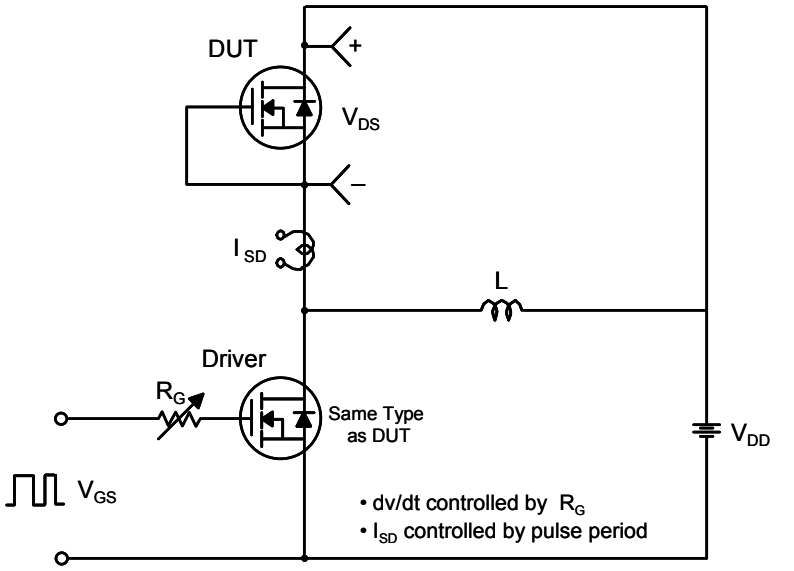
Resistive Switching Test Circuit & Waveforms

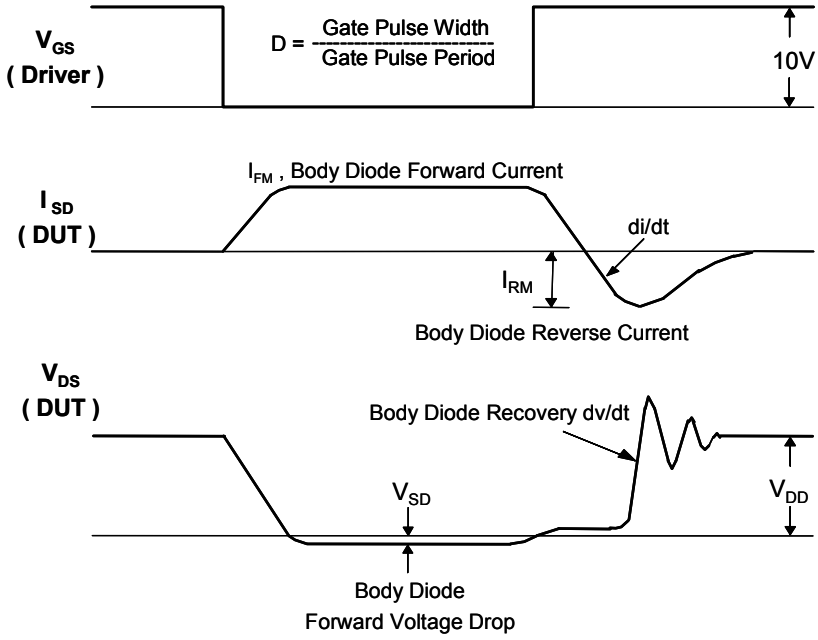


Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

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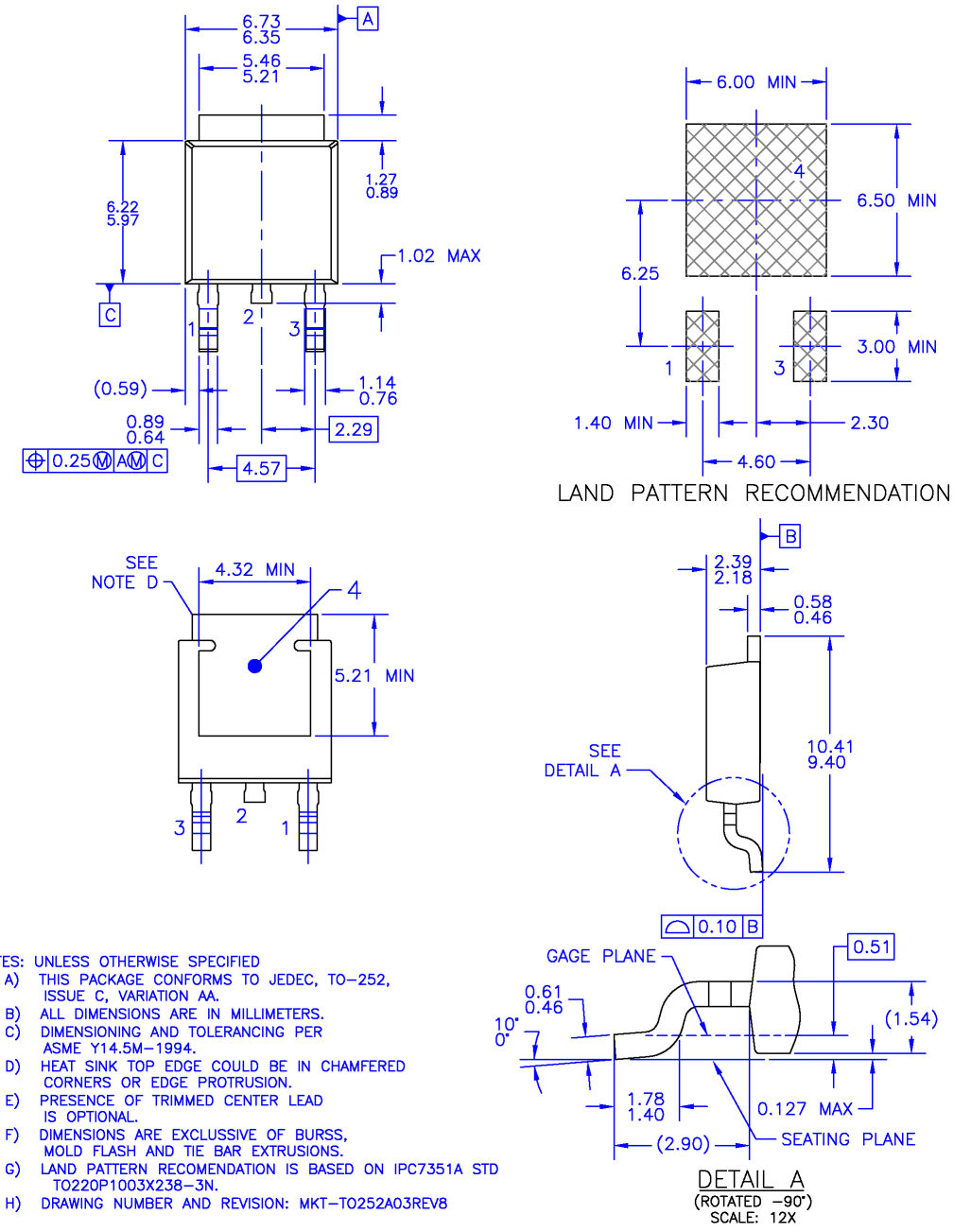

NOTES: UNLESS OTHERWISE SPECIFIED

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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Dimensions in Millimeters

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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