

FIN1017 3.3V LVDS 1-Bit High Speed Differential Driver

General Description

This single driver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTTL signal levels to LVDS levels with a typical differential output swing of 350 mV which provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock or data.

The FIN1017 can be paired with its companion receiver, the FIN1018, or with any other LVDS receiver.

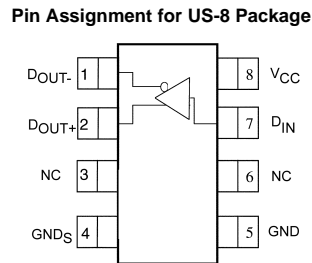
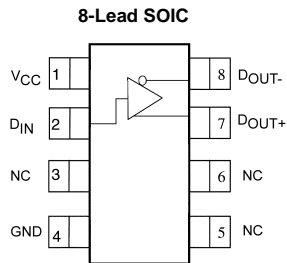
Features

- Greater than 600Mbps data rate
- 3.3V power supply operation
- 0.5ns maximum differential pulse skew
- 1.5ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Flow-through pinout simplifies PCB layout
- 8-Lead SOIC and US8 packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1017M	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TUBE]
FIN1017MX	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TAPE and REEL]
FIN1017K8X	MAB08A	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide [TAPE and REEL]

Connection Diagrams



Note: Ground pins 4 and 5 for optimum operation.

TOP VIEW

Pin Descriptions

Pin Name	Description
D _{IN}	LVTTTL Data Input
D _{OUT+}	Non-inverting Driver Output
D _{OUT-}	Inverting Driver Output
V _{CC}	Power Supply
GND	Ground
NC	No Connect

Function Table

Input	Outputs	
D _{IN}	D _{OUT+}	D _{OUT-}
L	L	H
H	H	L
OPEN	L	H

H = HIGH Logic Level L = LOW Logic Level X = Don't Care

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (D_{IN})	-0.5V to +6V
DC Output Voltage (D_{OUT})	-0.5V to +4.7V
Driver Short Circuit Current (I_{OSD})	Continuous
Storage Temperature Range (T_{STG})	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 6500V
ESD (Bus Pins D_{OUT+}/D_{OUT-} to GND)	≥ 10500V
ESD (Machine Model)	≥ 350V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_{IN})	0 to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{OD}	Output Differential Voltage	$R_L = 100 \Omega$, See Figure 1	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OFF}	Power-Off Output Current	$V_{CC} = 0V$, $V_{OUT} = 0V$ or $3.6V$			±20	μA
I_{OS}	Short Circuit Output Current	$V_{OUT} = 0V$ $V_{OD} = 0V$			-8 ±8	mA
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		GND		0.8	V
I_{IN}	Input Current	$V_{IN} = 0V$ or V_{CC}			±20	μA
$I_{I(OFF)}$	Power-Off Input Current	$V_{CC} = 0V$, $V_{IN} = 0V$ or $3.6V$			±20	μA
V_{IK}	Input Clamp Voltage	$I_{IK} = -18$ mA	-1.5			V
I_{CC}	Power Supply Current	No Load, $V_{IN} = 0V$ or V_{CC} $R_L = 100 \Omega$, $V_{IN} = 0V$ or V_{CC}			8 10	mA
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			6		pF

Note 2: All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 3.3V$.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLHD}	Differential Propagation Delay LOW-to-HIGH	$R_L = 100 \Omega$, $C_L = 10\text{pF}$, See Figure 2 and Figure 3	0.5		1.5	ns
t_{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.5		1.5	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.4		1.0	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.4		1.0	ns
$t_{SK(P)}$	Pulse Skew [$t_{PLH} - t_{PHL}$]				0.5	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 4)				1.0	ns

Note 3: All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 3.3V$.

Note 4: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

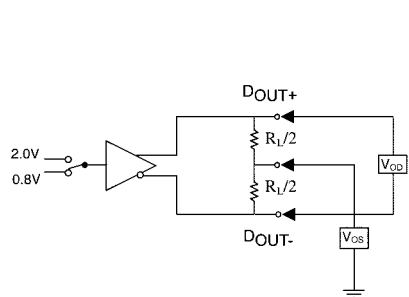
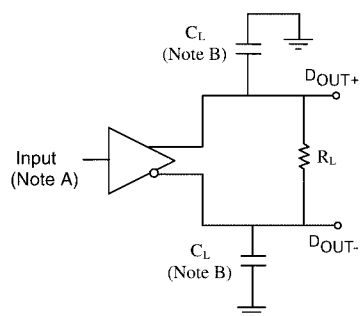


FIGURE 1. Differential Driver DC Test Circuit



Note A: All input pulses have frequency = 10 MHz, t_r or $t_f = 2$ ns
Note B: C_L includes all probe and fixture capacitances

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

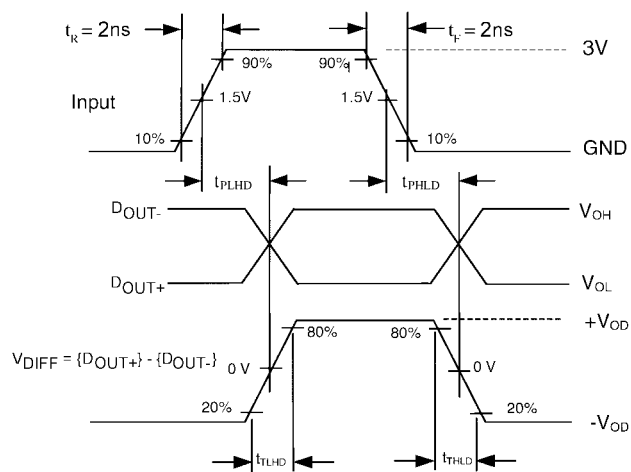


FIGURE 3. AC Waveforms

DC / AC Typical Performance Curves

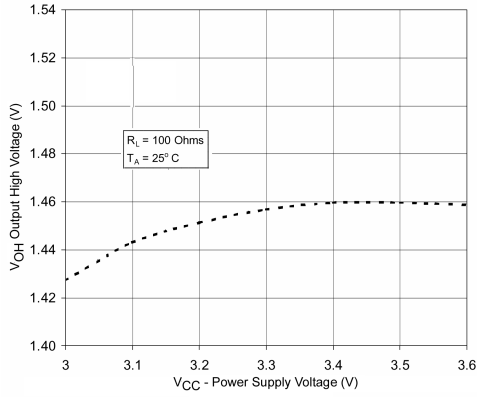


FIGURE 4. Output High Voltage vs. Power Supply Voltage

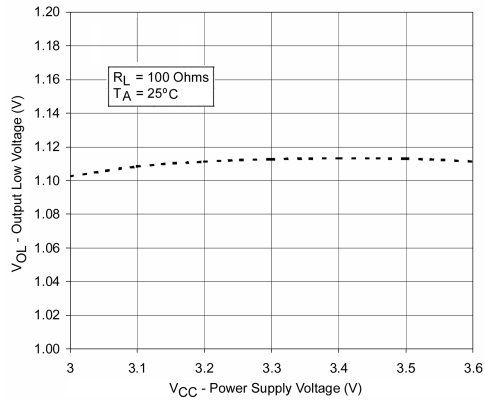


FIGURE 5. Output Low Voltage vs. Power Supply Voltage

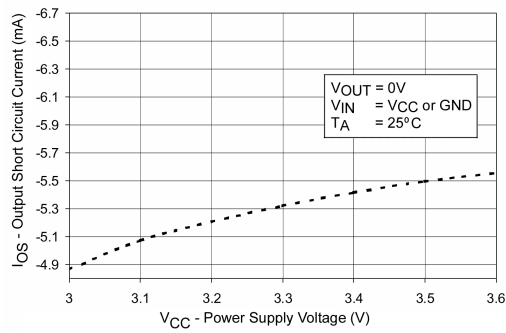


FIGURE 6. Output Short Circuit Current vs. Power Supply Voltage

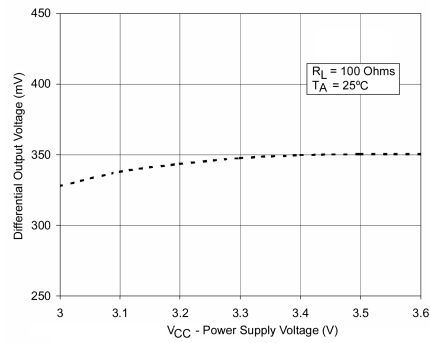


FIGURE 7. Differential Output Voltage vs. Power Supply Voltage

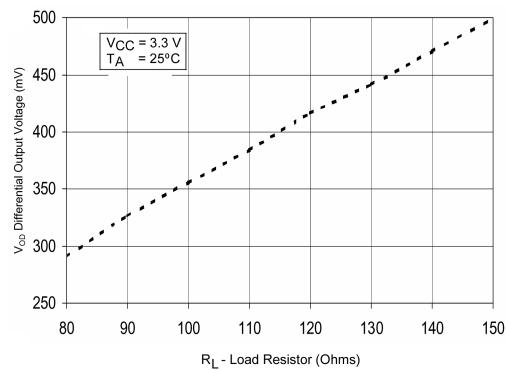


FIGURE 8. Differential Output Voltage vs. Load Resistor

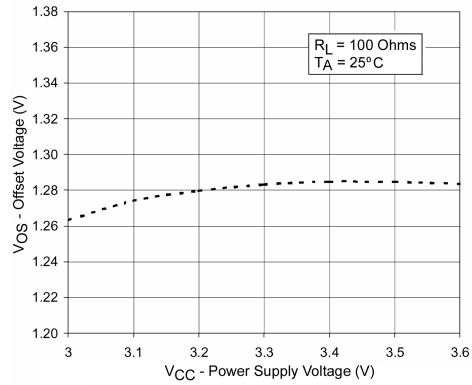


FIGURE 9. Offset Voltage vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

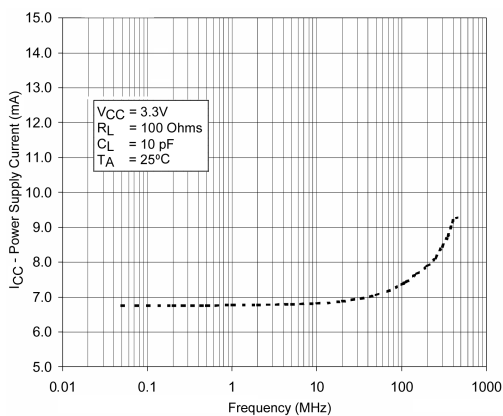


FIGURE 10. Power Supply Current vs. Frequency

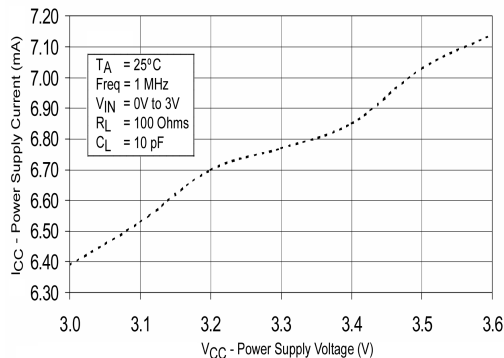


FIGURE 11. Power Supply Current vs. Power Supply Voltage

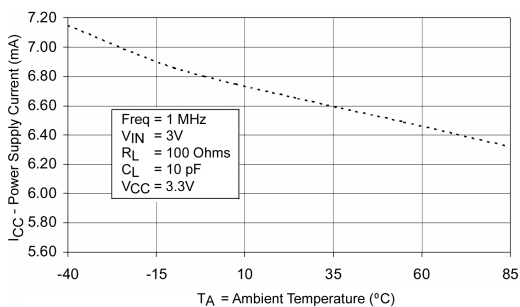


FIGURE 12. Power Supply Current vs. Ambient Temperature

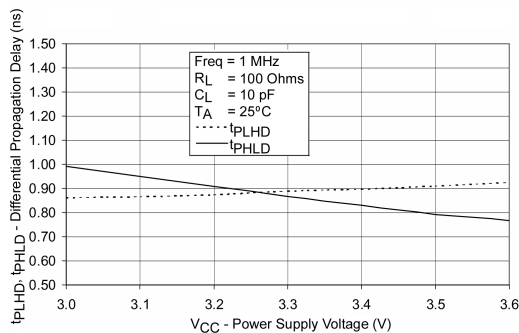


FIGURE 13. Differential Propagation Delay vs. Power Supply

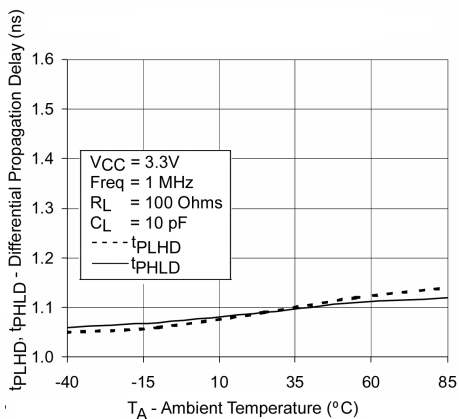


FIGURE 14. Differential Propagation Delay vs. Ambient Temperature

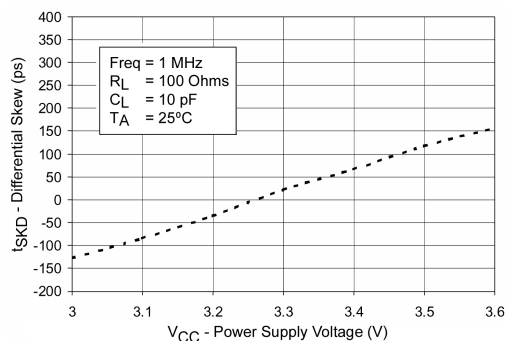


FIGURE 15. Differential Pulse Skew ($t_{PLH} - t_{PHL}$) vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

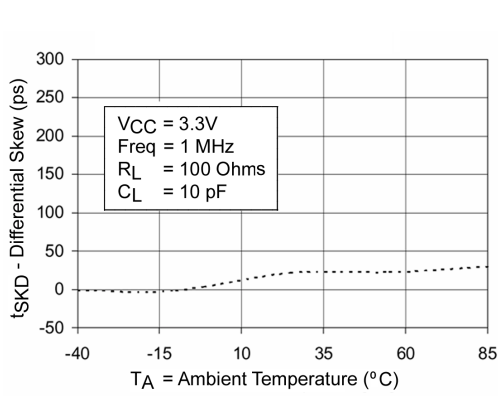


FIGURE 16. Differential Pulse Skew ($t_{PLH} - t_{PHL}$) vs. Ambient Temperature

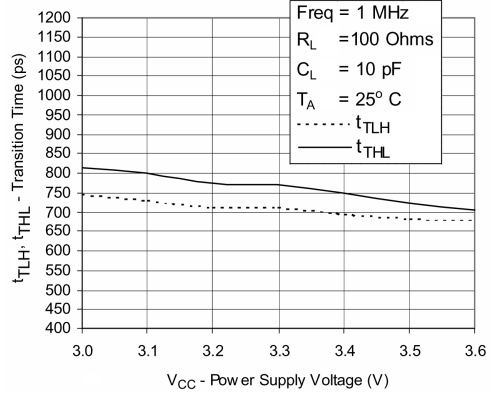


FIGURE 17. Transition Time vs. Power Supply Voltage

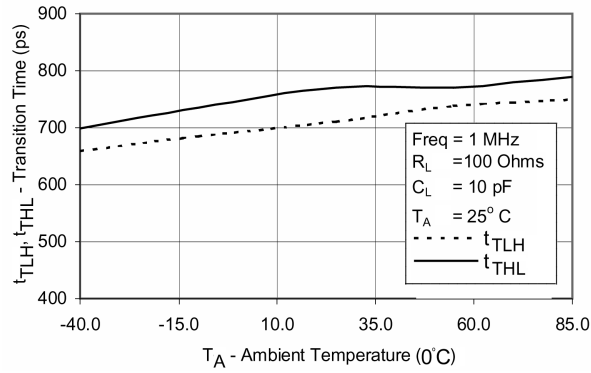
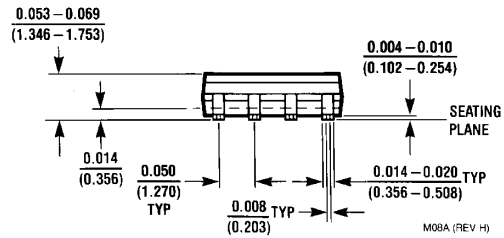
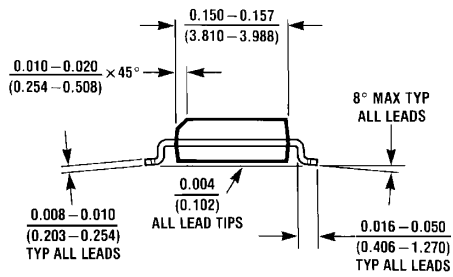
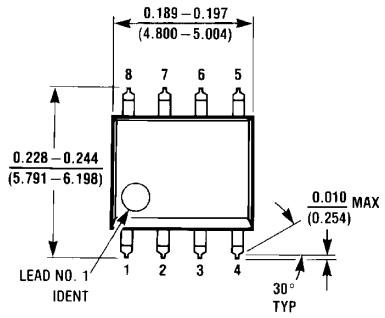


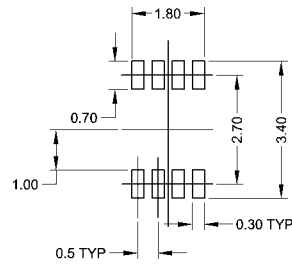
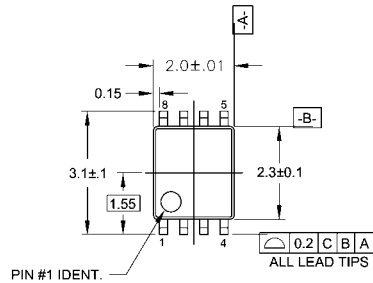
FIGURE 18. Transition Time vs. Ambient Temperature

Physical Dimensions inches (millimeters) unless otherwise noted

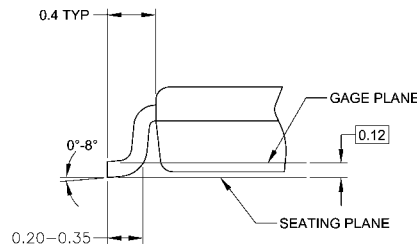
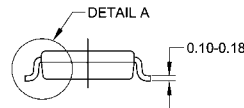
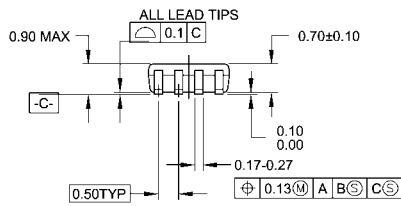


8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A**

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