TM

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SEMICONDUCTOR TM

December 2000

$QFET^{TM}$

TM

FQB10N20L / FQI10N20L

200V LOGIC N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, and motor control.

Features

- 10A, 200V, $R_{DS(on)} = 0.36\Omega$ @ $V_{GS} = 10$ V
- Low gate charge (typical 13 nC)
- Low Crss (typical 14 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirement allowing direct operation from logic drivers

D

G   S

D²-PAK
FQB Series

G   D   S

I²-PAK
FQI Series

D

G

S
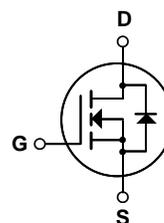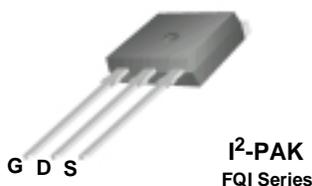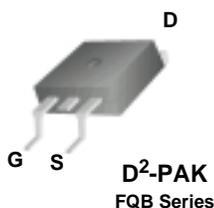
Absolute Maximum Ratings $T_C = 25°C$ unless otherwise noted

Symbol	Parameter			FQB10N20L / FQI10N20L	Units
V_{DSS}	Drain-Source Voltage			200	V
I_D	Drain Current	- Continuous ($T_C = 25°C$)		10	A
		- Continuous ($T_C = 100°C$)		6.3	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	40	A
V_{GSS}	Gate-Source Voltage			± 20	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	180	mJ
I_{AR}	Avalanche Current		(Note 1)	10	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	8.7	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25°C$) *			3.13	W
	Power Dissipation ($T_C = 25°C$)			87	W
	- Derate above 25°C			0.7	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.44	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

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Rev. A2, December 2000

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.18	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 160$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 5.0$ A	--	0.29	0.36	Ω
		$V_{GS} = 5$ V, $I_D = 5.0$ A (Note 4)		0.3	0.38	
g_{FS}	Forward Transconductance	$V_{DS} = 30$ V, $I_D = 5.0$ A	--	10.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	640	830	pF
C_{oss}	Output Capacitance		--	95	125	pF
C_{rss}	Reverse Transfer Capacitance		--	14	18	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100$ V, $I_D = 10$ A, $R_G = 25$ Ω	--	13	35	ns
t_r	Turn-On Rise Time		--	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time	(Note 4, 5)	--	50	110	ns
t_f	Turn-Off Fall Time		--	95	200	ns
Q_g	Total Gate Charge	$V_{DS} = 160$ V, $I_D = 10$ A, $V_{GS} = 5$ V	--	13	17	nC
Q_{gs}	Gate-Source Charge		--	2.4	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	6.1	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	10	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	40	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 10$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 10$ A, $dI_F / dt = 100$ A/μs (Note 4)	--	120	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.57	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 2.7mH, $I_{AS} = 10$A, $V_{DD} = 50$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 10$A, di/dt ≤ 300A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics
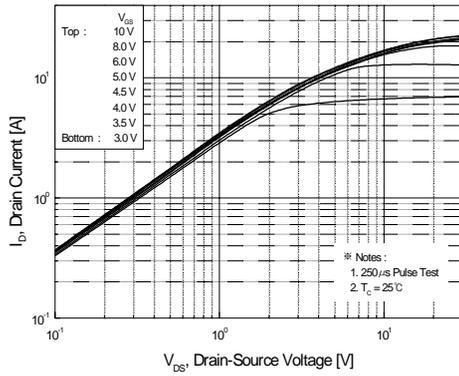
Figure 1. On-Region Characteristics
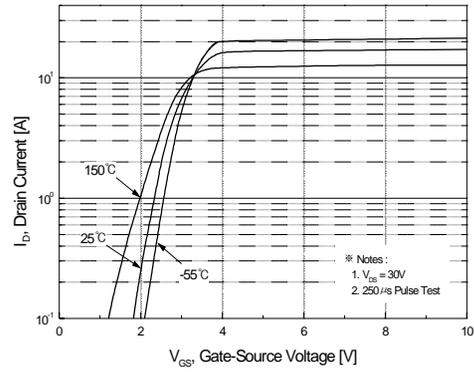
Figure 2. Transfer Characteristics
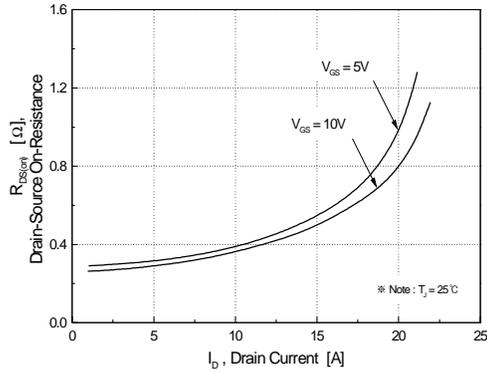
Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
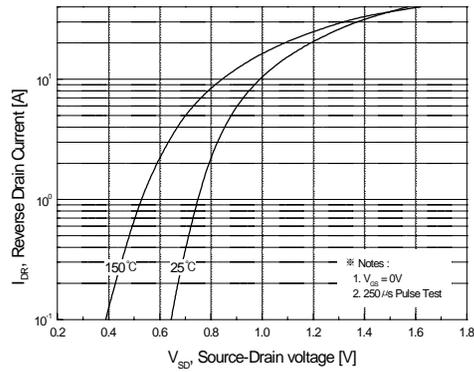
Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
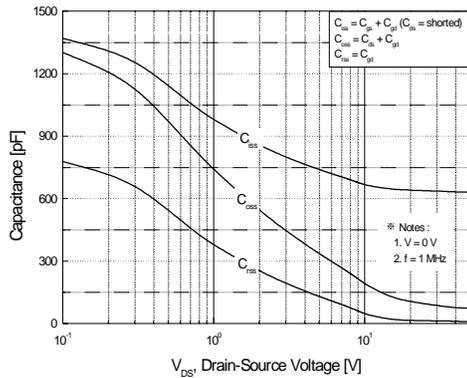
Figure 5. Capacitance Characteristics
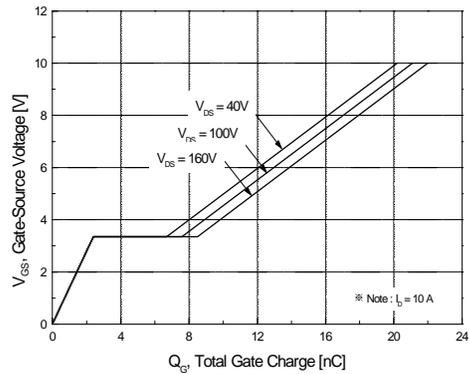
Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)
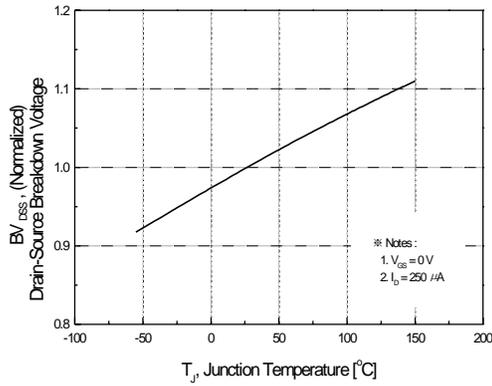
Figure 7. Breakdown Voltage Variation
vs. Temperature
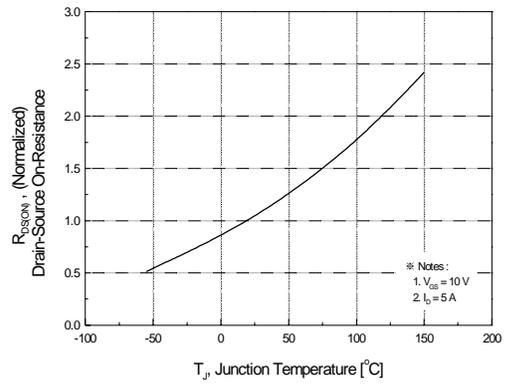
Figure 8. On-Resistance Variation
vs. Temperature
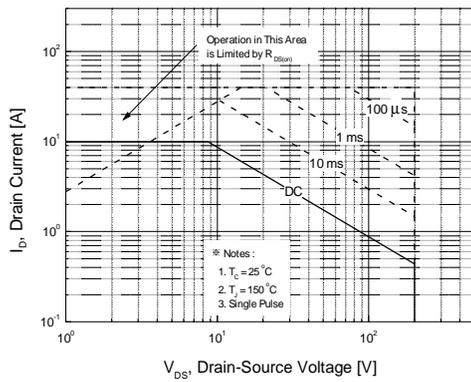
Figure 9. Maximum Safe Operating Area
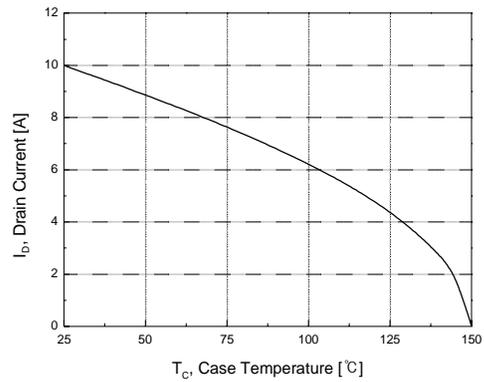
Figure 10. Maximum Drain Current
vs. Case Temperature
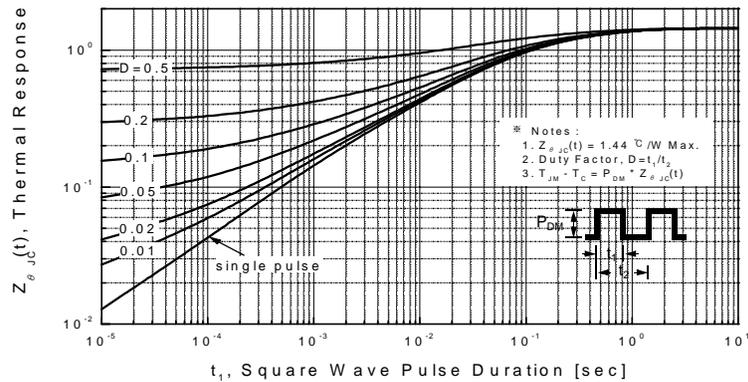
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

Same Type
as DUT

12V 200nF 50KΩ 300nF

V_{GS}

DUT

3mA

V_{DS}

V_{GS}

5V

Q_g

Q_{gs} Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

V_{DS} R_L

V_{DD}

R_G

V_{GS}

5V

DUT

V_{DS}

90%

V_{GS}

10%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
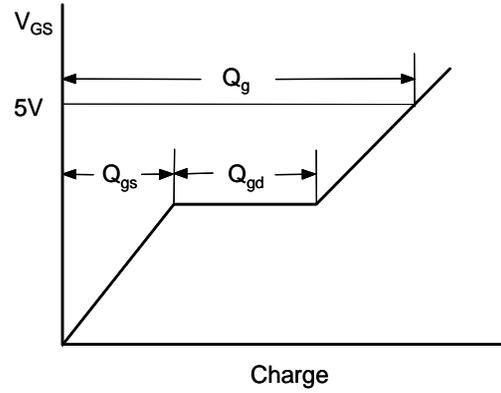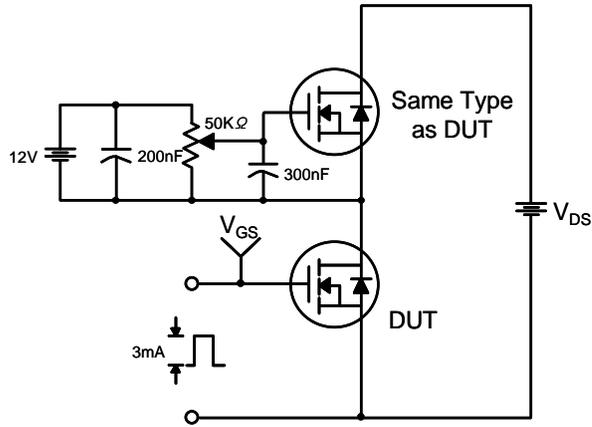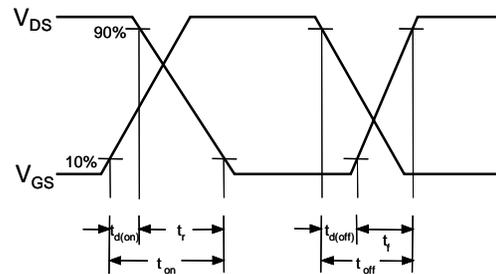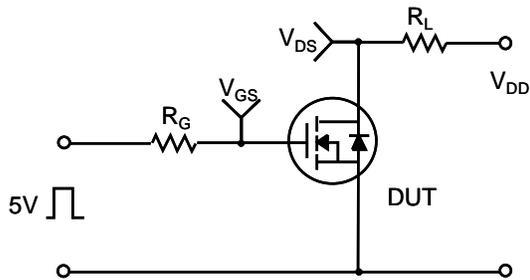
Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS} L

I_D

R_G

V_{DD}

10V

t_p

DUT

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD}

$V_{DS}(t)$

t_p Time
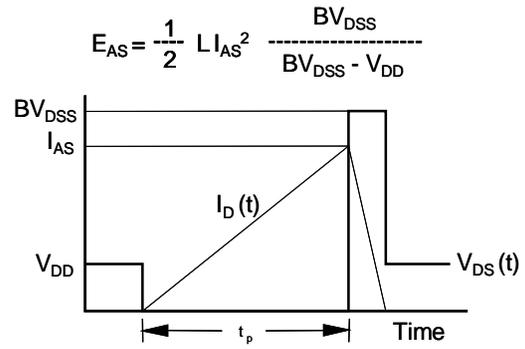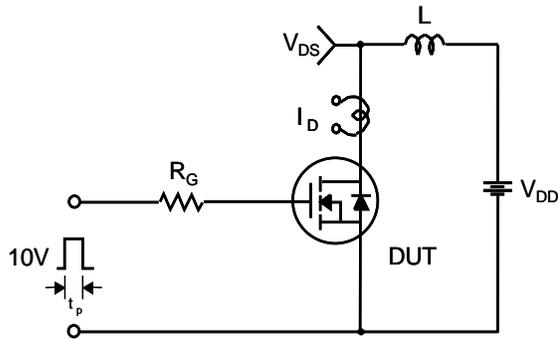
Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{GS}

V_{DD}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$D = \dfrac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

D^{2}PAK

9.90 ±0.20

(0.40)

4.50 ±0.20

1.30 $^{+0.10}_{-0.05}$

1.20 ±0.20

1.40 ±0.20

9.20 ±0.20

15.30 ±0.30

4.90 ±0.20

2.00 ±0.10

0.10 ±0.15

2.40 ±0.20

2.54 ±0.30

(0.75)

0°~3°

0.50 $^{+0.10}_{-0.05}$

1.27 ±0.10

0.80 ±0.10

2.54 TYP

2.54 TYP

10.00 ±0.20

10.00 ±0.20

(8.00)

(4.40)

(1.75)

(2XR0.45)

(7.20)

9.20 ±0.20

15.30 ±0.30

4.90 ±0.20

0.80 ±0.10

Package Dimensions (Continued)

I²PAK

9.90 ±0.20

(0.40)

1.20 ±0.20

9.20 ±0.20

MAX13.40

(1.46)

(0.94)

13.08 ±0.20

MAX 3.00

10.08 ±0.20

(45°)

1.27 ±0.10

1.47 ±0.10

0.80 ±0.10

2.54 TYP

2.54 TYP

4.50 ±0.20

1.30 $^{+0.10}_{-0.05}$

0.50 $^{+0.10}_{-0.05}$

2.40 ±0.20

10.00 ±0.20
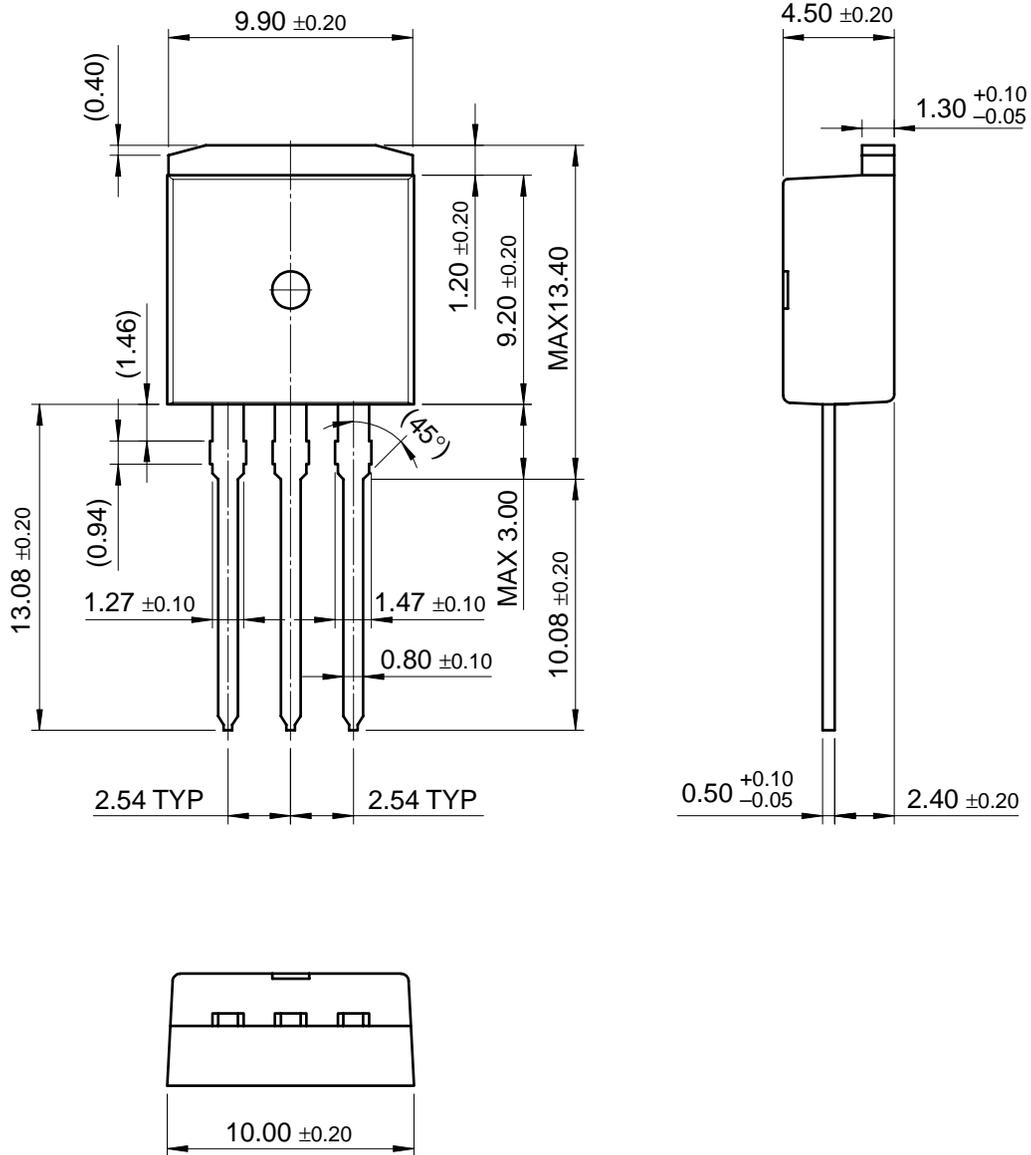
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Product	Product status	Pricing*	Package type	Leads	Packing method
FQB10N20LTM	Full Production	$0.62	TO-263(D2PAK)	2	TAPE REEL

* 1,000 piece Budgetary Pricing

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Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
TO-263(D2PAK)-2	Electrical/Thermal	-55°C to 150°C	9.2	Jul 21, 2000

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Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Packing method
FQI10N20LTU	Full Production	$0.62	TO-262(I2PAK)	3	RAIL

* 1,000 piece Budgetary Pricing

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Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
TO-262(I2PAK)-3	Electrical/Thermal	-55°C to 150°C	9	Jul 21, 2000

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