



# FCH104N60

## N-Channel SuperFET<sup>®</sup> II MOSFET

600 V, 37 A, 104 mΩ

### Features

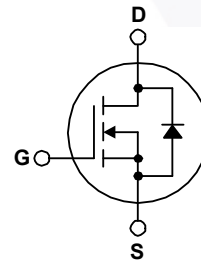
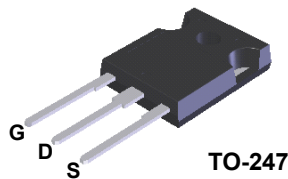
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 96\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 63\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 280\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies

### Description

SuperFET<sup>®</sup> II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH104N60	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC (f > 1 Hz)	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	37
		- Continuous ( $T_C = 100^\circ\text{C}$ )	24
$I_{DM}$	Drain Current	- Pulsed (Note 1)	111
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	809
$I_{AR}$	Avalanche Current	(Note 1)	6.8
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	3.57
dv/dt	MOSFET dv/dt		100
	Peak Diode Recovery dv/dt (Note 3)		20
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	357
		- Derate Above $25^\circ\text{C}$	2.85
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCH104N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH104N60	FCH104N60	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.67	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	1.98	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 18.5\text{ A}$	-	96	104	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 18.5\text{ A}$	-	33	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3130	4165	pF
$C_{oss}$	Output Capacitance		-	75	100	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3.66	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	280	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 18.5\text{ A}, V_{GS} = 10\text{ V}$	-	63	82	nC
$Q_{gs}$	Gate to Source Gate Charge		-	14	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	15	-
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.97	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 18.5\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$	-	26	62	ns
$t_r$	Turn-On Rise Time		-	18	46	ns
$t_{d(off)}$	Turn-Off Delay Time		-	72	154	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	3.3	17

### Drain-Source Diode Characteristics

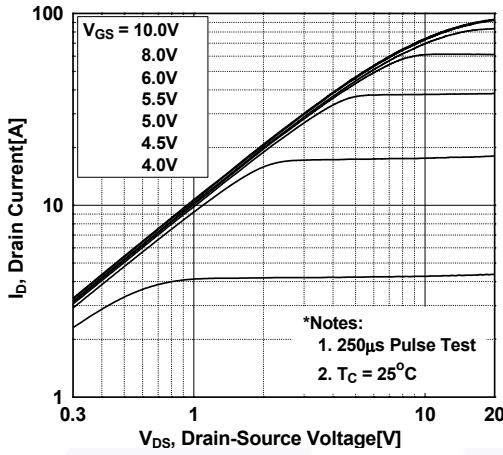
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	37	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	114	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 18.5\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 18.5\text{ A}$	-	414	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	8.8	-	$\mu\text{C}$

#### Notes:

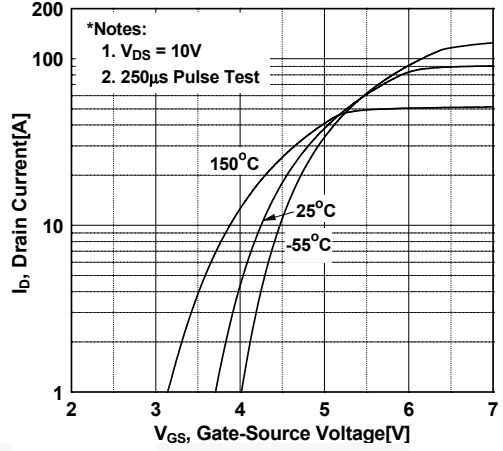
1. Repetitive Rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 6.8\text{ A}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 18.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature.

## Typical Characteristics

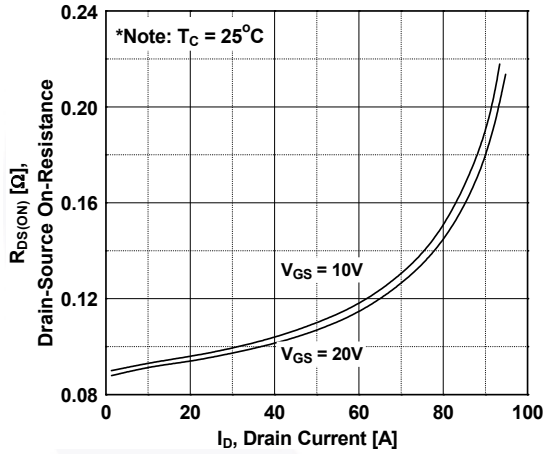
**Figure 1. On-Region Characteristics**



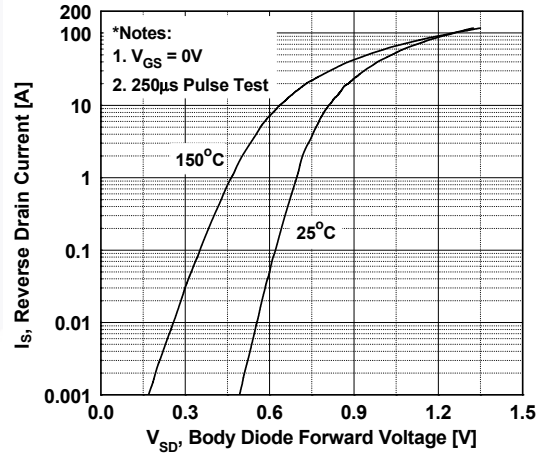
**Figure 2. Transfer Characteristics**



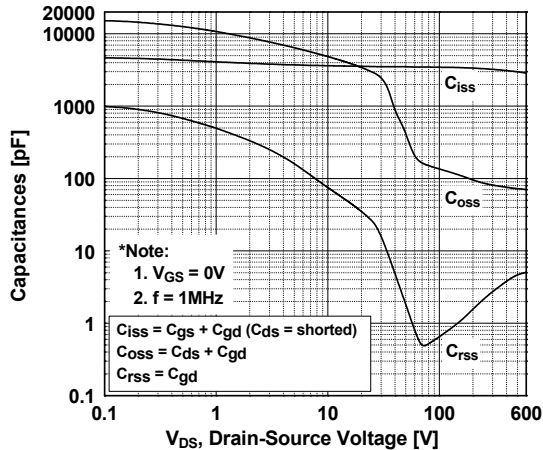
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



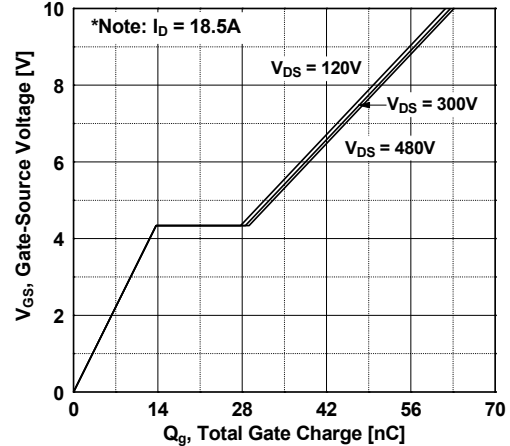
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

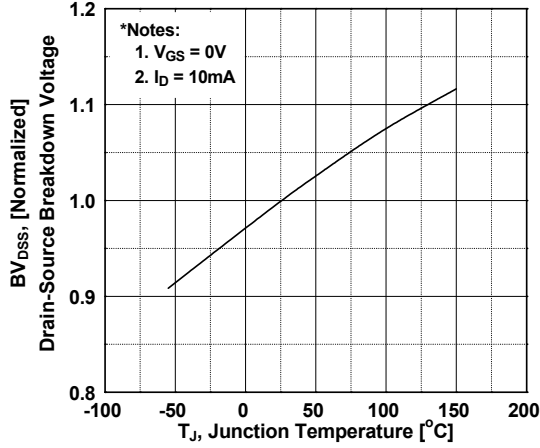


**Figure 6. Gate Charge Characteristics**

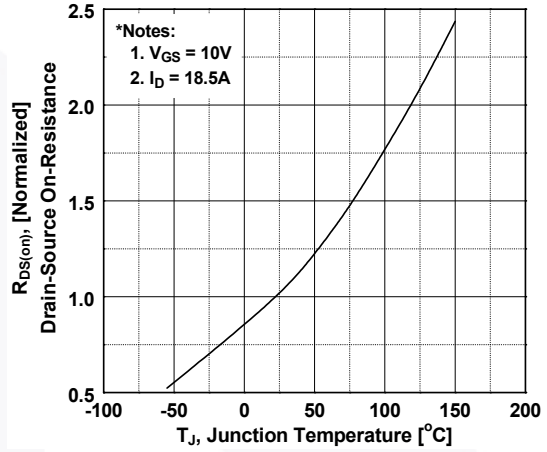


**Typical Characteristics** (Continued)

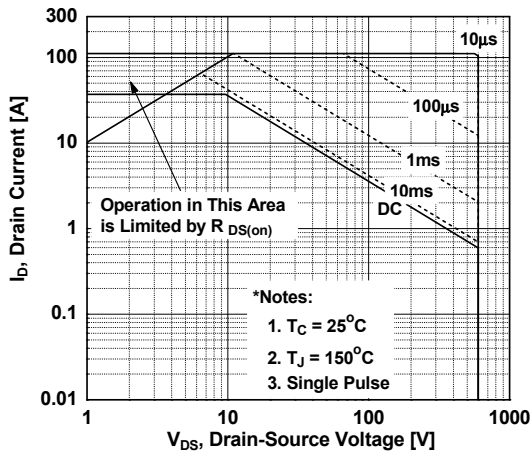
**Figure 7. Breakdown Voltage Variation vs. Temperature**



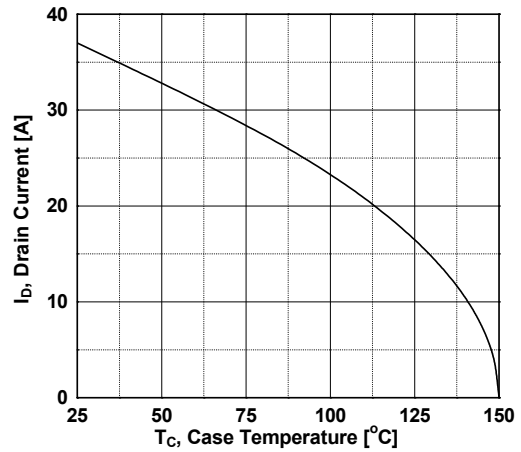
**Figure 8. On-Resistance Variation vs. Temperature**



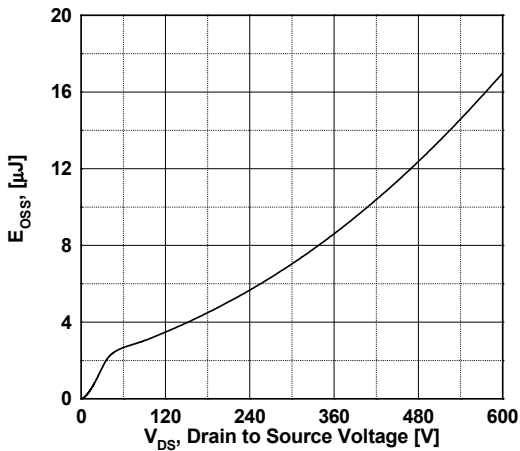
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

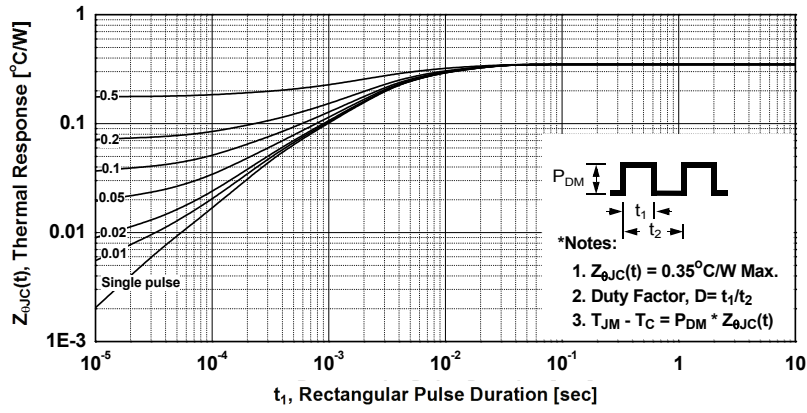


**Figure 11. Eoss vs. Drain to Source Voltage**

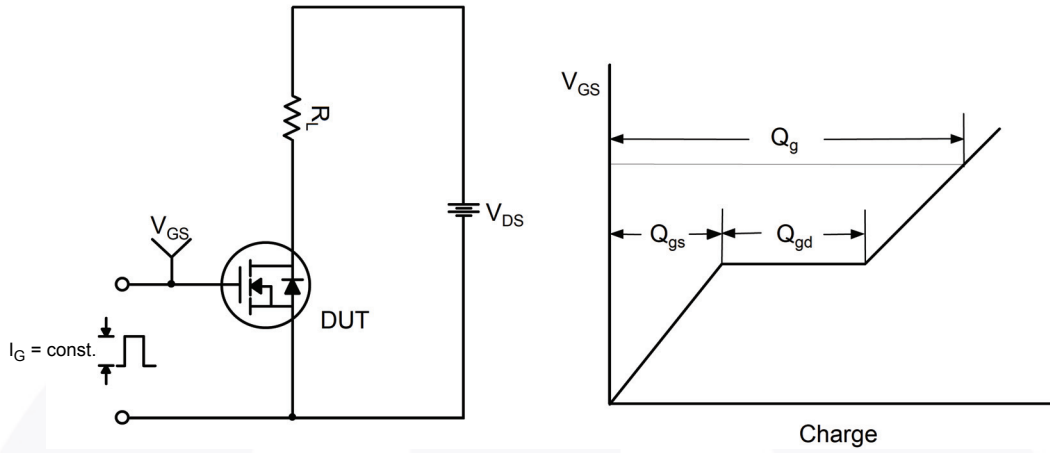


Typical Characteristics (Continued)

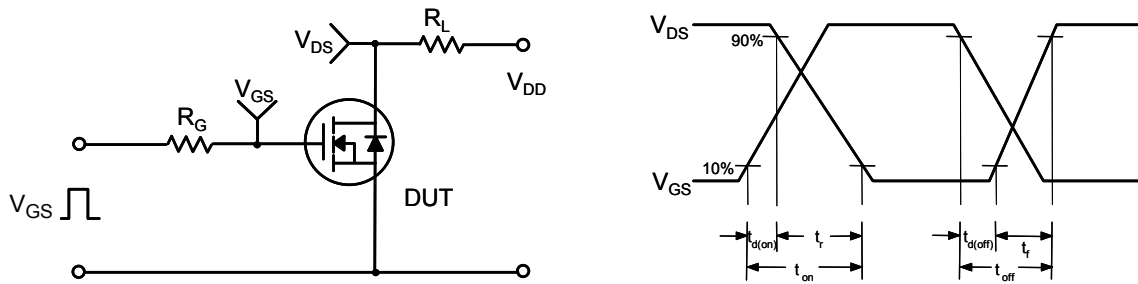
Figure 12. Transient Thermal Response Curve



**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**



**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**

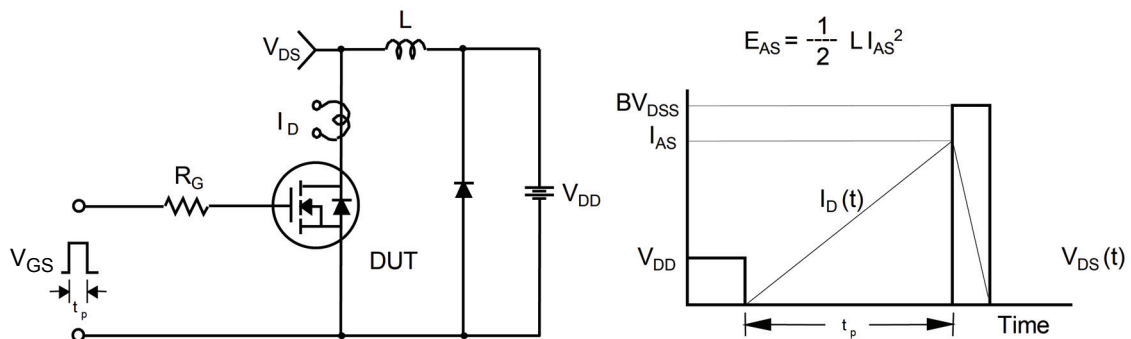
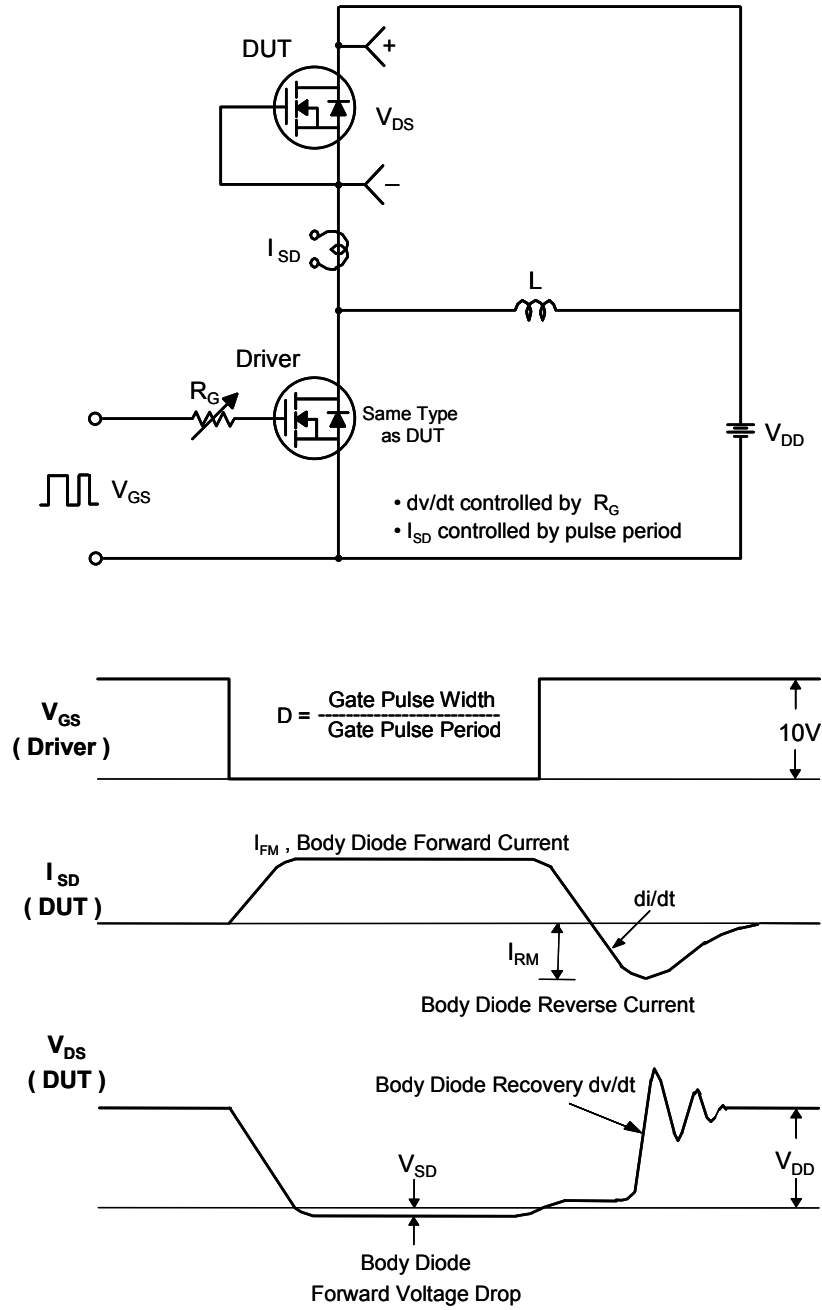
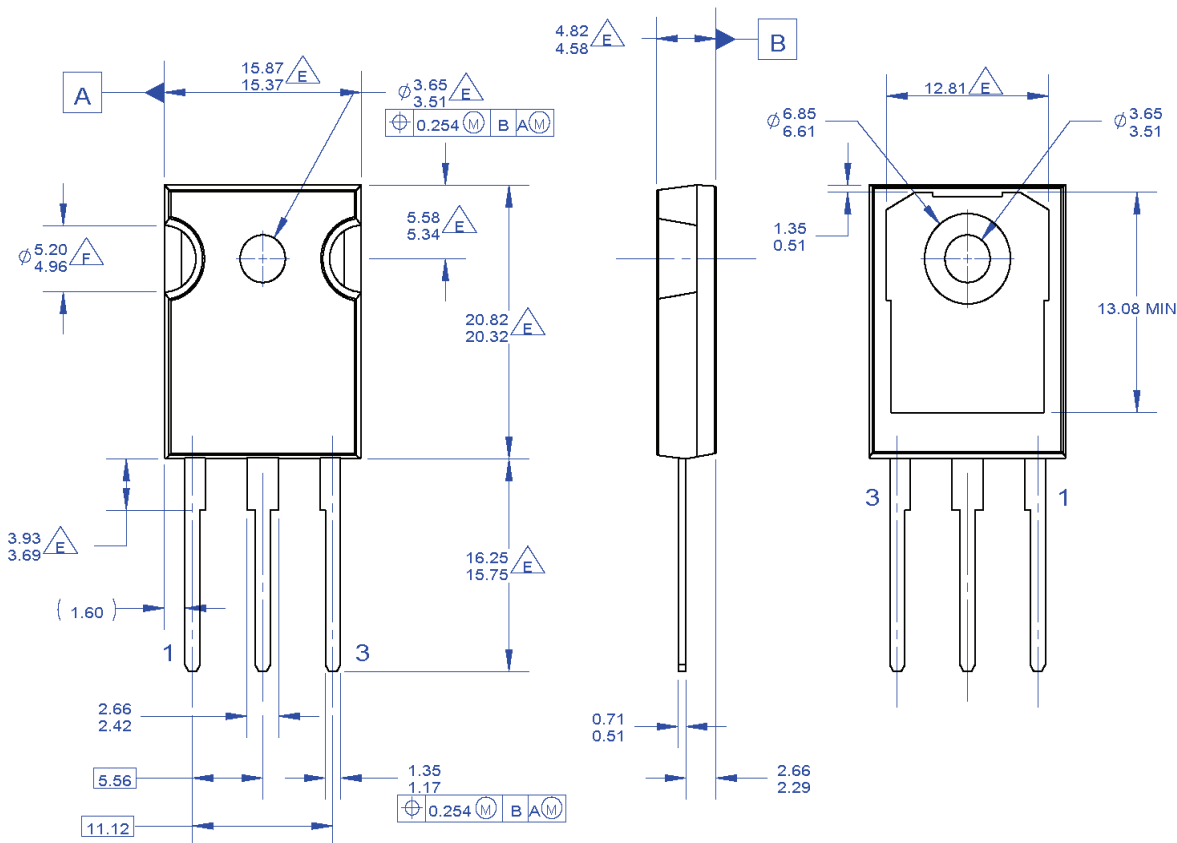


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$  NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 17. TO-247, Molded, 3 Lead, Jeduc Variation AB**

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