

# FQB32N12V2/FQI32N12V2

## 120V N-Channel MOSFET

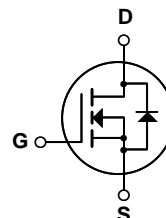
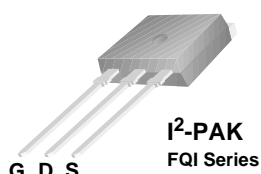
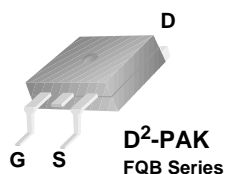
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for DC to DC converters, synchronous rectification, and other applications lowest Rds(on) is required.

### Features

- 32A, 120V,  $R_{DS(on)} = 0.05\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 41 nC)
- Low Crss ( typical 70 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQB32N12V2/FQI32N12V2	Units
V <sub>DSS</sub>	Drain-Source Voltage	120	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	32	A
		23	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	128	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	439	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	32	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	15	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *	3.75	W
	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	150	W
		1	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +175	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	--	1.0	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	120	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.14	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 96\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 16\text{ A}$	--	0.043	0.05	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 16\text{ A}$ (Note 4)	--	25	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1430	1860	pF
$C_{oss}$	Output Capacitance		--	310	405	pF
$C_{riss}$	Reverse Transfer Capacitance		--	70	90	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 60\text{ V}, I_D = 32\text{ A},$ $R_G = 25\ \Omega$	--	16	42	ns	
$t_r$	Turn-On Rise Time		--	190	390	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	114	238	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	158	326	ns
$Q_g$	Total Gate Charge	$V_{DS} = 96\text{ V}, I_D = 32\text{ A},$ $V_{GS} = 10\text{ V}$	--	41	53	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4, 5)	--	8	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	18	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	32	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	128	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 32\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 32\text{ A},$	--	123	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	0.54	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 0.5\text{ mH}, I_{AS} = 32\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 32\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

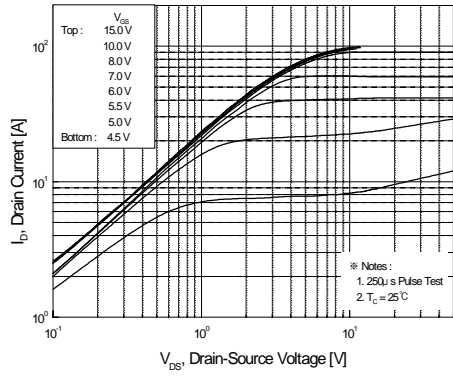


Figure 1. On-Region Characteristics

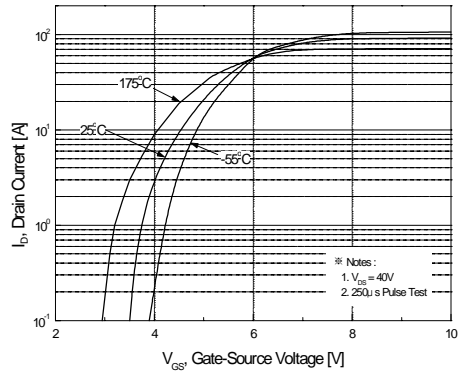


Figure 2. Transfer Characteristics

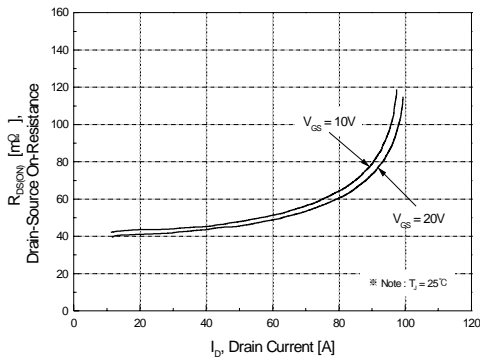


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

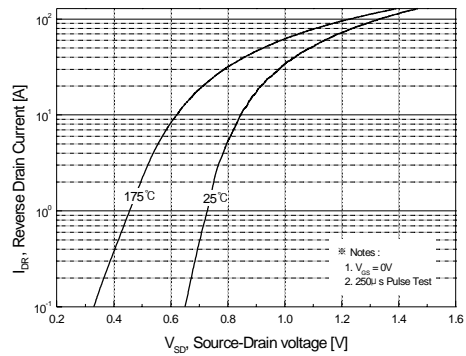


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

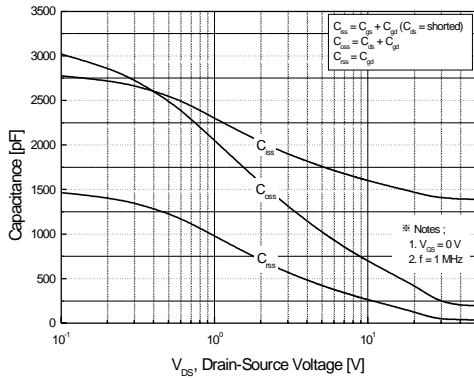


Figure 5. Capacitance Characteristics

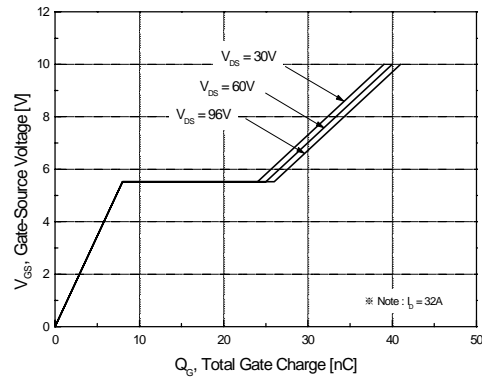
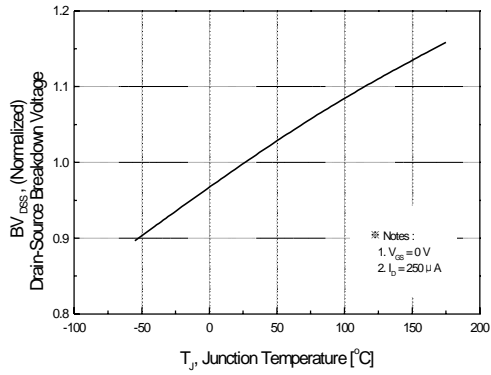
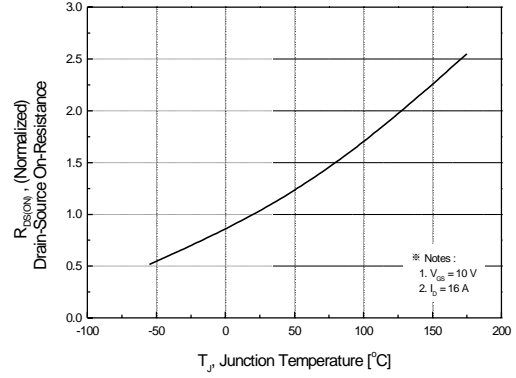


Figure 6. Gate Charge Characteristics

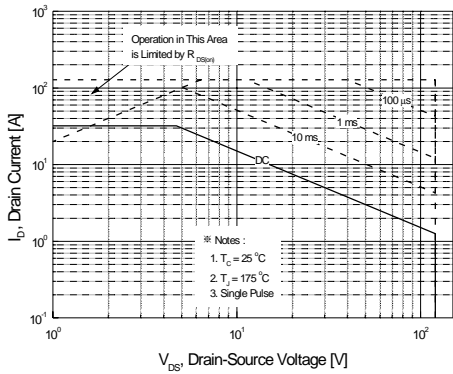
**Typical Characteristics (Continued)**



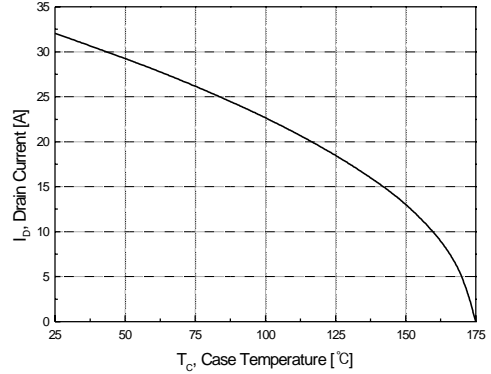
**Figure 7. Breakdown Voltage Variation vs Temperature**



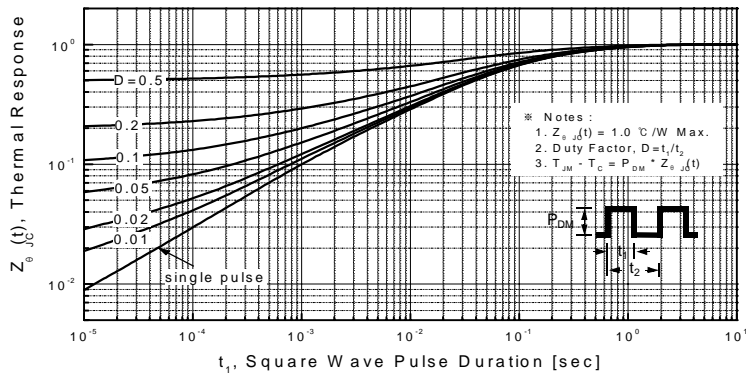
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

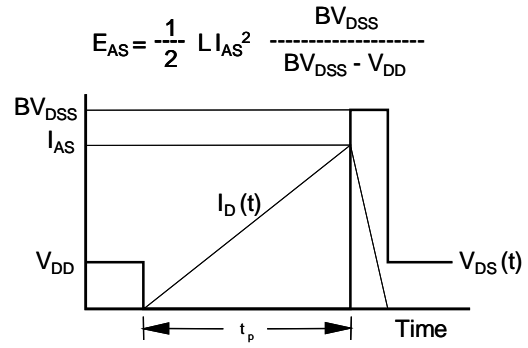
**Gate Charge Test Circuit & Waveform**



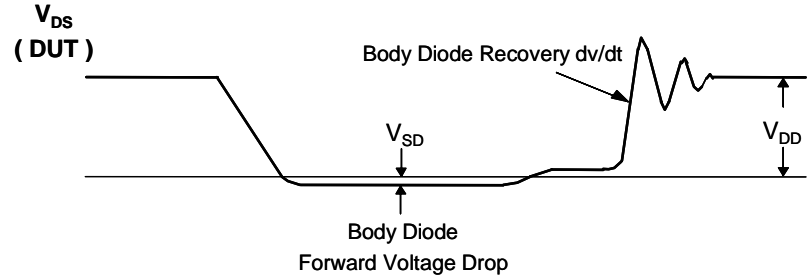
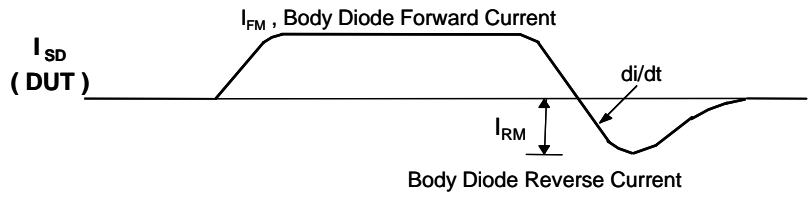
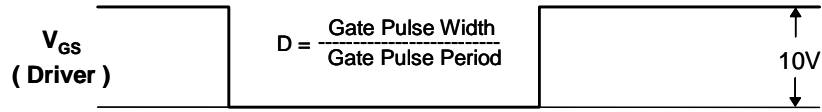
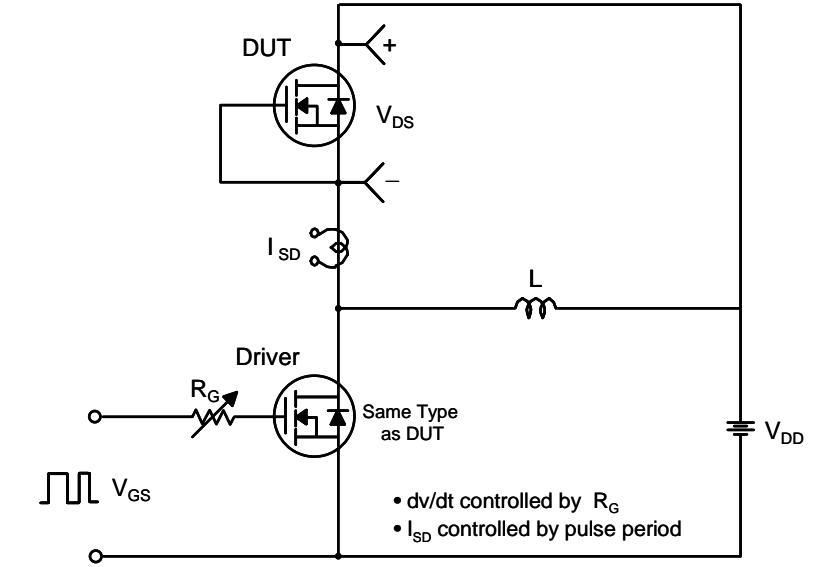
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

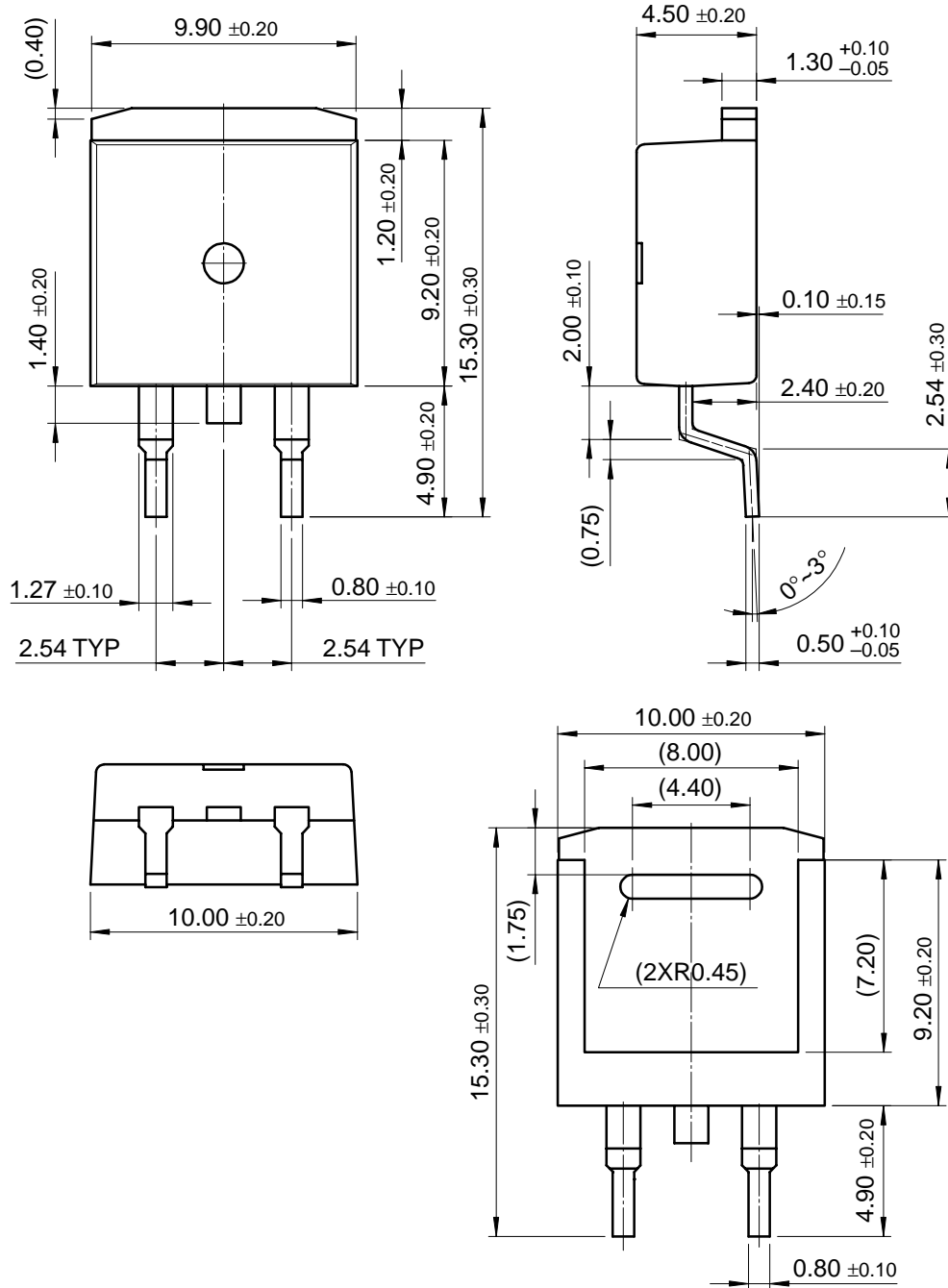


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

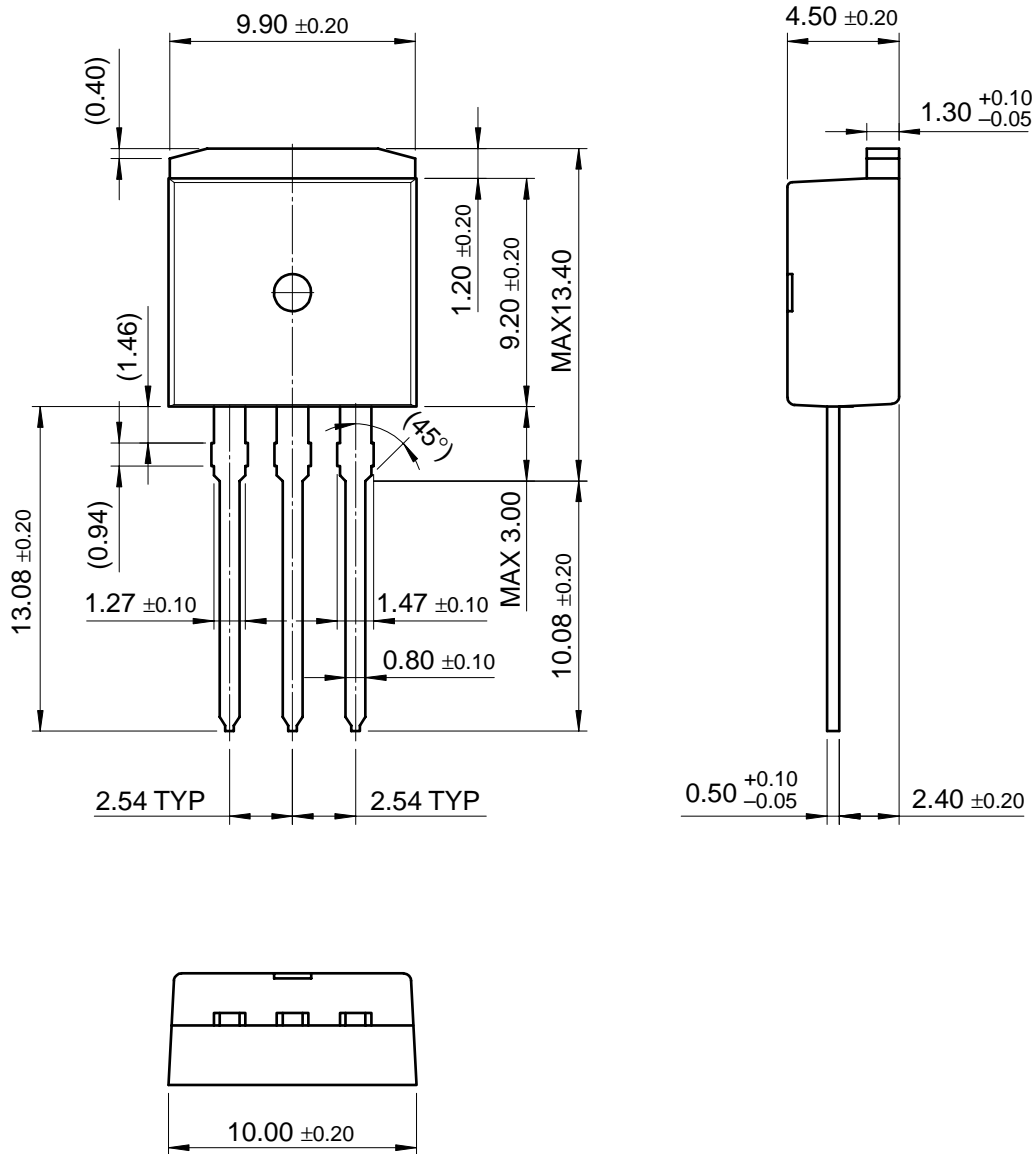
D<sup>2</sup>-PAK



Dimensions in Millimeters

Package Dimensions (Continued)

# I<sup>2</sup>-PAK



Dimensions in Millimeters

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## FQB32N12V2

120V N-Channel Advanced QFET V2 series

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### General description

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Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FQB32N12V2TM	Full Production	 Full Production	\$1.62	<a href="#">TO-263(D2PAK)</a>	2	TAPE REEL	Line 1: \$Y (Fairchild logo) &Z (Asm. Plant Code) &4 (4-Digit Date Code) Line 2: FQB Line 3: 32N12V2

\* Fairchild 1,000 piece Budgetary Pricing

\*\* A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a [Fairchild distributor](#) to obtain samples



Indicates product with Pb-free second-level interconnect. For more information [click here](#).

Package marking information for product FQB32N12V2 is available. [Click here for more information](#).

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Product
<a href="#">FQB32N12V2TM</a>

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