Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN74LS299

8-Bit Shift/Storage Register with 3-State Outputs

The SN74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

GUARANTEED OPERATING RANGES

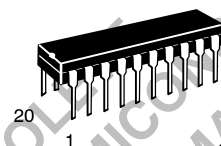
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High Q_0, Q_7			–0.4	mA
I_{OL}	Output Current – Low Q_0, Q_7			8.0	mA
I_{OH}	Output Current – High I/O_0 – $1/O_7$			–2.6	mA
I_{OL}	Output Current – Low I/O_0 – $1/O_7$			24	mA

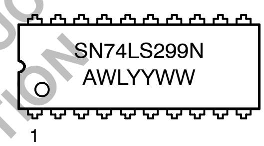
ON Semiconductor

http://onsemi.com

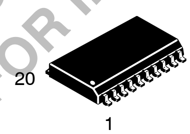
LOW POWER SCHOTTKY

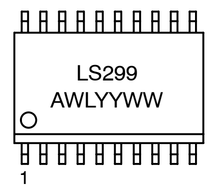
MARKING DIAGRAMS





PDIP–20
N SUFFIX
CASE 738





SOIC–20
DW SUFFIX
CASE 751D

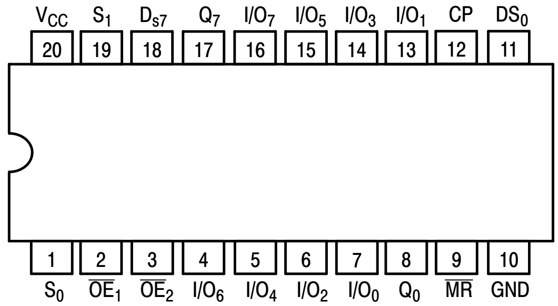
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
SN74LS299N	PDIP–20	1440 Units/Box
SN74LS299DW	SOIC–WIDE	38 Units/Rail
SN74LS299DWR2	SOIC–WIDE	2500/Tape & Reel

July, 2006 – Rev. 9
Publication Order Number:
SN74LS299/D

CONNECTION DIAGRAM DIP (TOP VIEW)

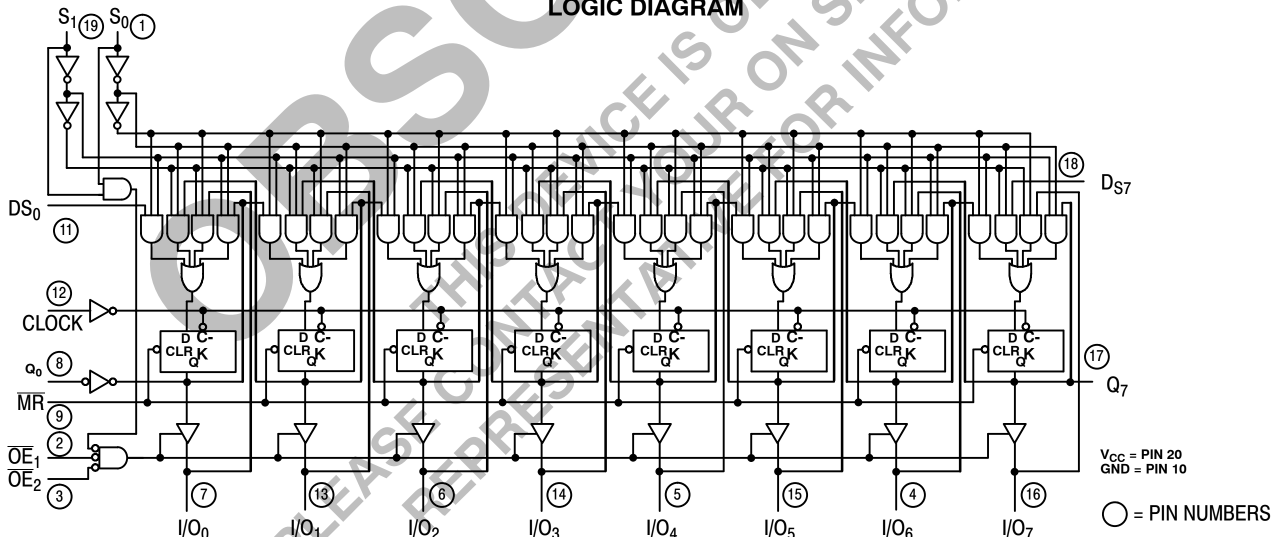


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
CP	Clock Pulse (Active Positive-Going Edge) Input	0.5 U.L.	0.25 U.L.
DS0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	0.5 U.L.	0.25 U.L.
	Parallel Output (3-State)	65 U.L.	15 U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs	10 U.L.	5 U.L.
$\overline{MR}$	Asynchronous Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	0.5 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								RESPONSE
$\overline{MR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L L L	X X H	X X H	H X X	X H X	X X X	X X X	X X X	Asynchronous Reset; $Q_0 = Q_7$ = LOW I/O Voltage Undetermined
L L	L X	X L	L L	L L	X X	X X	X X	Asynchronous Reset; $Q_0 = Q_7$ = LOW I/O Voltage LOW
H H	L L	H H	X L	X L	↑ ↑	D D	X X	Shift Right; D→Q_0; Q_0→Q_1; etc. Shift Right; D→Q_0 & I/O_0; Q_0→O_1 & I/O_1; etc.
H H	H H	L L	X L	X L	↑ ↑	X X	D D	Shift Left; D→Q_7; Q_7→Q_6; etc. Shift Left; D→Q_7 & I/O_7; Q_7→Q_6 & I/O_6; etc.
H	H	H	X	X	↑	X	X	Parallel Load; I/O_n→Q_n
H H	L L	L L	H X	X H	X X	X X	X X	Hold: I/O Voltage undetermined
H	L	L	L	L	X	X	X	Hold: I/O_n = Q_n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage $I/O_0-I/O_7$		2.4	3.1		V	V_{CC} = MIN, I_{OH} = MAX	
V_{OH}	Output HIGH Voltage Q_0, Q_7		2.7	3.4		V	V_{CC} = MIN, I_{OH} = MAX	
V_{OL}	Output LOW Voltage $I/O_0-I/O_7$			0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 24 mA	
V_{OL}	Output LOW Voltage $I/O_0-I/O_7$				0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
					0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH $I/O_0-I/O_7$				40	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW $I/O_0-I/O_7$				−400	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	Others			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		S_0, S_1, $I/O_0-I/O_7$			40	μA		
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		S_0, S_1			0.2	mA		
		$I/O_0-I/O_7$			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	Others			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		S_0, S_1			−0.8	mA		
I_{OS}	Short Circuit Current (Note 1)	Q_0, Q_7	−20		−100	mA	V_{CC} = MAX	
		$I/O_0-I/O_7$	−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				53	mA	V_{CC} = MAX	

1. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	35		MHz	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_0 or Q_7		26 22	39 33	ns	C_L = 15 pF
t_{PHL}	Propagation Delay, Clear to Q_0 or Q_7		27	40	ns	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to $I/O_0-I/O_7$		26 17	39 25	ns	C_L = 45 pF, R_L = 667 Ω
t_{PHL}	Propagation Delay, Clear to $I/O_0-I/O_7$		26	40	ns	C_L = 45 pF, R_L = 667 Ω
t_{PZH} t_{PZL}	Output Enable Time		13 19	21 30	ns	C_L = 45 pF, R_L = 667 Ω
t_{PHZ} t_{PLZ}	Output Disable Time		10 10	15 15	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Pulse Width HIGH	25			ns	V_{CC} = 5.0 V
t_W	Clock Pulse Width LOW	13			ns	V_{CC} = 5.0 V
t_W	Clear Pulse Width LOW	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	20			ns	V_{CC} = 5.0 V
t_s	Select Setup Time	35			ns	V_{CC} = 5.0 V
t_h	Data Hold Time	0			ns	V_{CC} = 5.0 V
t_h	Select Hold Time	10			ns	V_{CC} = 5.0 V
t_{rec}	Recovery Time	20			ns	V_{CC} = 5.0 V

3-STATE WAVEFORMS

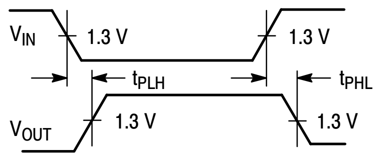


Figure 1.

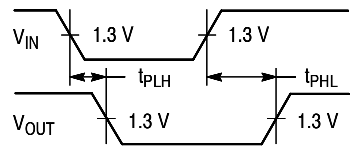


Figure 2.

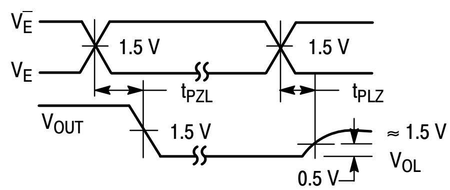


Figure 3.

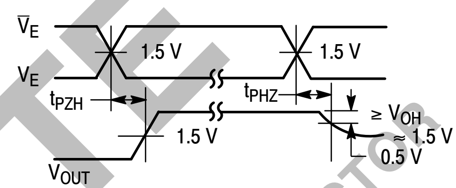
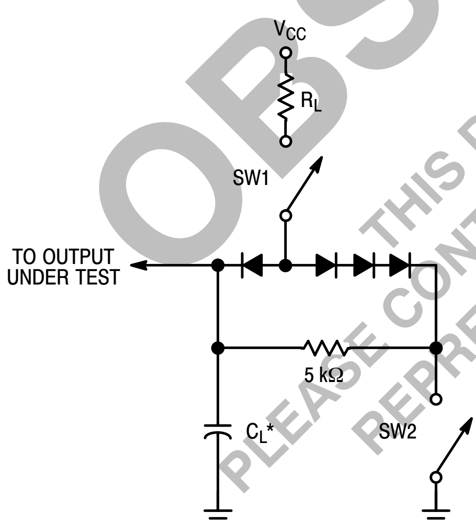


Figure 4.

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

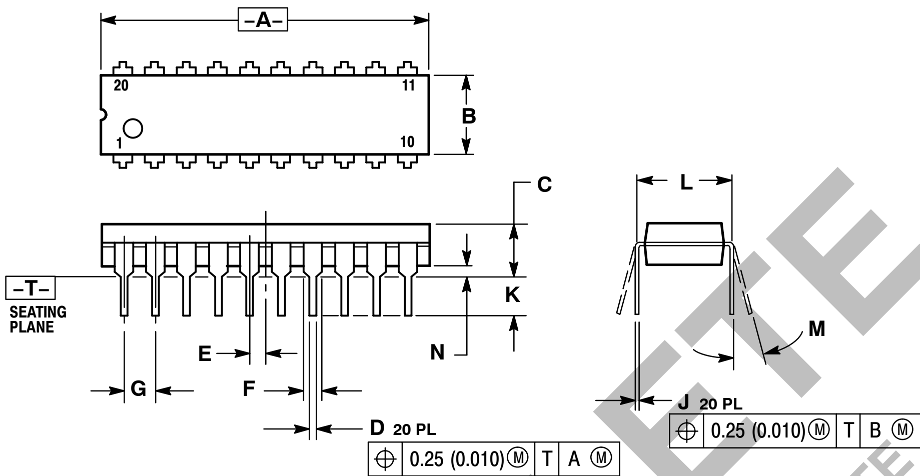
SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 5.

PACKAGE DIMENSIONS

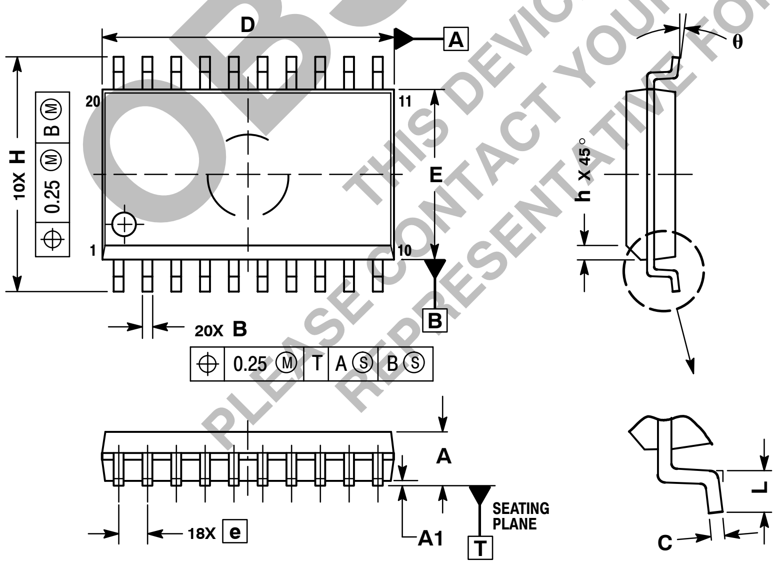
N SUFFIX
PLASTIC PACKAGE
CASE 738−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D−05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative