FAIRCHILD SEMICONDUCTOR®

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FAN53523 — Digitally-Programmable 3MHz, USB-Compliant Power Management Subsystem

Features

- Programmable USB-Compliant Input Current Limit
- 1A Output System Buck Regulator
- System Regulator has Priority Over RF Power
- 7V V_{BUS} Standoff
- 3MHz Fixed-Frequency Operation
- Voltage Limiting for Bulk Capacitors
- Reverse Blocking when V_{BUS} is Below Bulk Cap. Voltage
- PFM Mode for High Light-Load Efficiency
- Output Discharge Function when Disabled
- Low Ripple Light-Load PFM Mode
- 95µA Typical Quiescent Current in PFM Mode
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- Low-Power Suspend and Test Modes
- Host Enable and Interrupt Functions
- 16-Bump, 0.4mm Pitch, WLCSP

Applications

- USB Data Cards
- USB-to-Battery Power Replacement

Description

The FAN53523 is a step-down switching voltage regulator that delivers an adjustable output from a 3.7V to 5.5V USB input voltage. The IC includes a programmable input current-limit circuit to prevent overloading the USB source (V_{BUS}). The IC also features a voltage and current limiting input switch to charge bulk capacitors for an RF Power Amplifier (RFPA) power supply. The voltage limit is programmable in 140mV steps to allow optimal derating. The total input current is limited by an external sense resistor. The buck regulator is given priority when drawing power from V_{BUS}.

The buck regulator features a proprietary architecture with synchronous rectification and is capable of delivering 1A at over 90% efficiency, while maintaining a very high efficiency of over 80% at load currents as low as 2mA. The regulator is digitally programmable to conserve power, but still provides adequate power to the RFPA that may be attached through the current-limit switch at the buck regulator output. The regulator operates at a nominal fixed frequency of 3MHz, which reduces the value of the external components to as low as 1µH and as low as 10µF for the output capacitor. Additional output capacitance can be added to improve regulation during load transients without affecting stability. Inductance up to 1.2µH may be used with additional output capacitance.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate the device in Power-Save Mode with a typical quiescent current of 95µA. Even with such a low quiescent current, the IC exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 3MHz. In Shutdown Mode, supply current drops below 1µA, reducing power consumption. PFM Mode can be disabled if constant frequency is desired.

The VBUS input current limit (I_{BUS}) is digitally programmable. Large capacitors can be used to store energy for high-current transient loads, such as GSM pulses at the output of the VBUS current limit switch.

The IC includes diagnostics that alert the host processor of changes in bulk capacitor charge condition and buck status.

The FAN53523 is available in 16-bump, 0.4mm pitch WLCSP.

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN53523UCX	-40 to 85 °C	16-Bump, 0.4mm Pitch Wafer-Level Chip-Scale Package (WLCSP)	Tape and Reel

Typical Application

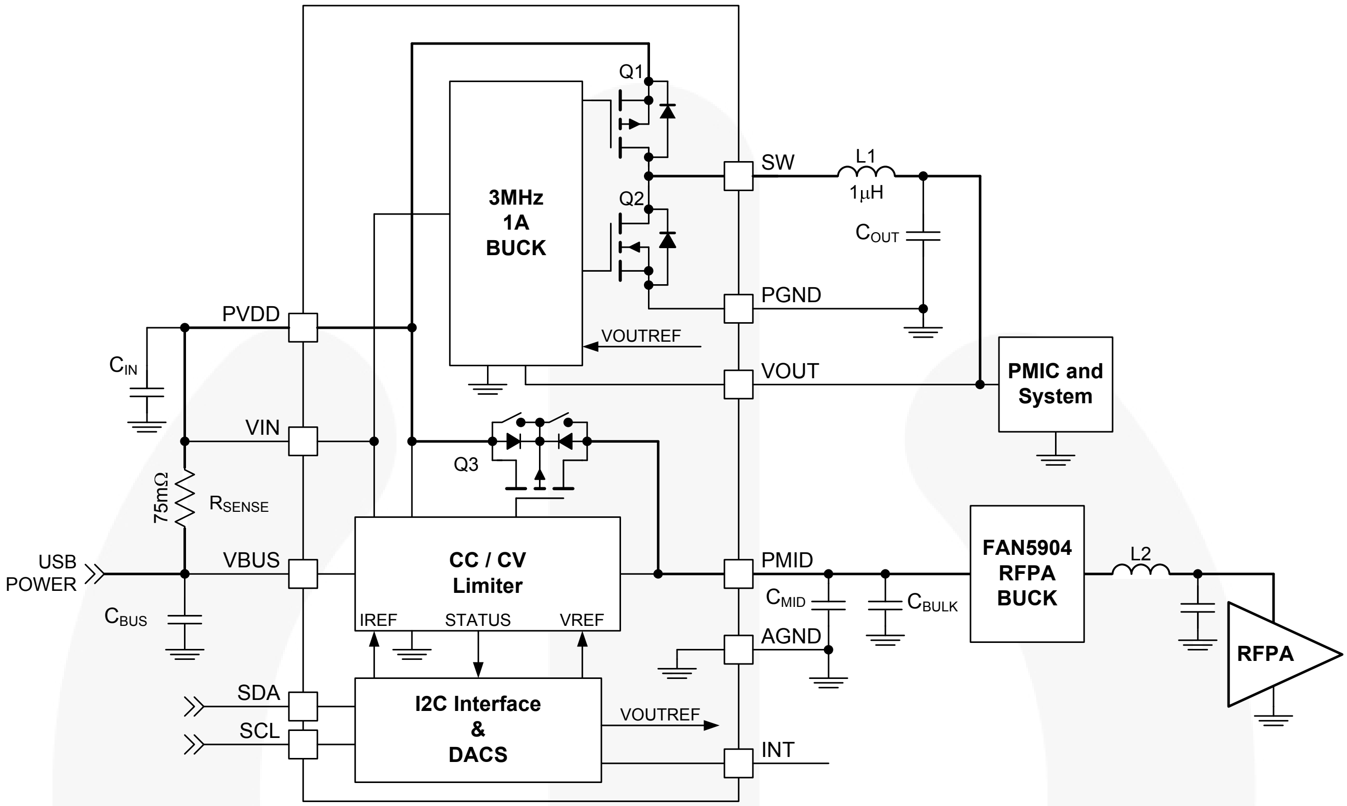
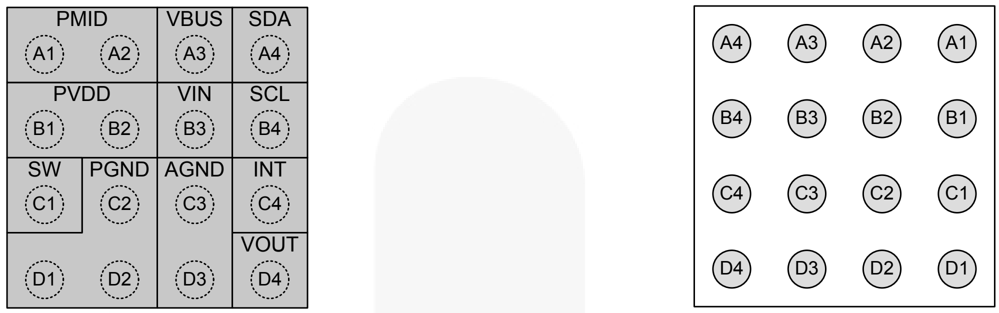


Figure 1. Typical Application using Bulk Capacitors at PMID to Provide RFPA Power (Bold Lines Indicate Power Path)

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Unit
L1	1μH, 1.4A Inductor, 2016	Murata: LQM2MPN1R0M	L	1	μH
C_{BUS}, C_{MID}	4.7μF, 6.3V, X5R, 0603	Various	C	4.7	μF
C_{OUT}	10μF, 6.3V, X5R, 0603	Various	C	10	μF
C_{IN}	1μF, 6.3V, X5R, 0402 or 0603	Various	C	1.0	μF
C_{BULK}	4 Pieces, 330μF, 6.3V, 100mΩ, 7343 Tantalum	Various	C	330	μF
R_{SENSE}	1% 0603	Various	R	75	mΩ

Pin Configuration



Top View (Bumps Down) **Bottom View (Bumps Up)**

Figure 2. Pin Assignments

Pin Definitions

Pin #	Name	Description
A1, A2	PMID	**PMID**. Output of current-limiting switch to charge CBULK for RFPA power.
A3	VBUS	**VBUS**. USB power input. Connect through RSENSE to PVDD
A4	SDA	**SDA**. I^2C interface serial data. This pin should not be left floating.
B1-B2	PVDD	**Power Input**. Input power for the buck regulator. Connect C_{IN} between this node and PGND with minimal path.
B3	VIN	**Bias Voltage Input**. Input power for analog and digital control circuits. This pin should be connected to the PVDD plane.
B4	SCL	**SCL**. I^2C interface serial clock. This pin should not be left floating.
C1	SW	**Switching Node**. Connect to the inductor.
C2 D1-D2	PGND	**Power Ground**. Low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins. These pins are part of the ground plane that extends through C3 and D3.
C3, D3	AGND	**Analog Ground**. All analog signals inside the IC are referenced to this node.
C4	INT	**Interrupt**. This pin pulses LOW whenever a fault condition occurs. This pin is LOW when the buck regulator is disabled or in soft-start and can therefore function as a PGOOD pin.
D4	VOUT	**VOUT**. Connect to C_{OUT}. This pin is the buck regulator's feedback input, as well as the power input for the PA current-limit switch.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	PVDD and VBUS Pin Voltage		–0.5	7.0	V
V_{PMID}	PMID Pin Voltage		–0.5	6.5	V
V_O	Other Pins[1]		–0.3	PMID+0.3	V
$\frac{dV_{BUS}}{dt}$	Maximum Rate of V_{BUS} Increase Above 5.5V when IC Enabled			25	V/ms
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2500		V
		Charged Device Model per JESD22-C101	1000		V
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:

1. Lesser of 6.5V or V_{PMID} + 0.3V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	Supply Voltage	4.0	5.5	V
V_{PMID}	PMID supply voltage	3.0	5.5	V
V_{OUT}	Output Voltage Range	3.0	0.9*PVDD	V
T_A	Ambient Temperature	–40	+85	°C
T_J	Junction Temperature (*See Thermal Regulation and Protection Section*)	0	+120	°C

Thermal Properties

Symbol	Parameter	Typical	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance[2]	74	°C/W

Note:

2. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with two-layer 2s2p boards in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Electrical Specifications

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{BUS} = 5.0V, AUTO Mode, typical values are for T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
I_{VBUS}	VBUS Current	V_{BUS} > $V_{BUS(min)}$, PWM Switching		10		mA
		V_{BUS} > $V_{BUS(min)}$; PWM Enabled, but Not Switching (V_{OUT} > V_{SEL})		3		mA
		SUSPEND State I_{VOUT}=0, I_{PMID}=0		95	150	µA
V_{UVLO}	Under-Voltage Lockout Threshold	V_{BUS} Rising		4.40	4.55	V
		V_{BUS} Falling, TEST=0	3.5	3.7		V
		V_{BUS} Falling, TEST=1	2.6	2.7		V
Logic Pins						
V_{IH}	HIGH-Level Input Voltage		1.05			V
V_{IL}	LOW-Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			200		mV
I_{IN}	Input Bias Current	Input Tied to GND or V_{IN}		0.01	1.00	µA
VOUT Regulation						
V_{OUT}	DC Accuracy At V_{OUT} Pin, W.R.T. Programmed Value,	T_A=25°C, I_{LOAD}=10mA	–1.5%		1.5%	
		I_{LOAD}=500mA	–2.2		2.2	%
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	$I_{OUT(DC)}$=0.3A to 1A		–0.25		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	2.7V ≤ V_{IN} ≤ 5.5V, $I_{OUT(DC)}$=500mA		0.01		%/V
	Transient Response	I_{LOAD} Step=250mA, T_R=T_F=100ns		±30		mV
Power Switches and Protection						
Q1 $R_{DS(ON)}$	Q1 MOSFET On Resistance			120		mΩ
Q2 $R_{DS(ON)}$	Q2 MOSFET On Resistance			100		mΩ
Q3 $R_{DS(ON)}$	Q3 MOSFET On Resistance			120		mΩ
I_{LKGP}	Q1, Q3 Leakage Current	V_{DS}=6V			1	µA
I_{LKGN}	Q2 Leakage Current	V_{DS}=6V			1	µA
I_{LIMPK}	Q1 Peak Current Limit		1350	1550	1800	mA
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			20		°C
T_{T120}	Thermal Regulation Threshold		110			°C
V_{SDWN}	Input OVP Shutdown	Rising Threshold	5.70	5.90	6.10	V
		Falling Threshold		5.5		V
I_{DIS}	PMID Discharge Resistance	V_{BUS} < PMID, PMID > 1.5V		200		Ω

Continued on the following page…

Electrical Specifications (Continued)

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{BUS} = 5.0, typical values are for T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Control						
f_{SW}	Oscillator Frequency		2.65	3.00	3.35	MHz
Soft-Start						
t_{SS}	Regulator Enable to Regulated V_{OUT}	$R_{LOAD} \geq 5\Omega$, to V_{OUT}=3.3V		2.5		ms
V_{SLEW}	Soft-Start V_{OUT} Slew Rate			1.4		V/ms
Input Current and PMID Voltage Limit						
I_{BUS}	Input Current Limit Accuracy, Voltage Across R_{SENSE}	$V(R_{SENSE})$ Setting < 40mV	–5		+5	%
		$V(R_{SENSE})$ Setting $\geq$ 40mV	–5		+5	
V_{MID}	PMID Voltage Limit Accuracy		–3		+3	%

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
		High-Speed Mode, $C_B \le 100pF$			3400	kHz
		High-Speed Mode, $C_B \le 400pF$			1700	kHz
t_{BUF}	Bus-free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		High-Speed Mode, $C_B \le 100pF$		160		ns
		High-Speed Mode, $C_B \le 400pF$		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \le 100pF$		60		ns
		High-Speed Mode, $C_B \le 400pF$		120		ns
$t_{SU;STA}$	REPEATED START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		ns
		High-Speed Mode		10		ns
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \le 100pF$	0		70	ns
		High-Speed Mode, $C_B \le 400pF$	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100pF$		10	80	ns
		High-Speed Mode, $C_B \le 400pF$		20	160	ns
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100pF$		10	40	ns
		High-Speed Mode, $C_B \le 400pF$		20	80	ns
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL After a REPEATED START Condition and After ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100pF$		10	80	ns
		High-Speed Mode, $C_B \le 400pF$		20	160	ns
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100pF$		10	80	ns
		High-Speed Mode, $C_B \le 400pF$		20	160	ns
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

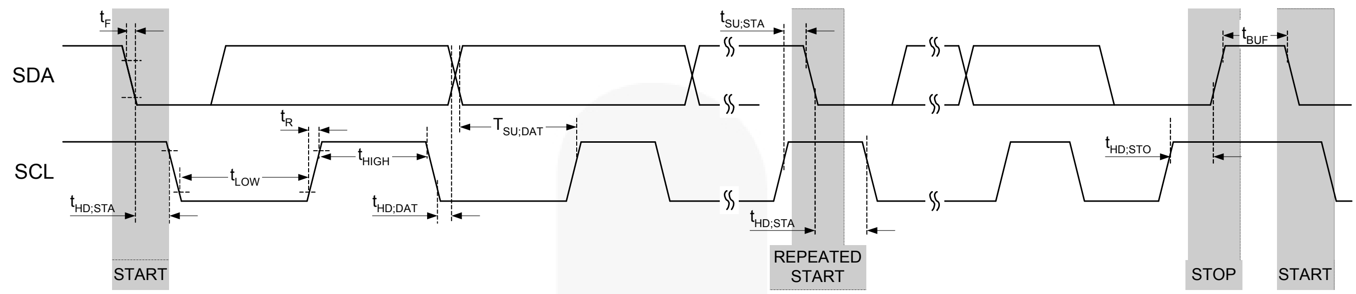
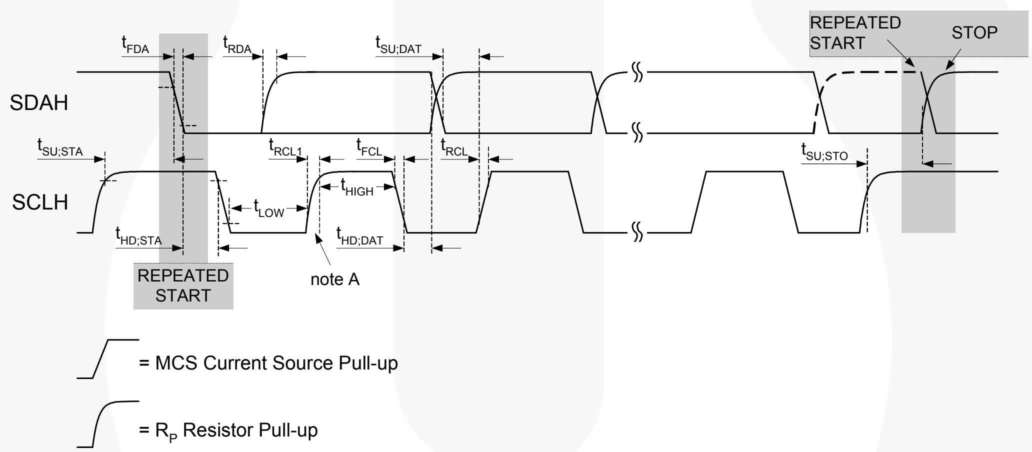


Figure 3. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 4. I²C Interface Timing for High-Speed Mode

Typical Characteristics

Unless otherwise noted, circuit of Figure 1 with component values of Table 1 V_{BUS}= 5.0V, AUTO Mode,V_{OUT}=3.52V.

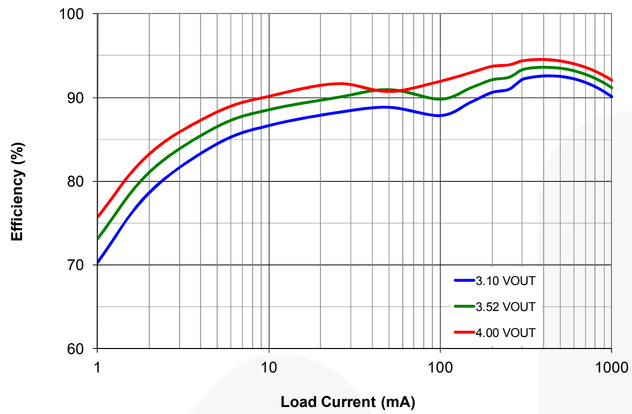


Figure 5. Buck Efficiency vs. Load Current and Output Voltage

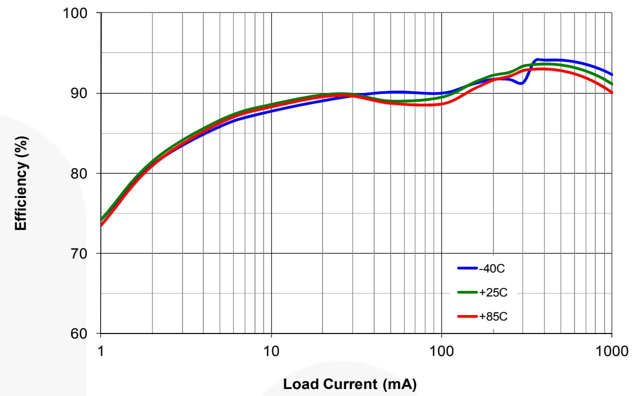


Figure 6. Buck Efficiency vs. Load Current and Temperature

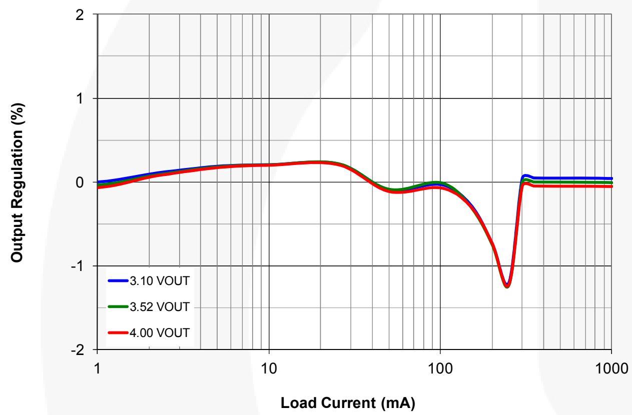


Figure 7. Output Regulation vs. Load Current and Output Voltage

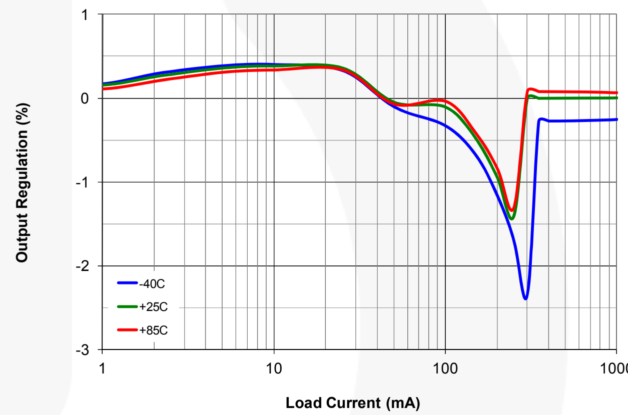


Figure 8. Output Regulation vs. Load Current and Temperature

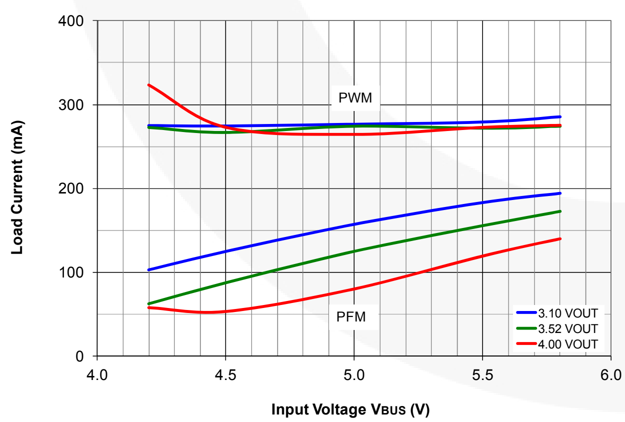


Figure 9. PFM Entry / Exit Level vs. Input Voltage and Output Voltage

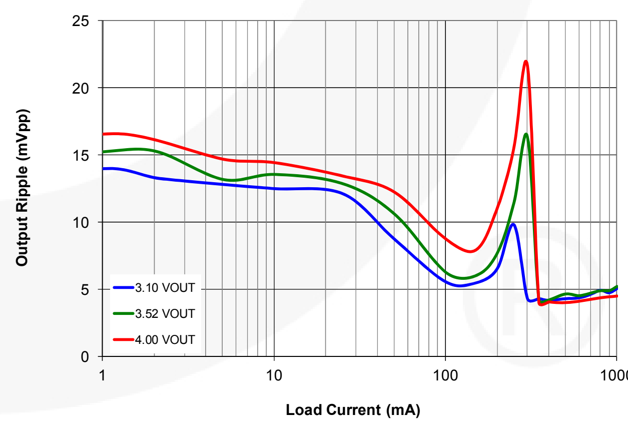


Figure 10. Output Ripple vs. Load Current and Output Voltage

Typical Characteristics (Continued)

Unless otherwise noted, circuit of Figure 1 with component values of Table 1 V_{BUS}= 5.0V, AUTO Mode, V_{OUT}=3.52V.

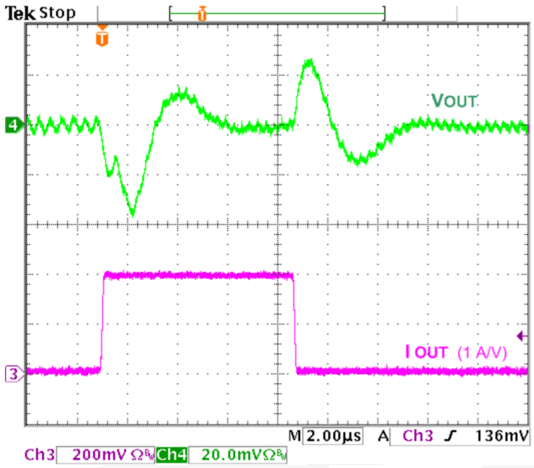


Figure 11. Load Transient, 10-400-10mA, 100ns Edge

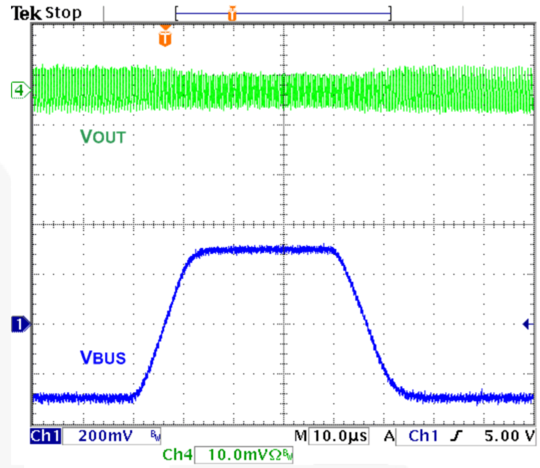


Figure 12. Line Transient, 4.7-5.3V_{BUS}, 10µs Edge (Ch1 HIGH=5.3V, Ch1 LOW=4.7V)

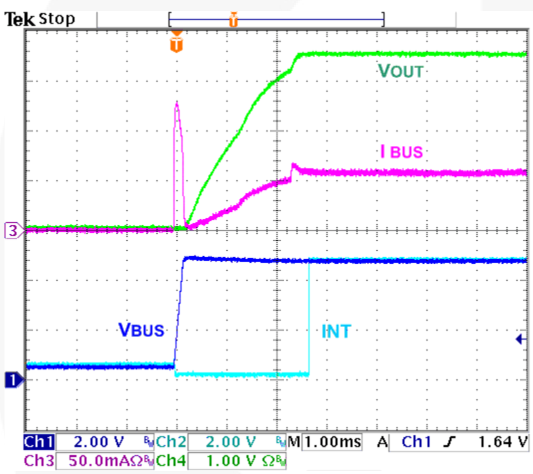


Figure 13. Startup, 50Ω Load

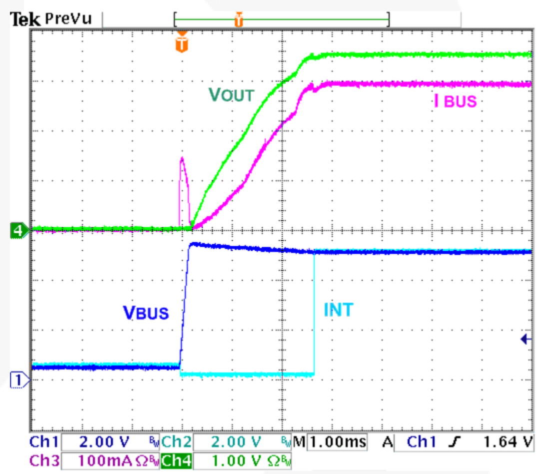


Figure 14. Startup, 10Ω Load,

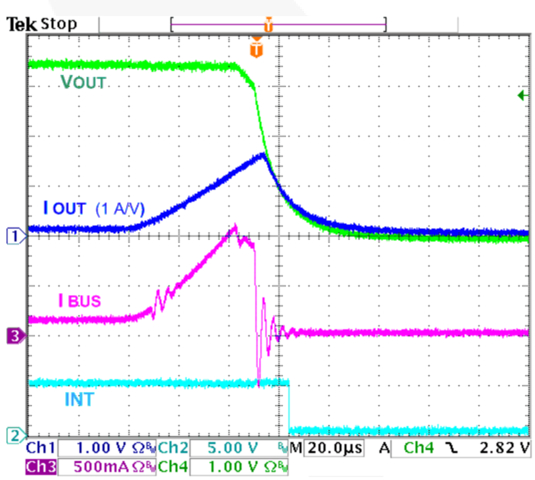


Figure 15. Output Fault (Applied While Running)

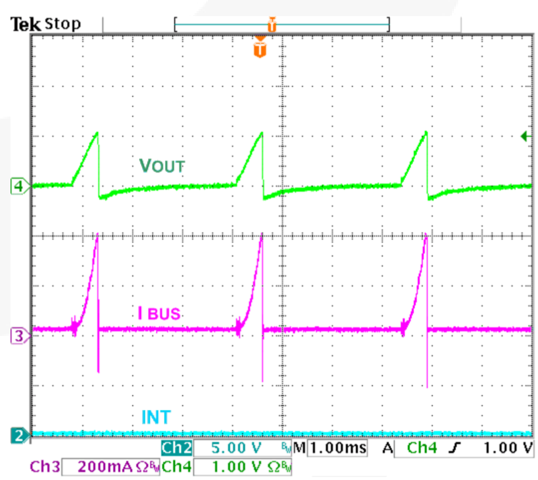


Figure 16. Automatic Restart Behavior (Hiccup) with Output Fault

Typical Characteristics (Continued)

Unless otherwise noted, circuit of Figure 1 with component values of Table 1 V_{BUS}= 5.0V, AUTO Mode, V_{OUT}=3.52V.

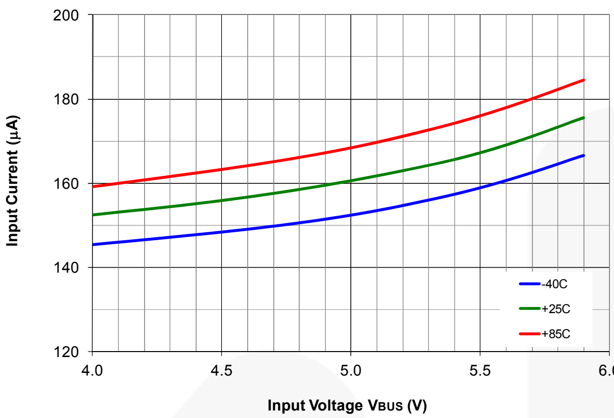


Figure 17. Quiescent Current, Not Suspend R1[6]=0, No Load V_{OUT} or PMID

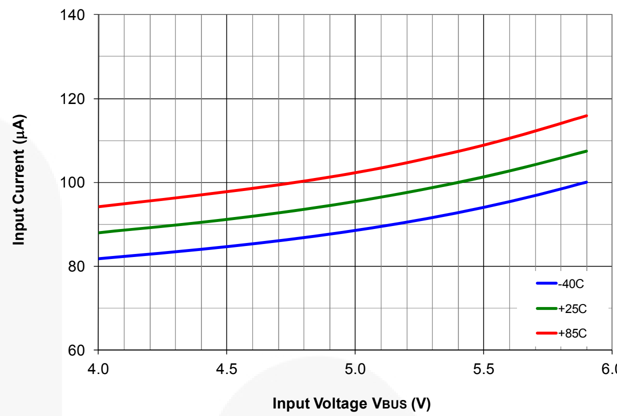


Figure 18. Quiescent Current, Suspend R1[6]=1, No Load V_{OUT} or PMID

The following scope shots were taken with 1.5m length USB cable, C_{BULK} (on PMID)=3x470µF, 100mΩ Tantalum.

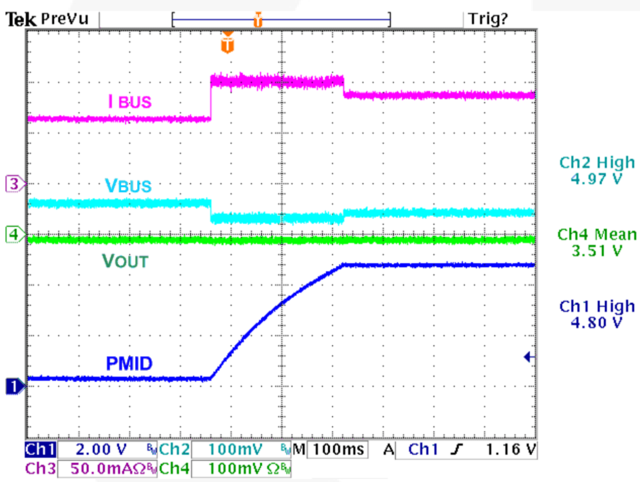


Figure 19. Suspend Release, 100mA I_{BUSLIM} V_{LIM}=4.68V, 3.52V_{OUT}, 50Ω Load, 200Ω on PMID

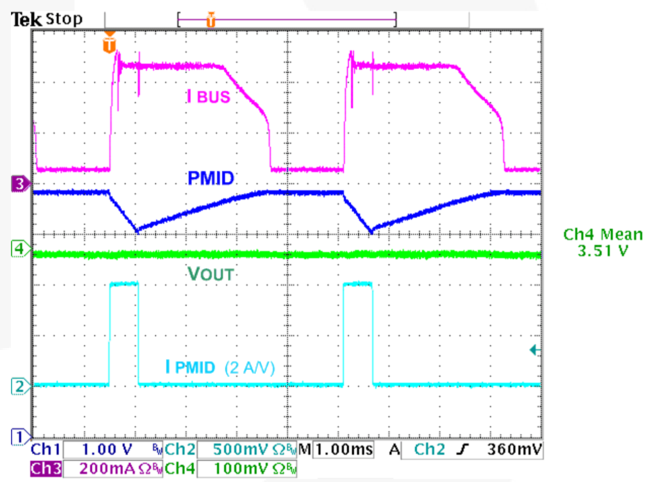


Figure 20. 2A GSM Pulse on PMID (577µs on, 217Hz, 5µs Edge) 500mA I_{BUSLIM}, V_{LIM}=4.68V, 3.52V_{OUT}, 50Ω Load

Operation Description

The FAN53523 combines a buck regulator that delivers an adjustable output from an input voltage supply of 4V to 6V, with USB protection and a current-limit switch. The current for both the buck regulator and the current-limiting switch (Q3 in Figure 1) pass through a current-sense resistor (R_{SENSE}). The voltage across the current-sense resistor controls the current-limiting switch, limiting C_{BULK} charge current. The system power, therefore, has priority when using a current limited input supply (USB).

Using a proprietary architecture with synchronous rectification, the buck is capable of delivering 1A at over 90% efficiency. The regulator operates at a nominal frequency of 3MHz when in PWM Mode, which reduces the value of the external components to 1μH for the output inductor and 10μF for the output capacitor. High efficiency is maintained at light load with single-pulse PFM Mode.

The USB switch (Q3) limits the input current from the USB bus (I_{BUS}) to charge bulk storage capacitors (C_{BULK}), which provide the high power required for Global System for Mobile Communications (GSM) and Long-Term Evolution (LTE) data transmission in USB data cards. The USB switch limits the maximum voltage (V_{LIM}) on C_{BULK}, which allows the use of a 6.3V capacitor with voltage derating. V_{LIM} can be programmed in 140mV steps from 3V to 4.96V.

To limit total input current, an external sense resistor, R_{SENSE}, is used. The buck regulator's input supply and the input to the current-limit switch are both taken from the PVDD side of the sense resistor. This gives the buck regulator priority over the bulk capacitor charging, ensuring that system power is not interrupted due to high-current demand from the RFPA.

Buck Control Scheme

The FAN53523 uses a proprietary non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. Regulator performance is independent of the output capacitor Equivalent Series Resistance (ESR), allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53523 operates in Discontinuous Current Mode (DCM) with single-pulse Pulse Frequency Modulation (PFM), which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, with a glitch of less than 18mV at V_{OUT} during the transition between DCM and CCM Modes.

Startup

Initially, the INT pin is LOW. When V_{BUS} rises above 4.4V, the buck regulator begins a soft-start sequence. When V_{OUT} has risen to its default value (3.52V), INT rises to indicate that power to the system is valid. In this way, the INT pin functions as a PGOOD pin that can be used to drive the host processor's enable pin. The system processor initializes and can then program the IC.

Programmability

Power-on defaults for all programmable values are listed in **bold** characters in Table 2.

I_{BUS}: Input Current Limit

These bits establish the input current limit. This current is the sum of the current through Q3 and the input current to the buck regulator.

Table 2. I_{BUS} Current Limit Programming

		R_{SENSE}=75mΩ
Decimal	**V(R_{SENSE})**	**I_{BUS} Current**
0	**6.8**	**91mA**
1	10.2	136mA
2	34.0	453mA
3	40.8	544mA
4	47.6	635mA
5	54.4	725mA
6	61.2	816mA
7	68.0	907mA

V_{LIM}: PMID Voltage Limit

To accommodate voltage derating of the typically tantalum bulk capacitors (C_{BULK}), the IC limits the voltage on PMID to a programmable value between 3.0V and 4.96V. If the VLIM bits are set to 1111, voltage limiting is disabled, which allows C_{BULK} to rise to PVDD under no load.

Table 3. V_{LIM}, PMID Voltage Limit Programming

V_{LIM} Bits		
Decimal	**Binary**	**V_{LIM}**
0	0000	3.00V
1	0001	3.14V
2	0010	3.28V
3	0011	3.42V
4	**0100**	**3.56V**
5	0101	3.70V
6	0110	3.84V
7	0111	3.98V
8	1000	4.12V
9	1001	4.26V
10	1010	440V
11	1011	4.54V
12	1100	4.68V
13	1101	4.82V
14	1110	4.96V
15	1111	No Limit

V_{SEL}: V_{OUT} Buck Output Voltage

The buck output voltage is programmable in 60mV steps from 3.1V to 4.0V. V_{OUT} may be changed "on the fly" by writing to the VSEL bit.

Table 4. V_{OUT} Programming

VSEL		
Decimal	**Hex**	**V_{OUT}**
0	0	3.10
1	1	3.16
2	2	3.22
3	3	3.28
4	4	3.34
5	5	3.40
6	6	3.46
7	**7**	**3.52**
8	8	3.58
9	9	3.64
10	A	370
11	B	3.76
12	C	3.82
13	D	3.88
14	E	3.94
15	F	4.00

V_{SEL} Transitions

The slew rate of a positive V_{SEL} is 2.4V/ms.

For positive V_{SEL} transitions, the PGOOD bit goes LOW when the V_{SEL} value changes. When V_{OUT} has settled to its new value, PGOOD is set and INT pulses.

Negative V_{SEL} transitions are controlled by the load current. When the V_{SEL} value is lowered by the host, the PGOOD bit goes LOW, the buck regulator reference is lowered, and synchronous rectification is disabled until V_{OUT} reaches the V_{SEL} value. At that point, synchronous rectification is enabled, PGOOD is set, and INT pulses.

Suspend Mode

When the SUSPEND bit is set, the buck regulator continues to operate. The CC/CV limiter is powered down to reduce input current draw; however, a low-current precharge regulator keeps PMID charged at the V_{LIM} setting.

Test Mode

The TEST bit enables a special test mode to facilitate system test and characterization. The intention of the test mode is to allow a power supply to control PMID directly by applying a power source at VBUS. When TEST = 1:

1. The buck regulator operates normally.
2. Q3 operates as a switch, with its gate at GND.
3. V_{UVLO} for V_{BUS} falling is set to 2.7V to allow PMID to be driven to a lower voltage without the IC disabling the buck.

Status and Monitoring

The IC provides extensive monitoring for PMID and VOUT. The monitoring functions are provided in the STAT0 registers and are described below.

PMID Charging Status

The status of the CC/CV limiter that controls Q3 is reported on the CC and CV bits during normal operation. The CV bit is set when the VLIM loop is controlling PMID and Q3 is not in a current-limit condition. Status of this bit is latched in to the I^2C registers when a read commences. The CC bit is set when current limit condition is entered. Status of the CC bit stays latched until reset by an I^2C read. For CV flag to rise, the current-limit loop must be released for at least 256µs.

INT Pin

The open-drain INT pin initially is LOW. When V_{OUT} is in regulation, INT goes HIGH. When the DIS_INT bit is cleared, INT pulses LOW for 125µs whenever a status bit changes state, except as noted below.

INT pulses when the I_{BUS} loop either begins limiting current (CC Mode entry) or stops limiting current (CV Mode entry) through Q3. Read transaction for STAT0 register causes a single INT pulse to be issued

INT pulsing is inhibited by default. The host processor must clear the DIS_INT bit after system startup is complete to receive interrupts. This facilitates use of the INT pin for a PGOOD pin function (host enable) without the use of external low-pass filtering on the INT pin.

If INT pulsing is not inhibited and INT is used as both interrupt and enable functions, an external low-pass filter to the enable pin is needed, as shown in Figure 21.

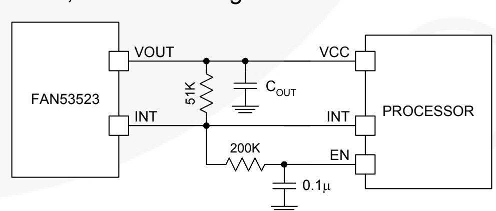


Figure 21. Using INT Pin for Host Processor Interrupt and Enable Function

Thermal Regulation

A dedicated thermal regulation circuit monitors the die temperature at Q3 and limits the thermal dissipation of the device by turning off the PMID path when die temperature exceeds 120°C.

The die temperature is sampled every 4ms. If the detected temperature exceeds 120°C for two consequent sampling periods, the PMID path is turned off for 8ms and a fault is indicated by pulsing INT LOW (T120 interrupt). The T120 interrupt can be disabled by setting the DIS_T120 bit.

The thermal state of the device can be read back from the OT bit in the STAT0 register (STAT0[0]). The OT bit can be used in conjunction with the T120 interrupt to allow the host to ensure that the buck regulator does not shutdown due to the die continuing to heat.

Buck Regulator Details

Soft-Start

The buck regulator uses output slew rate limiting to limit inrush current. If V_{OUT} fails to increase within 1ms from the beginning of soft-start, the regulator shuts down and waits 3.3ms before attempting a restart. If the regulator is at its current limit for more than ~100µs, the regulator shuts down before restarting 3.3ms later. This limits the duty cycle of full output current into a soft-start to about 3%.

$$COUT_{MAX} \approx \left(1A - \overline{I_{LOAD}}\right) \bullet \frac{2000\,\mu}{V_{OUT}} \tag{1}$$

Synchronous rectification is inhibited during soft-start, allowing the IC to start into a pre-charged load.

Under-Voltage Lockout

The under-voltage lockout keeps the buck from operating until V_{BUS} rises above the V_{UVLO} threshold (3.7V). This ensures no misbehavior of the regulator during startup or shutdown.

V_{BUS} Over-Voltage Protection (OVP)

When V_{BUS} exceeds ~5.7V, the IC stops switching and Q3 is turned off. V_{BUS} must return below 5.5V for the IC to restart.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. A series of 16 consecutive PWM cycles in current limit causes the regulator to shut down and stay off for about 3.3ms before attempting a restart.

In the event of a short circuit, the soft-start circuit attempts to restart at 60% of normal current limit and produces an over-current fault after ~300µs, which results in a duty cycle of less than 10% providing current into a short.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or a high ambient temperature, output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 20°C hysteresis.

Minimum Off-Time Effect on Switching Frequency

$t_{ON(MIN)}$ and $t_{OFF(MIN)}$ are both 45ns. This imposes constraints on the maximum $\frac{V_{OUT}}{V_{IN}}$ that the FAN53523 can provide while maintaining a fixed switching frequency in PWM Mode.

The switching frequency drops when the regulator cannot provide sufficient duty cycle at 3Mhz to maintain regulation.

The calculation for switching frequency is:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, \frac{1}{333.3ns}\right)$$

where: (2)

$$t_{SW(MAX)} = 45ns \bullet \left(1 + \frac{V_{OUT} + I_{OUT} \bullet R_{OFF}}{V_{IN} - I_{OUT} \bullet R_{ON} - V_{OUT}}\right)$$

Register Descriptions

FAN53523 has the following user-accessible registers:

Table 5. I²C Register Address

Name	REG# (Hex)	Type	Default
STAT0	0 (00)	Read-Only	
CONTROL0	1 (01)	R/W	0110 0000
BUS_CONTROL	2 (02)	R/W	0000 0100
BUCK_CONTROL	3 (03)	R/W	0111 0000

Register Bit Definitions

The following table defines the operation of each register bit for all IC versions. Default values are in **bold** text.

Bit	Name	Description
STAT0		
7	CV	The status of this bit is updated from the control logic when read commences. 0: Q3 has been in current-limit condition for the past 256μs. 1: Q3 has been in voltage-limit condition for 256μs (current limit released).
6	CC	This bit is reset to 0 immediately after reading STAT0. 0: Q3 has not been in current-limit condition. 1: Q3 has stayed in current-limit condition for more than 256μs.
5	VBUS_OV	0 V_{BUS} is below the V_{BUS} OV threshold. 1 V_{BUS} is above the V_{BUS} OV threshold.
4	VBUS_UV	0 V_{BUS} has fallen below the V_{BUS_UVTH} (3.7V falling) or below PMID. 1 V_{BUS} has risen above the V_{BUS_UVTH} (4.4V rising) and above PMID.
3	PGOOD	1 indicates that V_{OUT} is in regulation. This bit goes LOW whenever : The VSEL register value is changed. PGOOD remains low until V_{OUT} has reached the new V_{SEL} setting. The buck regulator is in current-limit condition for more than 16 PWM cycles. The buck regulator's output has fallen below 10% of its programmed value.
2	BUCK_UV	1 indicates that V_{OUT} is below 90% of its programmed value.
1	BUCK_OC	1 indicates that the buck is in current-limit condition for more than 16 PWM cycles.
0	OT	1 indicates that the IC die temperature is above the thermal regulation limit or the device is in thermal shutdown.
CONTROL0		**Default: 0110 0000**
7	TEST	**0 Normal operation** 1 Test Mode: Q3 is turned on with CC/CV limits disabled. UVLO falling = 2.7V; buck regulator is enabled.
6	SUSPEND	0 Normal operation **1 Buck regulator is enabled, but Q3 operation is disabled. A low current precharge regulator keeps PMID charged at VLIM setting.**
5	DIS_INT	0 INT pin pulses LOW for 125μs to indicate a change in IC status bits. **1 INT pin pulses are disabled. INT pin functions as a buck PGOOD indicator at startup.**
4	DIS_TR	**0 Enable thermal regulation.** When the die temperature is above 120°C, Q3 turns off. *See Thermal regulation section.* 1 Disable thermal regulation. Q3 continues to regulate PMID when the die temperature is above 120°C.
3	DIS_T120	**0 Enable thermal regulation interrupt** when the die temperature is above 120°C. 1 No interrupt occurs when high die temperature is detected.
2:0	Reserved	These bits return 0 when read.
BUS_CONTROL		**Default: 0000 0100**
7:5	IBUS	*See Table 2.*
4	Reserved	This bit returns 0 when read.
3:0	VLIM	*See Table 3.*
BUCK_CONTROL		**Default: 0111 0000**
7:4	VSEL	Sets buck output voltage. *See Table 4.*
3	FPWM	**0 Buck regulator operates in auto PWM/PFM.** 1 Buck regulator operation is forced PWM.
2:0	Reserved	These bits return 0 when read.

I²C Interface

The FAN53523 serial interface is compatible with standard, fast, Fast Plus, and High-Speed (HS) Modes per the I²C-Bus® specifications. The SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 6. I²C Slave Address

7	6	5	4	3	2	1	0
1	1	0	1	0	1	1	R/$\overline{W}$

In Hex notation, the slave address assumes a 0 LSB. The hex slave address is D6H.

Bus Timing

As shown in Figure 22, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

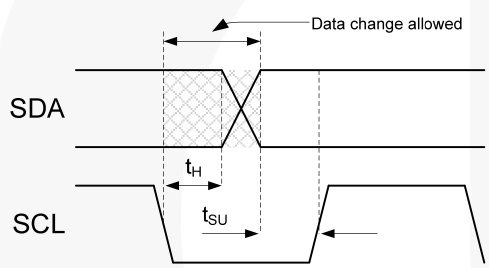


Figure 22. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a "START" condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 23.

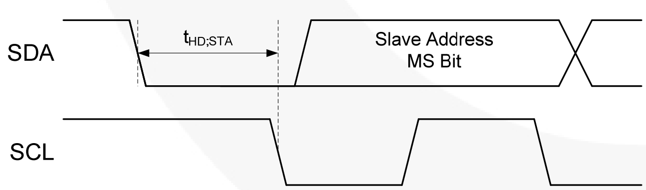


Figure 23. START Bit

A transaction ends with a "STOP" condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 24.

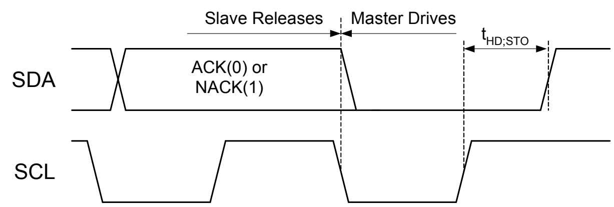


Figure 24. STOP Bit

During a read from the FAN53523 (Figure 27), the master issues a "REPEATED START" after sending the register address and before resending the slave address. The "REPEATED START" is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 25.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical, except the bus speed for HS Mode is 3.4MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast Plus Mode (less than 1MHz clock); slaves do not ACK this transmission.

The master then generates a REPEATED START condition (Figure 23) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 24) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 25).

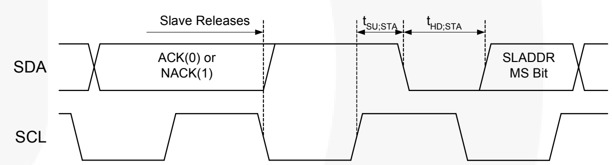


Figure 25. REPEATED START Timing

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 7. Bit Definitions for Figure 26 and Figure 27

Symbol	Definition
S	START, *see Figure 23.*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	REPEATED START, *see Figure 25*
P	STOP, *see Figure 24.*

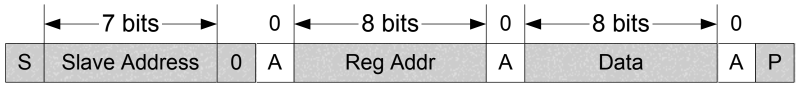


Figure 26. Write Transaction

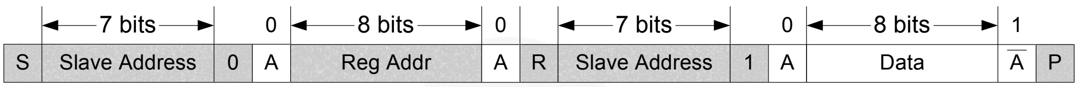


Figure 27. Read Transaction

Applications Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application.

The inductor value affects the average current limit, the PWM-to-PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \right) \quad (3)$$

The maximum average load current, $I_{MAX(LOAD)}$ is related to the peak current limit, $I_{LIM(PK)}$ by the ripple current:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (4)$$

The FAN53523 is optimized for operation with L=1µH, but is stable with inductances up to 1.2µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so lowers the amount of DC current that the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do the core and skin effect losses:

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{\ 2} + \frac{\Delta I^2}{12}} \quad (5)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 8 shows the effects of inductance higher or lower than the recommended 1µH on regulator performance.

Table 8. Inductor Effect on Regulator Performance

Inductance L1	I_{MAX} (LOAD)	ΔV_{OUT}(6)	Transient Response
Increase	Increase	Decrease	Degraded

Inductor Current Rating

The FAN53523 current-limit circuit can allow a peak current of 1.8A to flow through L1 under worst-case conditions. If it is possible for the load to draw that much continuous current, the inductor should be capable of sustaining that current or failing in a safe manner.

For space-constrained applications, a lower current rating for L1 can be used. The FAN53523 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor

Table 1 suggests 0805 capacitors. 0603 capacitors may used if space is at a premium. Due to voltage effects, the 0603 capacitors have a lower in-circuit capacitance than the 0805 package, which can degrade transient response and output ripple.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \quad (6)$$

If values greater than 100µF of C_{OUT} are used, the regulator may fail to start.

If an inductor value greater than 1.0µH is used, at least 30µF of C_{OUT} should be used to ensure stability.

Equivalent Series Inductance (ESL) Effects

The ESL of the output capacitor network should be kept low to minimize the square wave component of output ripple that results from the division ratio C_{OUT}'s ESL and the output inductor (L_{OUT}). The square wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \bullet \frac{ESL_{COUT}}{L1} \quad (7)$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT} = 10µF, a single 10µF 0805 would produce twice the square wave ripple of 2 x 4.7µF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206s. If low output ripple is a chief concern, some vendors produce 0508 or 0612 capacitors that have ultra-low ESL. Placing additional, small-value capacitors near the load also reduces the high-frequency ripple components.

Input Capacitor

The 1µF ceramic input capacitor should be placed as close as possible between the VIN pin and PGND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional bulk capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce under-damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

Layout Recommendations

The layout recommendations below highlight various top copper planes by using different colors.

Bulk capacitors are shown as 7343 capacitors. Bulk capacitors may be paralleled by extending the PGND and PMID planes indefinitely, depending on the number of bulk caps required.

The 0603 C_{IN} capacitor on PMID carries high-frequency currents and must be connected as close to the IC's PMID and PGND pins as possible, as shown in Figure 28 below. VOUT current has less high-frequency content. Its bypass capacitor is shown with a short return to GND. The VOUT pin carries no high-frequency current and can therefore be returned to the IC through vias. Similarly, the VBUS input carries no significant AC current, so the return of CBUS is carried through vias to PGND.

To minimize RFI, SW trace should be as short as possible.

Extending the PGND and VBUS planes improves IC cooling.

Logic signals (EN, SDA, SCL, INT) can connect through vias to the system control logic.

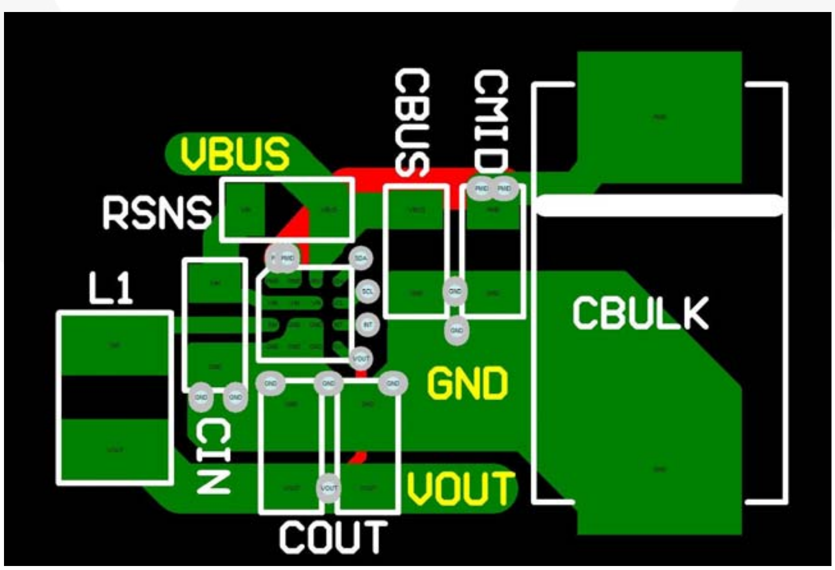
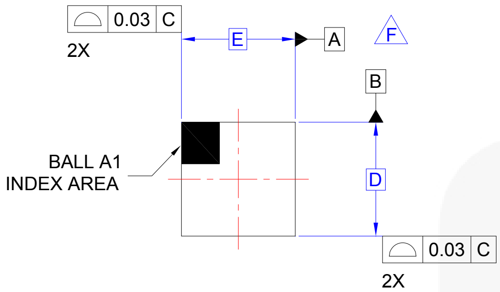
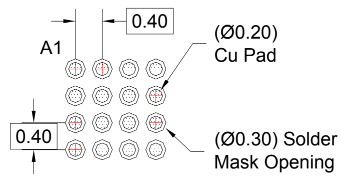


Figure 28. Layout Recommendation

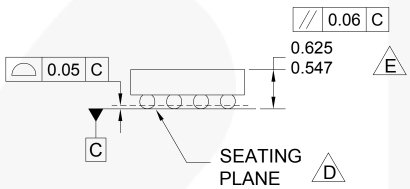
Physical Dimensions

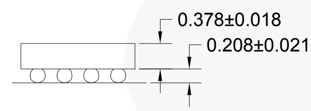


TOP VIEW

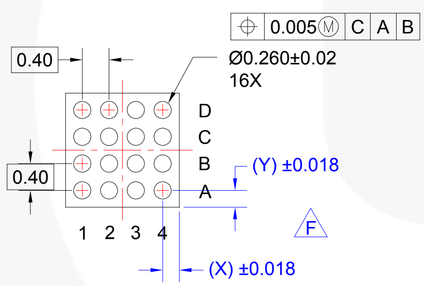


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

Figure 29. 16-Bump, 0.4mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

Product-Specific Dimensions

Product	D	E	X	Y
FAN53523UC	1.56 ±0.030mm	1.56 ±0.030mm	0.180mm	0.180mm

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mWSaver™
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OPTOLOGIC®
OPTOPLANAR®
®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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