FAIRCHILD SEMICONDUCTOR®

January 2008

FAN7316
LCD Backlight Inverter Drive IC

Features

- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 4.5V to 24V
- Backlight Lamp Ballast and Soft Dimming
- Reduces Required External Components
- Precision Voltage Reference Trimmed to 2%
- N-N Half-Bridge Topology
- PWM Control at Fixed Frequency
- Analog and Burst Dimming Function
- Selectable Burst Dimming Polarity by ADIM Voltage
- Striking Frequency Depending on Normal Frequency
- Open-Lamp Protection
- Open-Lamp Regulation
- Short-Circuit Protection
- 20-Pin SOIC

Applications

- LCD TV
- LCD Monitor

Description

The FAN7316 is a LCD backlight inverter drive IC that controls N-N half-bridge topology. The FAN7316 can also drive push-pull topology.

The FAN7316 provides a low-cost solution by integrating the external open-lamp protection circuit. The operating voltage of the FAN7316 is wide, so the FAN7316 doesn't need an external regulator to supply the voltage to the IC. The FAN7316 has the internal bootstrap driver, so the external fast recovery diode can be avoided.

The FAN7316 provides various protections, such as open-lamp regulation, arc protection, open-lamp protection, short-circuit protection, and CMP-high protection to increase the system reliability. The FAN7316 provides analog dimming, burst dimming, and burst dimming polarity selection functions.

The FAN7316 is available in a 20-SOIC package.

Ordering Information

Part Number	Package	Operating Temperature	Packing Method
FAN7316M	20-SOIC	-25 to +85°C	RAIL
FAN7316MX	20-SOIC	-25 to +85°C	TAPE & REEL

All packages are lead free per JEDEC: J-STD-020B standard.

Block Diagram

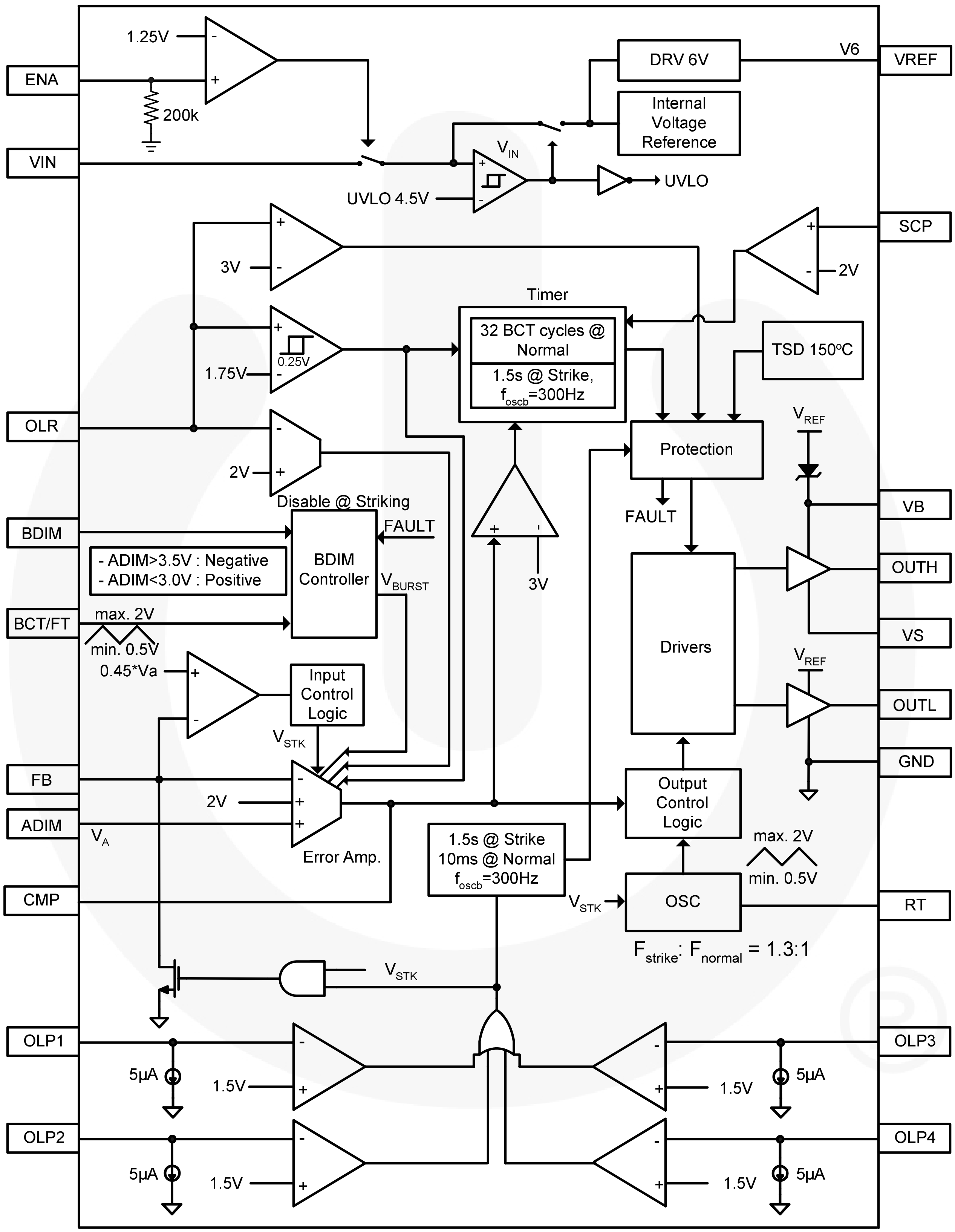
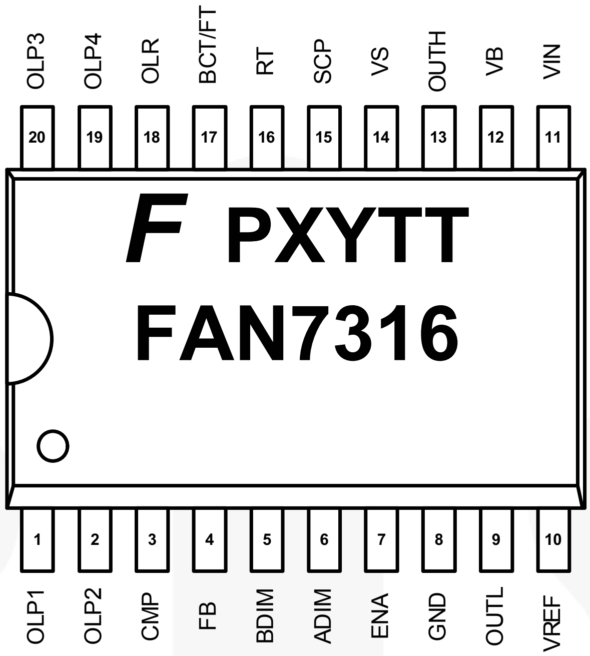


Figure 1. Internal Block Diagram

Pin Assignments



F : Fairchild logo
P : Assembly site code
XY : Year & weekly code
TT : Die run code
FAN7316 : Device name

Figure 2. Package Diagram

Pin Definitions

Pin #	Name	Description
1	OLP1	This pin is for open-lamp protection. If OLP is lower than 1.5V at initial operation, the IC operates at striking mode for BCT 450 cycles. If OLP is lower than 1.5V in normal mode, the IC is shut down after a delay of three BCT cycles.
2	OLP2	
3	CMP	Error amplifier output. A compensation capacitor should be connected between this pin and ground.
4	FB	Error amplifier inverting input. This pin voltage is regulated at 2V or ADIM voltage.
5	BDIM	This pin is for burst dimming input. The voltage range of 0.5 to 2V at this pin controls burst mode duty cycle from 0% to 100%.
6	ADIM	This pin is for positive analog dimming input. This voltage to 2V at this pin controls the amplitude of the lamp current.
7	ENA	This pin is for turning on/off the IC.
8	GND	Ground.
9	OUTL	Low-side driver output. The output stage can deliver about 500mA source and sink current, typically.
10	VREF	6V reference voltage.
11	VIN	IC supply voltage.
12	VB	High-side floating supply. The bootstrap capacitor should be connected between this pin and VS pin, which can be fed by an internal bootstrap MOSFET.
13	OUTH	High-side driver output. The output stage can deliver about 500mA source and sink current, typically.
14	VS	High-side floating supply return. Layout care should be taken to avoid below-ground spikes on this pin.
15	SCP	This pin is for short-circuit protection. If SCP is higher than 2V, IC enters shutdown mode after a delay of 32 BCT cycles.
16	RT	This pin programs the switching frequency. The resistor should be connected between this pin and ground.
17	BCT/FT	This pin programs the burst dimming frequency. A capacitor should be connected between this pin and ground. The waveform of this pin is the triangular waveform whose amplitude is from 0.5V to 2V. This pin voltage goes up to 4V when the IC enters shutdown mode.
18	OLR	This pin is for open-lamp regulation. If the voltage at OLR reaches 2V, the IC makes this pin voltage be controlled not to exceed 2V. If OLR voltage is higher than 1.75V, the IC enters shutdown mode after delays of 451 BCT cycles in striking mode and three BCT cycles in normal mode, respectively. If this pin voltage is higher than 3V, the IC enters shutdown mode without delay.
19	OLP4	This pin is for open lamp protection. If OLP is lower than 1.5V at initial operation, the IC operates at striking mode for BCT 450 cycles. If OLP is lower than 1.5V in normal mode, the IC is shut down after a delay of three BCT cycles.
20	OLP3	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	IC Supply Voltage	4.5	24	V
V_B	High-Side Floating Supply	-0.3	33	V
V_S	High-Side Floating Supply Return	-2(3)	V_B-7	V
T_J	Operating Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
θ_{JA}	Thermal Resistance Junction-Air(1,2)		90	°C /W
P_D	Power Dissipation		1.4	W

Notes:
1. Thermal resistance test board. Size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
2. Assume no ambient airflow.

Recommended Operating Ratings

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	IC Supply Voltage	4.5	22	V
V_B	High-Side Floating Supply	V_S-0.3	V_S+6.5	V
V_S	High-Side Floating Supply Return	(3)	25	V
T_A	Operating Ambient Temperature	-25	+85	°C

Notes:
3. The V_S is tolerant to short negative transient spikes.

Pin Breakdown Voltage

Pin #	Name	Value	Unit	Pin #	Name	Value	Unit
1	OLP1	7	V	11	VIN	24	V
2	OLP2	7		12	VB	33	
3	CMP	7		13	OUTH	7	
4	FB	7		14	VS	33	
5	BDIM	7		15	SCP	7	
6	ADIM	7		16	RT	7	
7	ENA	7		17	BCT/FT	7	
8	GND			18	OLR	7	
9	OUTL	7		19	OLP4	7	
10	VREF	7		20	OLP3	7	

Electrical Characteristics

For typical values, T_A=25°C, V_{IN}=18V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF} Section (Recommend X7R Capacitor)						
V_6	6V Regulation Voltage	CMP=0V	5.76	6.00	6.24	V
V_{6line}	6V Line Regulation	V_{IN}=7V, 18V			25	mV
V_{6load}	6V Load Regulation	10μA≤16≤5mA			60	mV
Oscillator Section (Main)						
V_{fbth}	FB Threshold Voltage	ADIM=1, OLP=0V		0.45		V
V_{cth}	CT High Voltage[4]			2.0		V
V_{ctl}	CT Low Voltage[4]			0.5		V
Oscillator Section (Burst)						
f_{oscb}	Oscillation Frequency	T_A=25°C, BCT=10nF	288	300	312	Hz
		BCT=10nF	282	300	318	Hz
V_{bcth}	BCT High Voltage	BCT=10nF		2		V
V_{bctl}	BCT Low Voltage	BCT=10nF		0.5		V
V_{bctft}	BCT Fault Voltage	SCP=2.5V		4		V
Error Amplifier Section						
G_{m1}	Error Amplifier Trans-conductance	CMP=1, ADIM=1V	100	360	600	umho
A_V	Error Amplifier Open-loop Gain[4]			50		dB
V2	2V Regulation Voltage	T_A=25°C, ADIM=2.5V	1.97	2.00	2.03	V
				260		ppm/°C
I_{sin}	CMP Sink Current	ADIM=1V, FB=2.5V	66	100	134	μA
I_{sur1}	CMP Source Current 1	CMP=1V, FB=0V	-134	-100	-66	μA
I_{sur2}	CMP Source Current 2	1.75V<OLR<2V		1.6		μA
I_{sur3}	CMP Source Current 3[4]	OLR>2V		0		μA
Under-Voltage Lockout Section (UVLO)						
V_{th}	Start Threshold Voltage	ENA=2.5V	3.9	4.2	4.5	V
V_{thhys}	Start Threshold Voltage Hysteresis	ENA=2.5V	0.2	0.4	0.6	V
I_{st}	Start-up Current	V_{IN}=V_{th}-0.2	20	60	150	μA
I_{op}	Operating Supply Current	Not switching		1.5	2.0	mA
ENA Section						
V_{ena}	Enable State Input Voltage		2		5	V
V_{dis}	Disable Stage Input Voltage				0.7	V
I_{sb}	Stand-by Current	ENA=0		100	150	μA

Note:
4. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (Continued)

For typical values, T_A=25°C, V_{IN}=18V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Protection Section						
V_{scp}	Short-Circuit Protection Voltage		1.9	2.0	2.1	V
V_{cmpr}	CMP Protection Voltage		2.8	3.0	3.2	V
V_{olp}	Open-Lamp Protection Voltage		1.4	1.5	1.6	V
V_{ovp}	Over-Voltage Protection		2.85	3.00	3.15	V
V_{olr1}	Open-Lamp Regulation Voltage 1		1.60	1.75	1.90	V
V_{olr2}	Open-Lamp Regulation Voltage 2		1.9	2.0	2.1	V
V_{olrhy}	Open-Lamp Regulation Hysteresis(5)			250		mV
t_{scp}	Short-Circuit Protection Delay(5)	Striking, f_{oscb}=300Hz	1.4	1.5	1.6	s
		Normal, f_{oscb}=300Hz	80	100	120	ms
t_{cmp}	CMP Protection Delay(5)	Striking, f_{oscb}=300Hz	1.4	1.5	1.6	s
		Normal, f_{oscb}=300Hz	80	100	120	ms
t_{olp}	Open-Lamp Protection Delay(5)	Striking, f_{oscb}=300Hz	1.4	1.5	1.6	s
		Normal, f_{oscb}=300Hz	6		10	ms
t_{olr}	Open-Lamp Regulation Delay(5)	Striking, f_{oscb}=300Hz	1.4	1.5	1.6	s
		Normal, f_{oscb}=300Hz	80	100	120	ms
TSD	Thermal Shutdown(5)			150		°C
Output Section						
f_{nrmo}	Output Normal Frequency	T_A=25°C, R_T=27kΩ	47.4	49.0	50.6	kHz
		R_T=27kΩ	47	49	51	
f_{str}	Output Striking Frequency	T_A=25°C, R_T=27kΩ	61.5	64.0	66.4	kHz
		R_T=27kΩ	61	64	67	
V_{ouvh}	OUTH Voltage Before Start-up	V_{IN}=V_{th}-0.6	-0.45	0	0.45	V
V_{ouvl}	OUTL Voltage Before Start-up	V_{IN}=V_{th}-0.6	-0.45	0	0.45	V
V_{osth}	High-Side Output Voltage at V_{ENA}=0V	V_{IN}=18V	-0.45	0	0.45	V
V_{ost}	Low-Side Output Voltage at V_{ENA}=0V	V_{IN}=18V	-0.45	0	0.45	V
V_{ohh}	High-Side Output Voltage	V_{IN}=18V	5.5	6.0	6.5	V
V_{ohl}	Low-Side Output Voltage	V_{IN}=18V	5.5	6.0	6.5	V
I_{dsurh}	High-Side Output Drive Source Current(5)	V_{IN}=18V		500		mA
I_{dsinh}	High-Side Output Drive Sink Current(5)	V_{IN}=18V		500		mA
I_{dsurl}	Low-Side Output Drive Source Current(5)	V_{IN}=18V		500		mA
I_{dsinl}	Low-Side Output Drive Sink Current(5)	V_{IN}=18V		500		mA
t_{dead}	Dead Time(5)			500		ns

Note:
5. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

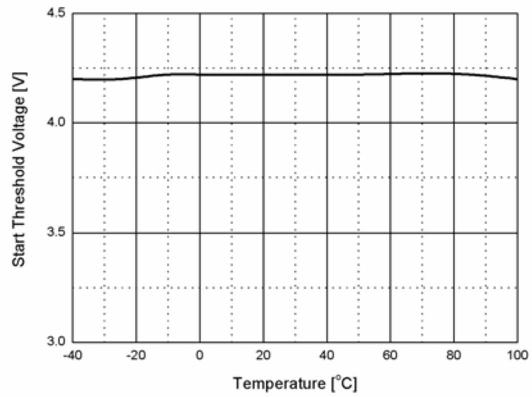


Figure 3. Start Threshold Voltage vs. Temp.

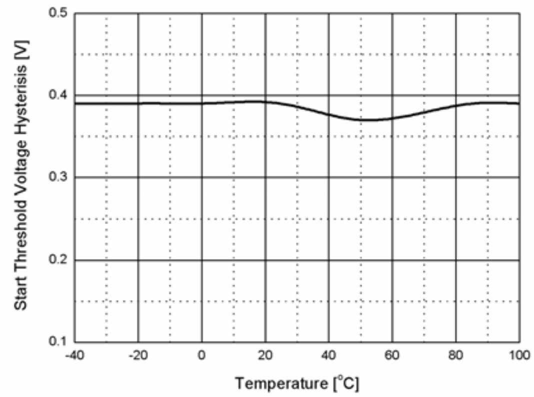


Figure 4. Start Threshold Voltage Hys. vs. Temp.

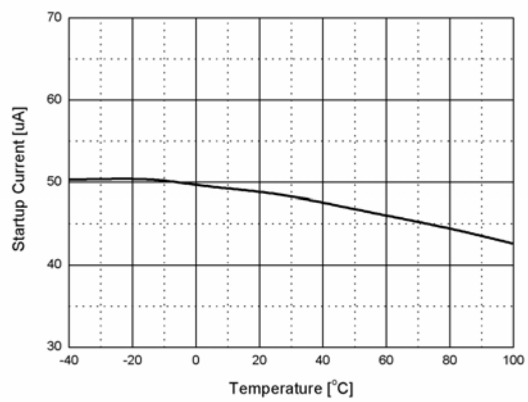


Figure 5. Start-up Current vs. Temp.

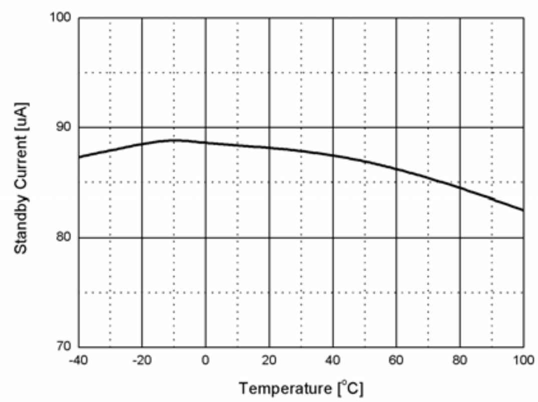


Figure 6. Standby Current vs. Temp.

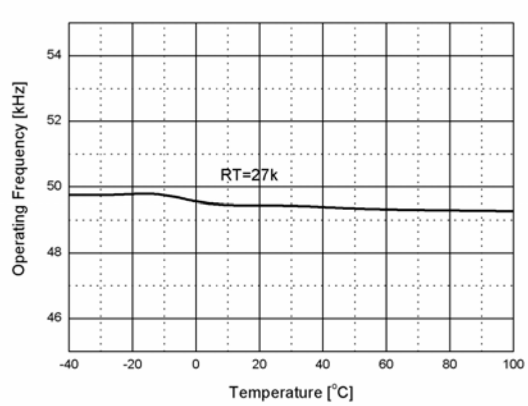


Figure 7. Operating Frequency vs. Temp.

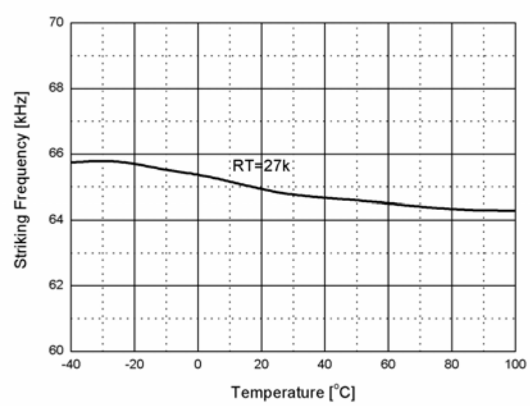


Figure 8. Striking Frequency vs. Temp.

Typical Performance Characteristics (Continued)

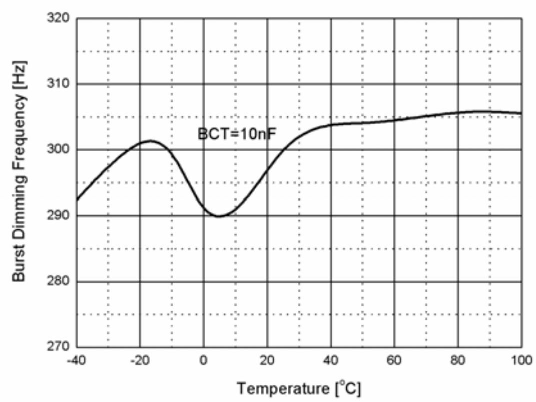


Figure 9. Burst Dimming Frequency vs. Temp.

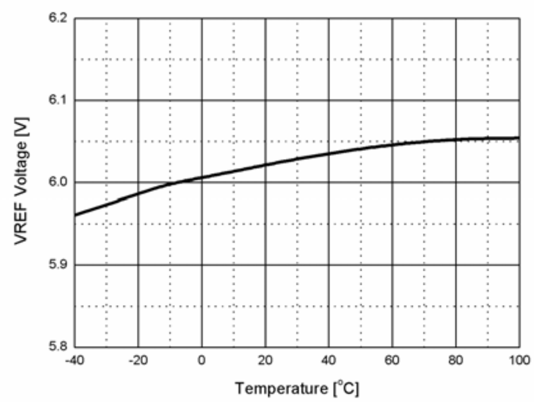


Figure 10. V_{REF} Voltage vs. Temp.

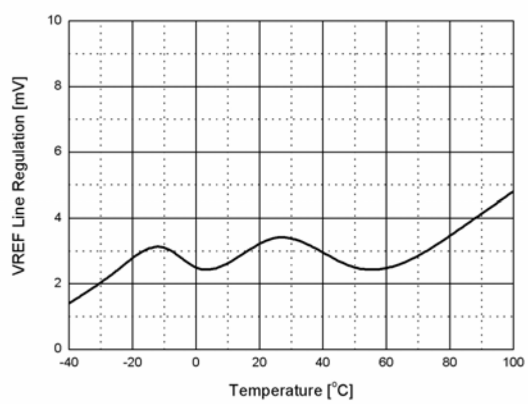


Figure 11. V_{REF} Line Regulation Voltage vs. Temp.

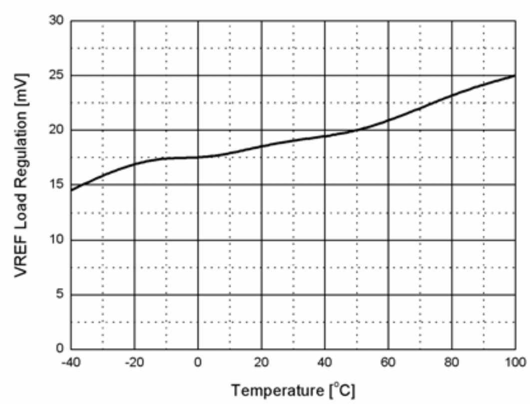


Figure 12. V_{REF} Load Regulation Voltage vs. Temp.

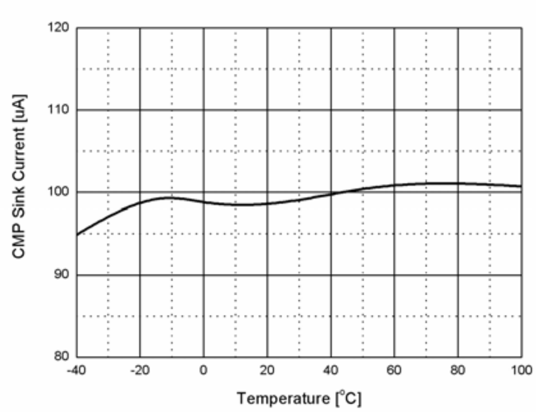


Figure 13. CMP Sink Current vs. Temp.

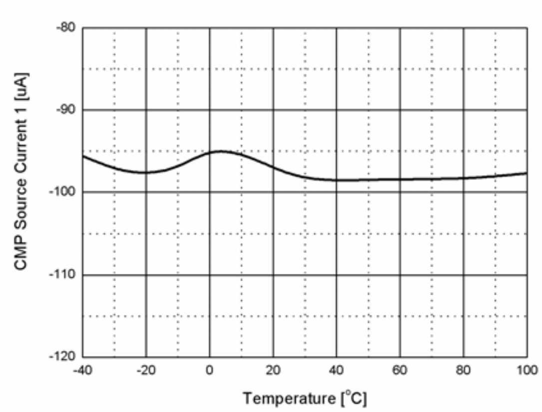


Figure 14. CMP Source Current 1 vs. Temp.

Typical Performance Characteristics (Continued)

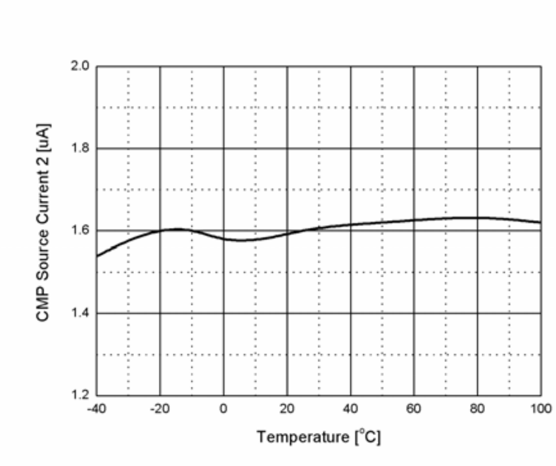


Figure 15. CMP Source Current 2 vs. Temp.

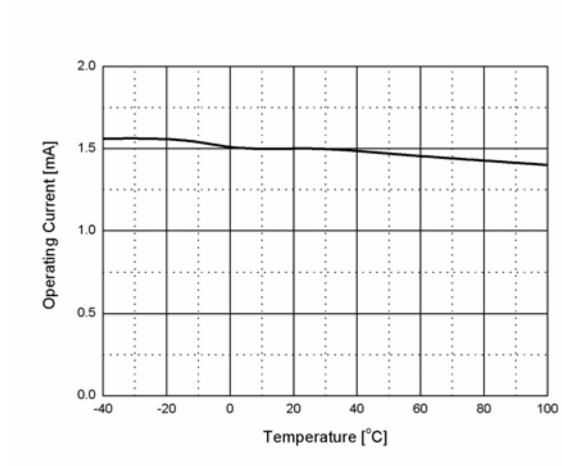


Figure 16. Operating Current vs. Temp.

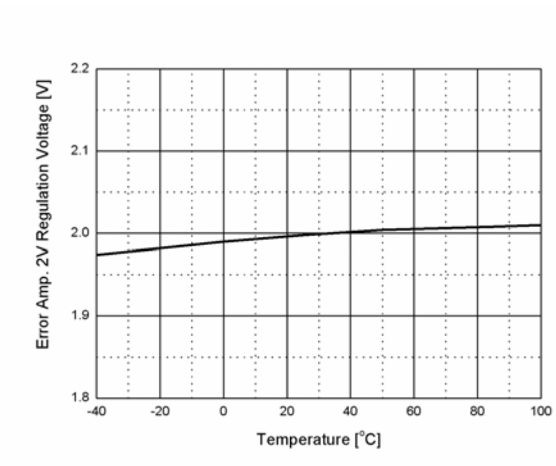


Figure 17. Error Amplifier 2V Voltage vs. Temp.

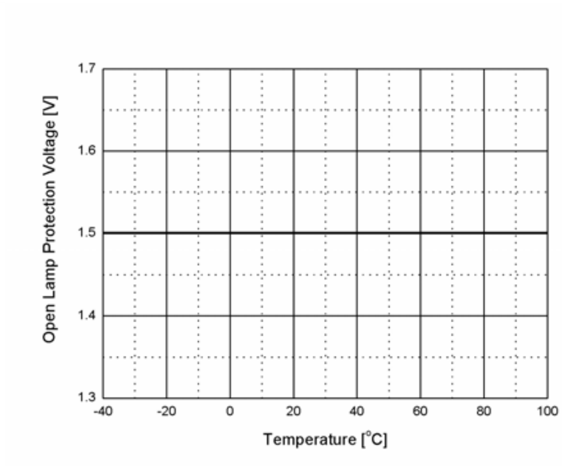


Figure 18. Open-Lamp Protection Voltage vs. Temp.

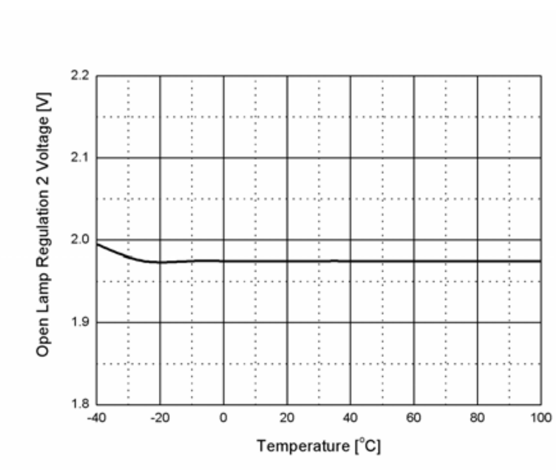


Figure 19. Open-Lamp Regulation Voltage 2 vs. Temp.

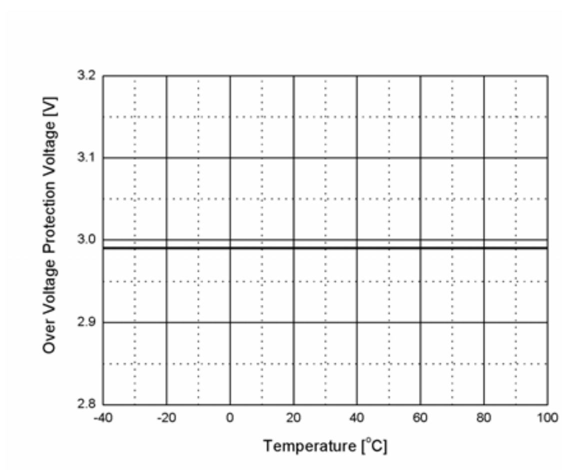


Figure 20. Over-Voltage Protection vs. Temp.

Typical Performance Characteristics (Continued)

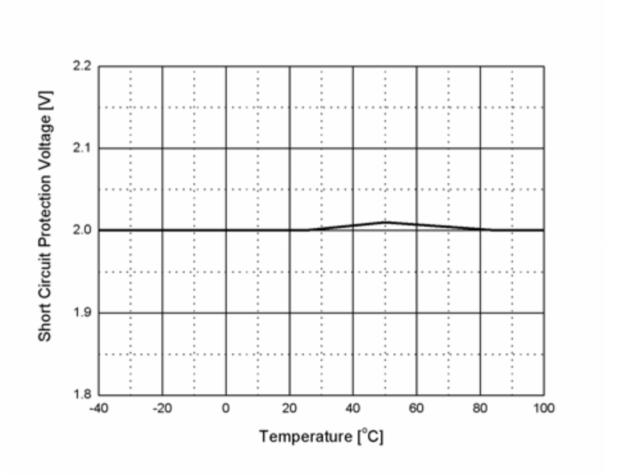


Figure 21. Short-Circuit Protection Voltage vs. Temp.

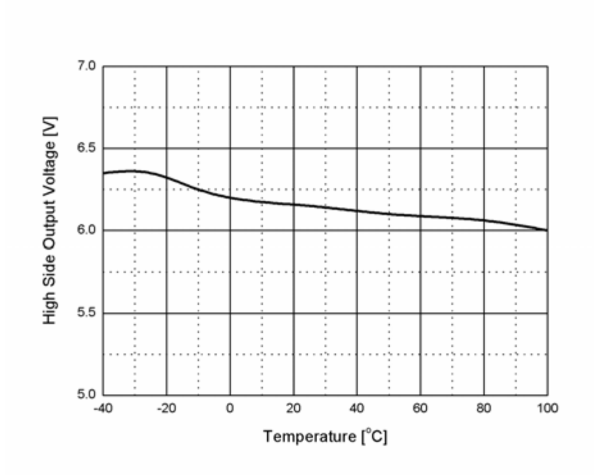


Figure 22. High-Side Output Voltage vs. Temp.

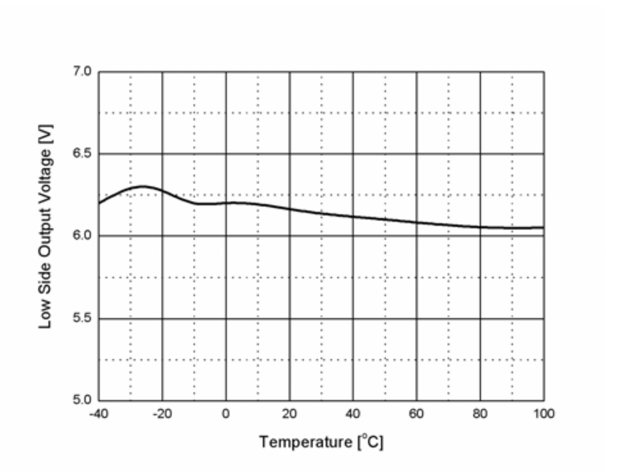


Figure 23. Low-Side Output Voltage vs. Temp.

Functional Description

UVLO: The under-voltage lockout (UVLO) circuit guarantees the stable operation of the IC's control circuit by stopping and starting it as a function of the V_{IN} value. The UVLO circuit turns on the control circuit when V_{IN} exceeds 4.5V. When V_{IN} is lower than 3.9V, the IC's start-up current is less than 150µA.

ENA: Applying voltage higher than 2V to the ENA pin enables the IC. Applying voltage lower than 0.7V to the ENA pin disables the IC.

Internal Main Oscillator: The internal timing capacitor (CT), 20pF, is charged by the reference current source, which is formed by the timing resistor (RT). The RT voltage is regulated at 1.728V. The sawtooth waveform charges up to 2V. Once CT voltage is reached, the CT begins discharging down to 0.5V. Next, the CT starts charging again and a new switching cycle begins, as shown in Figure 24. The main frequency is programmed by adjusting the R_T value. The main frequency is calculated as:

$$f_{OSC} \approx \frac{2736}{R_T[K\Omega]}[KHz] \quad (1)$$

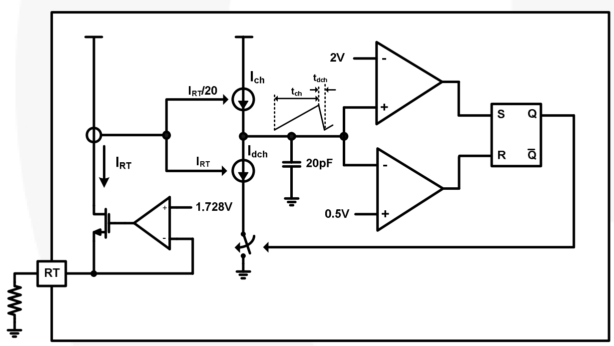


Figure 24. Main Oscillator Circuit

The striking frequency is 1.3 times as high as the main frequency.

Burst Dimming Oscillator: The burst capacitor timing (BCT) is charged by the internal reference current source. The triangular waveform charges up to 2V. Once the BCT voltage is reached, the capacitor begins discharging down to 0.5V. Next, the BCT starts charging again and a new switching cycle begins, as shown in Figure 25. The burst dimming frequency is programmed by adjusting BCT value. The burst dimming frequency is calculated as:

$$f_{OSCB} \approx \frac{3 \bullet 10^3}{BCT[nF]}[Hz] \quad (2)$$

To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

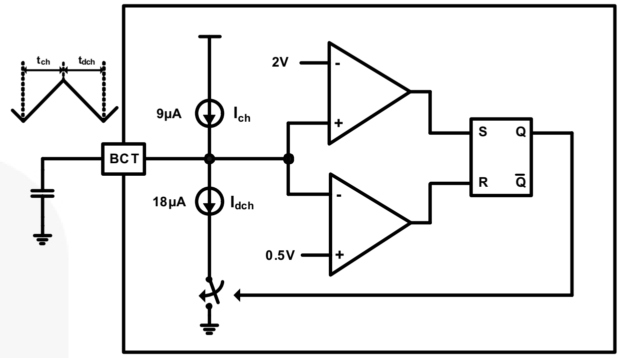


Figure 25. Burst Dimming Oscillator Circuit

Analog Dimming: There are two kinds of analog dimming polarity: positive analog dimming and negative analog dimming.

For positive analog dimming, the lamp intensity is controlled with the ADIM signal. The lamp intensity is proportional to ADIM signal; as ADIM voltage increases, the lamp intensity increases. Figure 26 shows how to implement negative analog dimming circuit and Figure 27 shows the lamp current waveform vs. DIM in positive analog dimming mode.

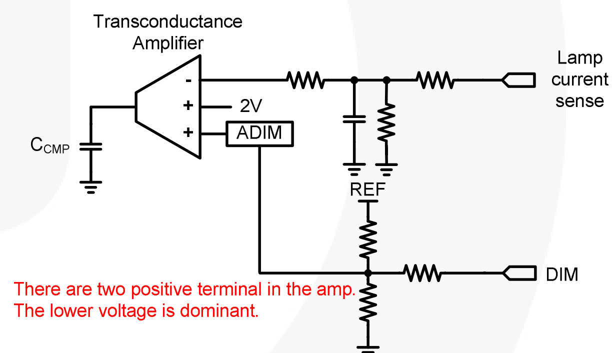


Figure 26. Positive Analog Implementation Circuit

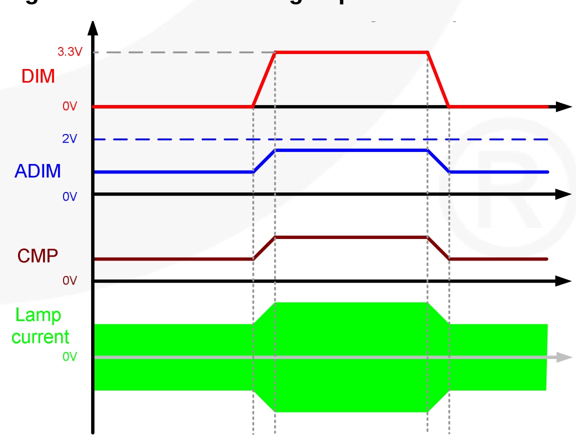


Figure 27. Positive Analog Dimming Waveform

For negative analog dimming, the lamp intensity is controlled with the external DIM signal and the resistors. The lamp intensity is inversely proportional to DIM voltage. As DIM voltage increases, the lamp intensity decreases. Figure 28 shows how to implement a negative analog dimming circuit and Figure 29 shows the lamp current waveform vs. DIM in negative analog dimming mode.

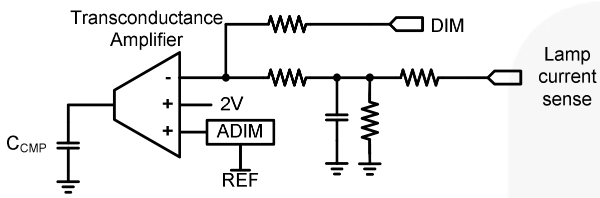


Figure 28. Negative Analog Implementation Circuit

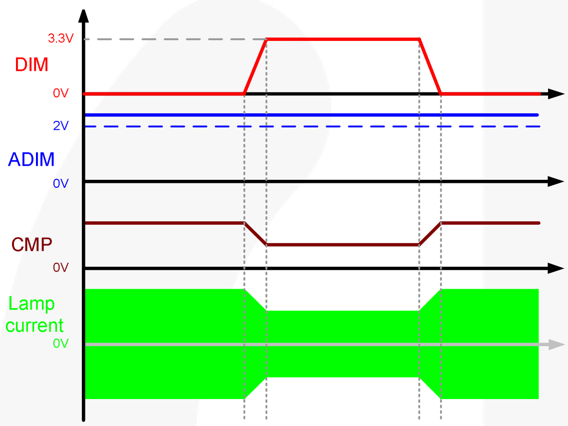


Figure 29. Negative Analog Dimming Waveform

Burst Dimming Polarity Selection: FAN7316 provides the function to select burst dimming polarity by ADIM pin voltages. If ADIM pin voltage is lower than 3V, positive burst dimming is chosen. Refer to Figure 30.

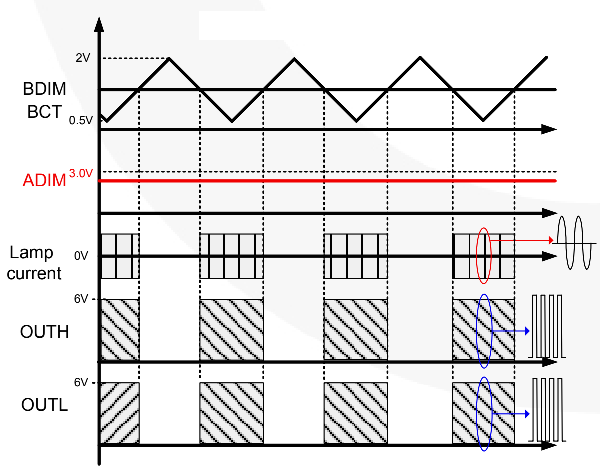


Figure 30. Positive Burst Dimming Chosen

If the ADIM pin voltage is higher than 3.5V, negative dimming polarity is chosen. Refer to Figure 31.

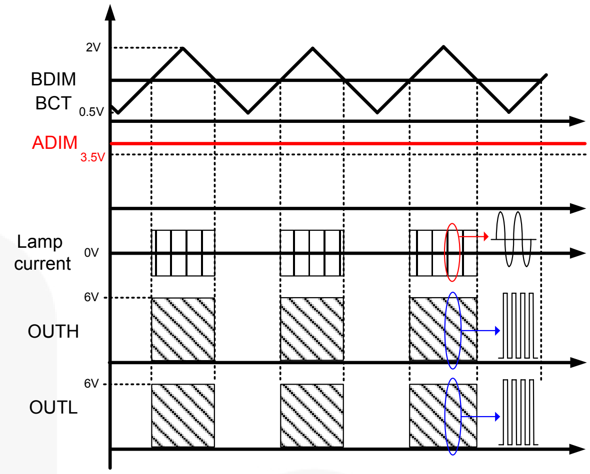


Figure 31. Negative Burst Dimming Chosen

Burst Dimming: There are also two kinds of burst dimming polarity: positive analog dimming and negative analog dimming. The lamp intensity is controlled with the BDIM voltage. By comparing the BDIM voltage with the 0.5~2V triangular waveform of burst dimming oscillator (BCT), the PWM pulse is generated. The PWM pulse controls the CMP voltage by discharging and charging the CMP capacitor.

For positive burst dimming, when BDIM voltage is higher than BCT voltage, the lamp current is turned on. So, 2V on BDIM commands full brightness. The duty cycle of the PWM pulse determines the lamp brightness. The lamp intensity is proportional to BDIM voltage. As BDIM voltage increases, the lamp intensity also increases. Figure 32 shows the lamp current waveform vs. DIM in positive analog dimming mode.

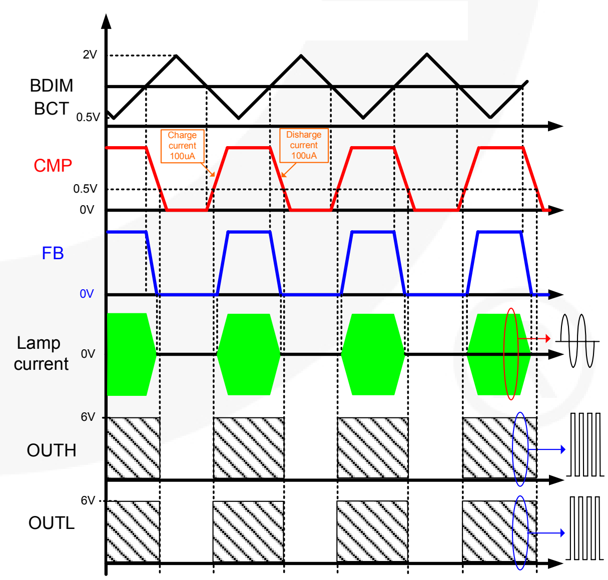


Figure 32. Positive Burst Dimming Operation

For negative burst dimming, when BDIM voltage is lower than BCT voltage, the lamp current is turned on. So, 0V on BDIM commands full brightness. The duty cycle of the PWM pulse determines the lamp brightness. The lamp intensity is inversely proportional to BDIM voltage. As BDIM voltage increases, the lamp intensity decreases. Figure 32 shows the lamp current waveform vs. DIM in negative analog dimming mode.

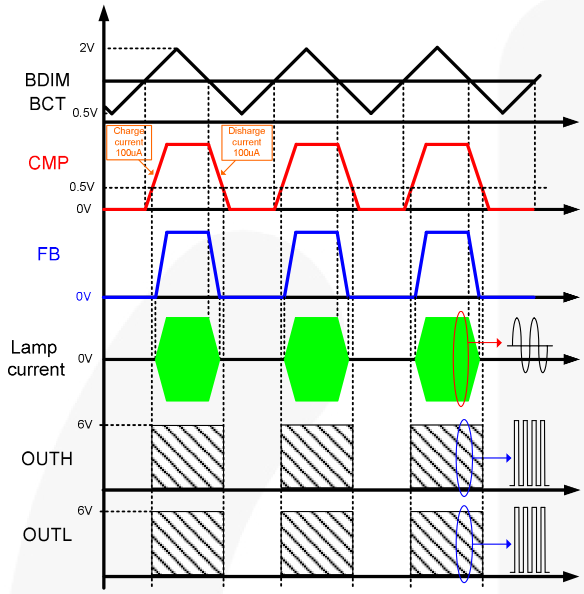


Figure 33. Positive Burst Dimming Operation

Burst dimming can be implemented by not only DC voltage, also PWM pulse as BDIM signal. Figure 34 shows how to implement burst dimming by using PWM pulse as BDIM signal.

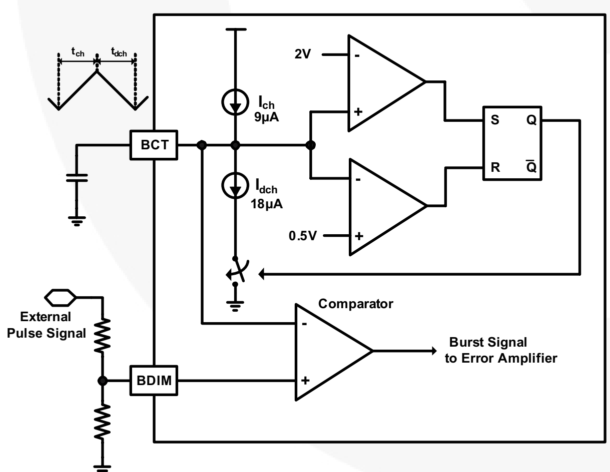


Figure 34. Burst Dimming Using an External Pulse

During striking mode, burst dimming operation is disabled to guarantee the continuous striking time. Figure 35 shows that burst dimming is disabled during striking mode.

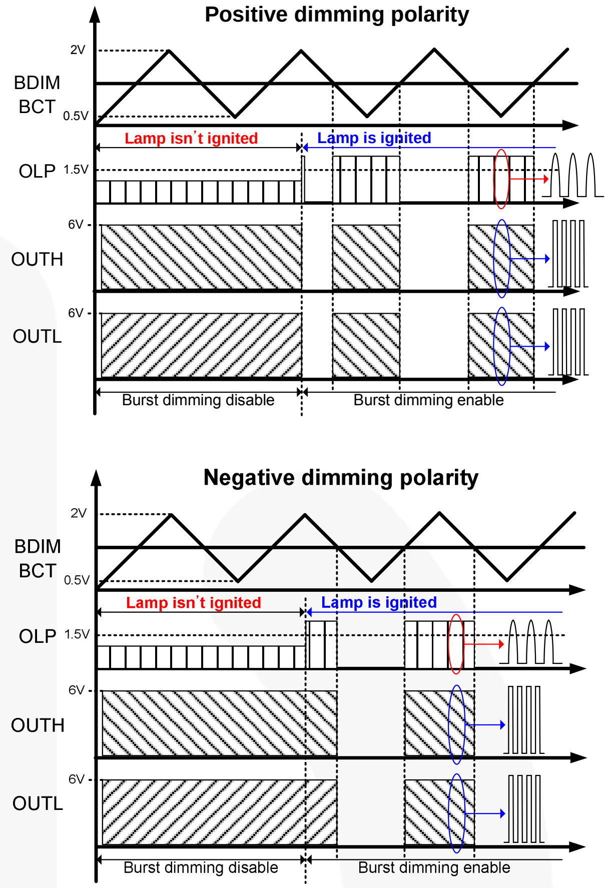


Figure 35. Burst Dimming During Striking Mode

Output Drives: FAN7316 is designed to drive high-side and low-side MOSFETs with symmetrical duty cycle. A fixed dead time of 500ns is introduced between two outputs at maximum duty cycle, as shown Figure 36.

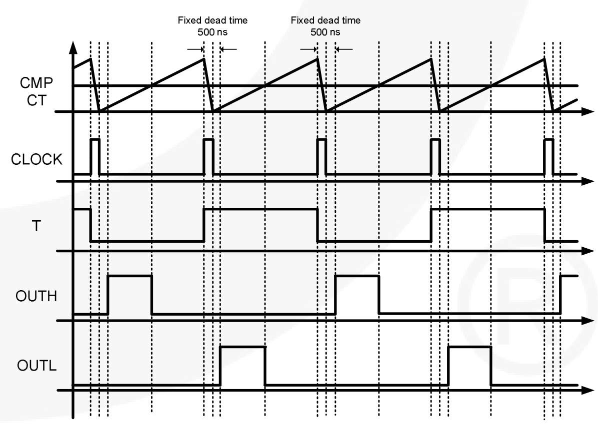


Figure 36. MOSFETs Gate Drive Signal

Bootstrap Operation: To choose the proper C_{BS} value, the external MOSFET can be seen as an equivalent capacitor. This capacitor, C_{IN}, is related to the MOSFET total gate charge as:

$$C_{IN} = \frac{Q_{GATE}}{V_{GATE}} \tag{3}$$

The ratio between capacitors C_{IN} and C_{BS} is proportional to the cyclical voltage loss:

$$C_{BS} >> C_{IN} \tag{4}$$

For example: if Q_{GATE} is 24nC and V_{GATE} is 10V, C_{IN} is 2.4nF. With C_{BS}=100nF, the drop is 240mV.

The bootstrap driver introduces a voltage drop due to MOSFET R_{DSON} (typical value: 100Ω). The following equation is useful to compute the voltage drop on the bootstrap MOSFET:

$$V_{DROP} = I_{CHARGE} \bullet R_{DSON} \rightarrow V_{DROP} = \frac{Q_{GATE}}{T_{CHARGE}} \bullet R_{DSON} \tag{5}$$

where Q_{GATE} is the gate charge of the external MOSFET, R_{DSON} is the on resistance of the bootstrap MOSFET, and T_{CHARGE} is the charging time of the bootstrap capacitor.

For example: If Q_{GATE} is 24nC and T_{CHARGE} is 10µs, the drop on the bootstrap MOSFET is about 0.24V.

$$V_{DROP} = \frac{24nC}{10\mu s} \bullet 100\Omega = 0.24V \tag{6}$$

Protections: The FAN7316 has several protections: Open-Lamp Regulation (OLR), Arc Protection, Open-Lamp Protection (OLP), Short-Circuit Protection (SCP), CMP-High Protection, and Thermal Shutdown (TSD). All protections are latch-mode protections. The latch is reset when V_{IN} falls to the UVLO voltage or ENA is pulled down to GND.

Open-Lamp Regulation: When a voltage higher than 2V is applied to the OLR pin, the IC enters regulation mode and controls CMP voltage. The IC limits the lamp voltage by decreasing CMP source current. If the OLR voltage is higher than 1.75V, CMP source current decreases from 100µA to 1.6µA. If the OLR voltage reaches at 2V, CMP source current decreases to 0µA, so CMP voltage remains constant and the lamp voltage also remains constant, as shown in Figure 37. At the same time, the counter based on BCT time starts counting 450 cycles and 32 cycles at striking mode and normal mode, respectively, then the IC enters shutdown, as shown in Figure 38 and Figure 39.

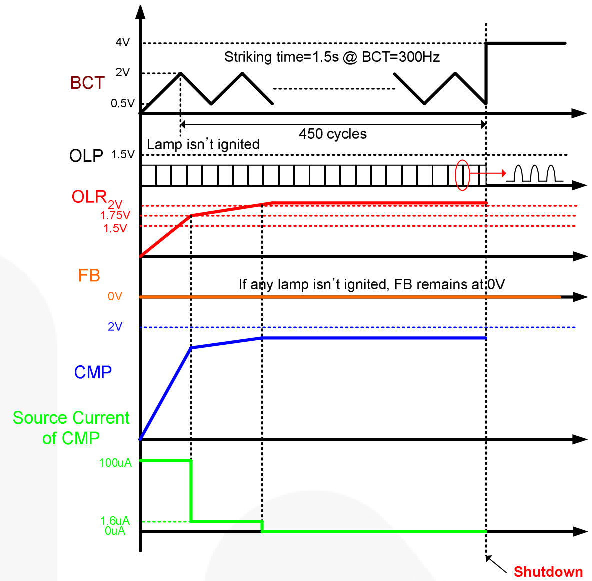


Figure 37. Open-Lamp Regulation in Striking Mode

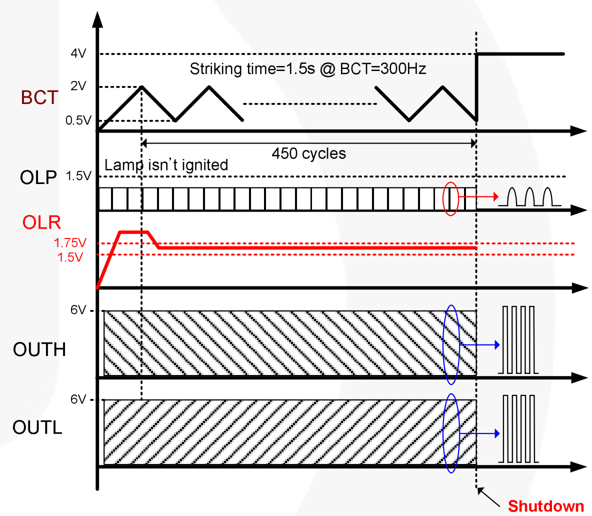


Figure 38. Open-Lamp Regulation in Striking Mode

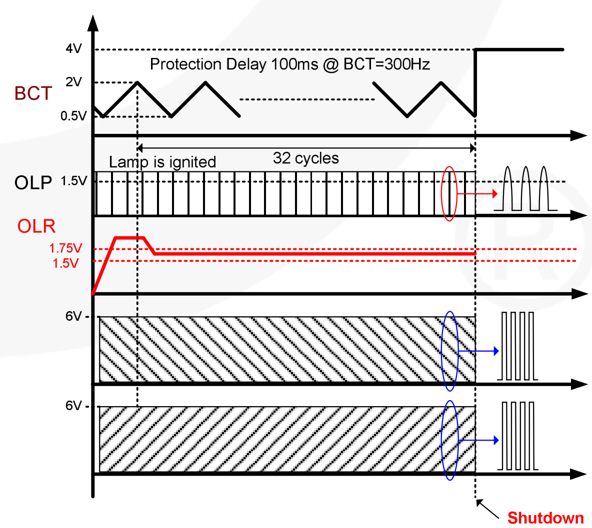


Figure 39. Open-Lamp Regulation in Normal Mode

Arc Protection: If OLR voltage is higher than 3V, the IC enters shutdown mode after a delay of two CT cycles, as shown in Figure 40.

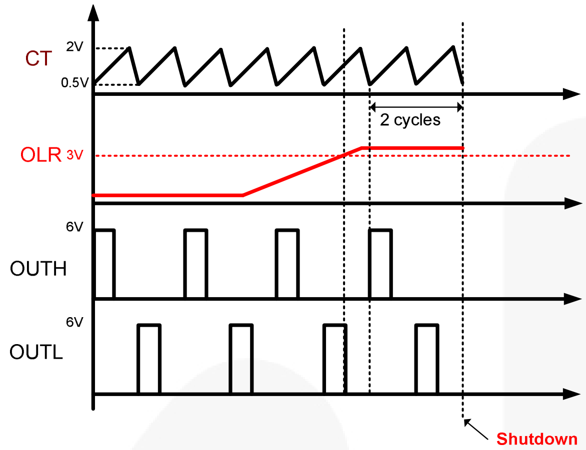


Figure 40. Arc Protection

Open-Lamp Protection: If OLP is lower than 1.5V at initial operation, the IC operates at striking mode for BCT 450 cycles, as shown in Figure 41. If OLP is lower than 1.5V at normal mode, the IC is shut down after a delay of three BCT cycles, as shown in Figure 42.

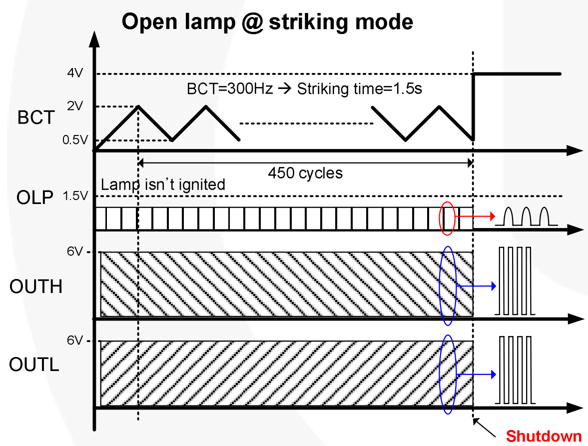


Figure 41. Open-Lamp Protection in Striking Mode

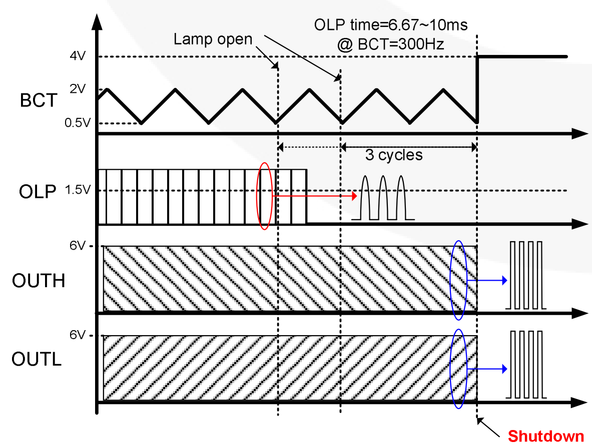


Figure 42. Open-Lamp Protection in Normal Mode

Short-Circuit Protection: If SCP is higher than 2V, the counter based on BCT time starts counting 450 cycles and 32 cycles at striking mode and normal mode, respectively, then the IC enters shutdown, as shown in Figure 43 and Figure 44.

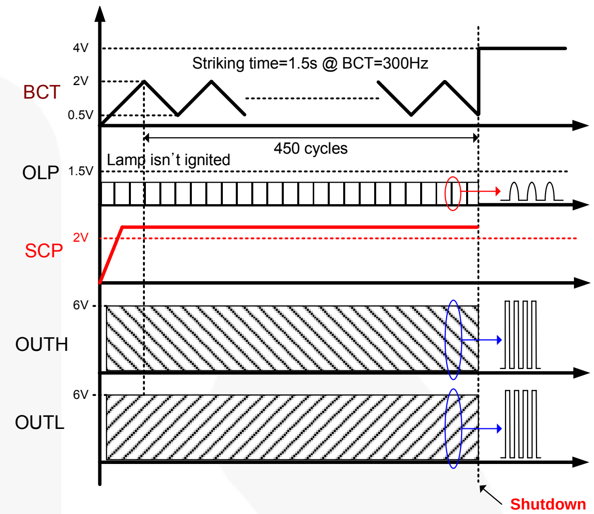


Figure 43. Short-Circuit Protection in Striking Mode

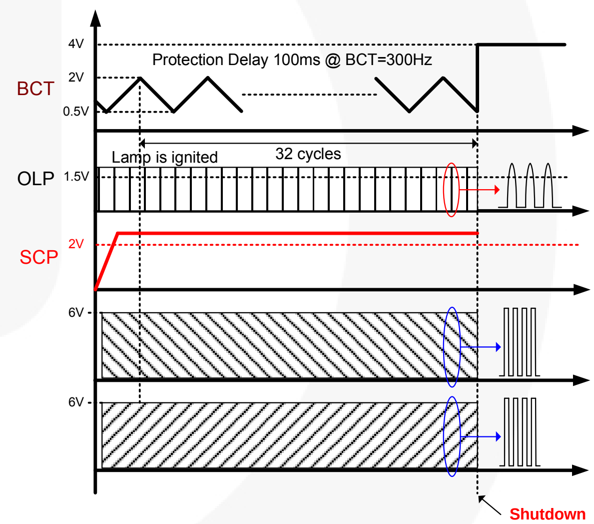


Figure 44. Short-Circuit Protection in Normal Mode

CMP-High Protection: If CMP is higher than 3V, the counter based on BCT time starts counting 450 cycles and 32 cycles at striking mode and normal mode, respectively, then the IC enters shutdown, as shown in Figure 45 and Figure 46.

CMP-High Protection: If CMP is higher than 3V, the counter based on BCT time starts counting 450 cycles and 32 cycles at striking mode and normal mode, respectively, then the IC enters shutdown, as shown in Figure 45 and Figure 46.

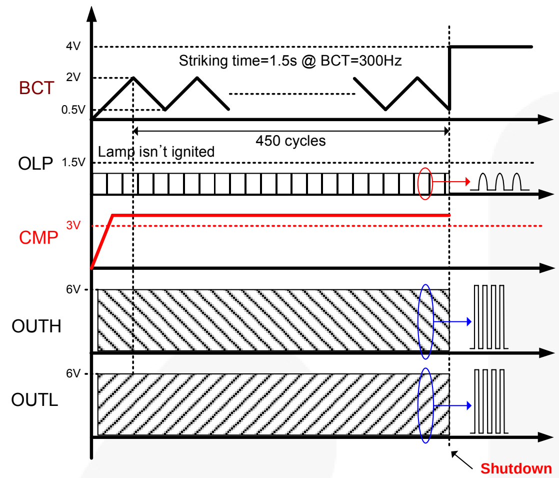


Figure 45. CMP-High Protection in Striking Mode

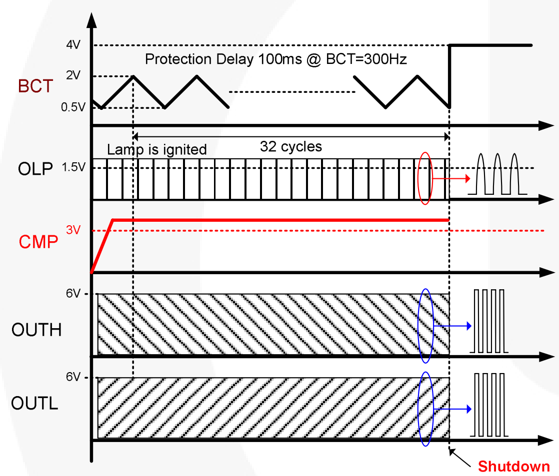


Figure 46. CMP-High Protection in Normal Mode

Thermal Shutdown: The IC provides the function to detect the abnormal over-temperature. If the IC temperature exceeds approximately 150°C, the thermal shutdown triggers.

Typical Application Circuit (LCD Backlight Inverter)

Application	Device	Input Voltage Range	Number of lamps
19-Inch LCD Monitor	FAN7316	14.5±10%	4

1. Features

- High-Efficiency Single-Stage Power Conversion
- N-N Half-Bridge Topology
- Reduces Required External Components
- Enhanced System Reliability through Protection Functions

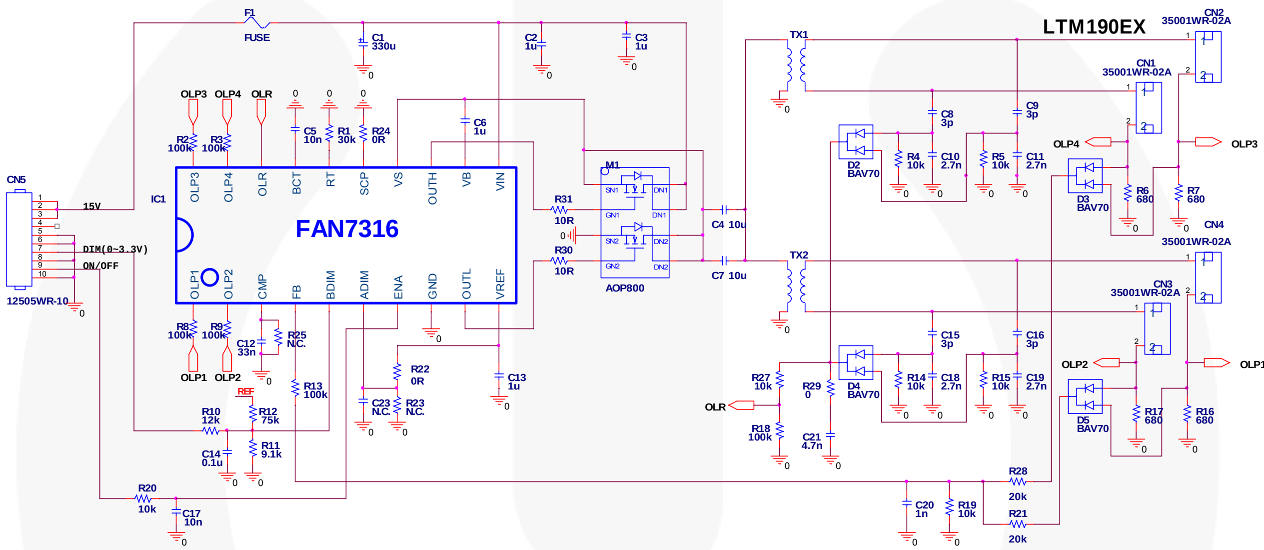


Figure 47. Typical Application Circuit

2. Transformer Schematic Diagram

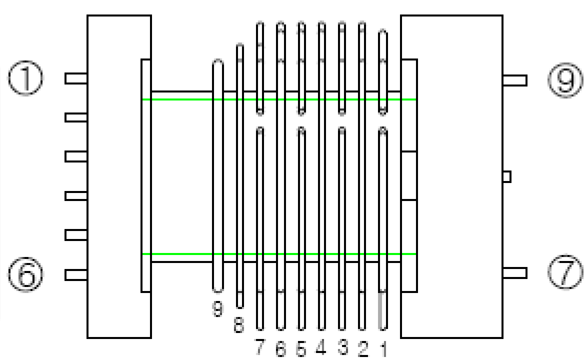


Figure 48. Transformer Schematic Diagram

3. Core & Bobbin

- Core: EFD2126
- Material: PL7
- Bobbin: EFD2126

4. Winding Specification

Pin No.	Wire	Turns	Inductance	Leakage Inductance	Remarks
5 → 2	1 UEW 0.45ϕ	12	94µH	9.1µH	1kHz, 1V
7 → 9	1 UEW 0.04ϕ	2560(=0+360•7)	3.88H	420mH	1kHz, 1V

5. BOM of the Application Circuit

Part Ref.	Value	Description	Part Ref.	Value	Description
Fuse			C5	10nF	50V 1608 K
F1	24V 3A	FUSE	C6	1µF	50V 2012 K
Resistor (SMD)			C7	10µF	16V 3216
R1	30k	1608 F	C10	2.7nF	50V 1608 K
R2	100k	1608 J	C11	2.7nF	50V 1608 K
R3	100k	1608 J	C12	33nF	50V 1608 K
R4	10k	1608 F	C13	1µF	50V 3216 K
R5	10k	1608 F	C14	10nF	50V 1608 K
R6	680	1608 F	C17	10nF	50V 1608 K
R7	680	1608 F	C18	2.7nF	50V 1608 K
R8	100k	1608 J	C19	2.7nF	50V 1608 K
R9	100k	1608 J	C20	1nF	50V 1608 K
R10	12k	1608 F	C21	4.7nF	50V 1608 K
R11	9.1k	1608 F	C23	NC	
R12	75k	1608 F	**Capacitor (DIP)**		
R13	100k	1608 J	C8	3p	3KV
R14	10k	1608 F	C9	3p	3KV
R15	10k	1608 F	C15	3p	3KV
R16	680	1608 F	C16	3p	3KV
R17	680	1608 F	**Diode (SMD)**		
R18	100k	1608 F	D2	BAV70	Fairchild Semiconductor
R19	10k	1608 F	D3	BAV70	Fairchild Semiconductor
R20	10k	1608 J	D4	BAV70	Fairchild Semiconductor
R21	20k	1608 F	D5	BAV70	Fairchild Semiconductor
R22	0		**Electrolytic capacitor**		
R23	NC		C1	330µ	25V
R24	0		**MOSFET (SMD)**		
R25	NC		M1	AOP800	Alpha & Omega
R27	10k	1608 F	**Wafer (SMD)**		
R28	20k	1608 F	CN1	35001WR-02A	
R29	0		CN2	35001WR-02A	
R30	10	1608 J	CN3	35001WR-02A	
R31	10	1608 J	CN4	35001WR-02A	
Capacitor (SMD)			CN5	12505WR-10	
C2	1µF	50V 3216 K	**Transformer (DIP)**		
C3	1µF	50V 3216 K	TX1		EFD2126
C4	10µF	16V 3216	TX2		EFD2126

Physical Dimensions

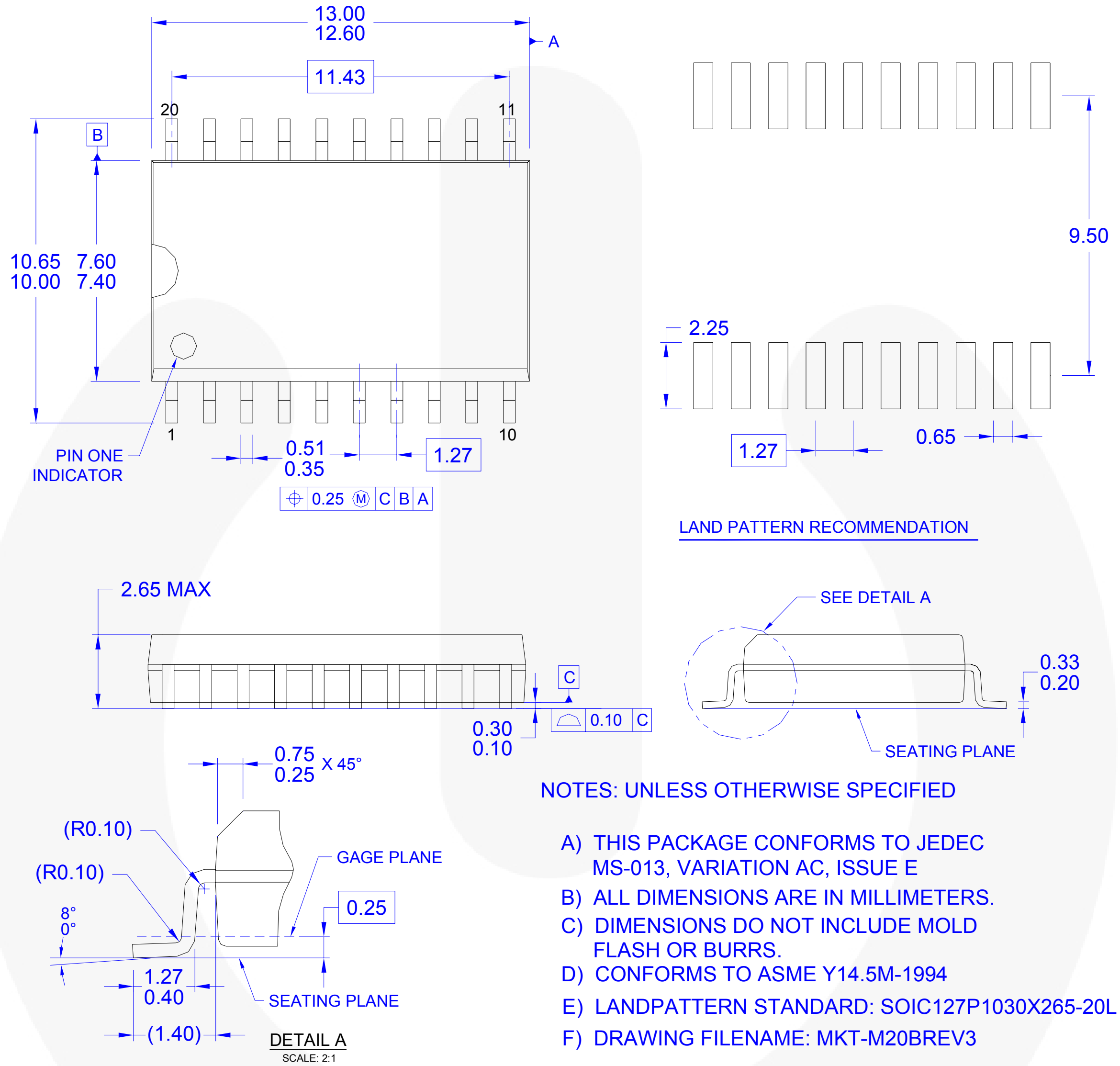


Figure 49. 20-SOIC Package

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