September 2014



FNA51060T3 Motion SPM[®] 55 Series

Features

- UL Certified No. E209204 (UL1557)
- 600 V 10 A 3-Phase IGBT Inverter Including Control IC for Gate Drive and Protections
- Low-Loss, Short-Circuit Rated IGBTs
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Active-HIGH interface, works with 3.3 / 5 V Logic, Schmitt-trigger Input
- HVIC for Gate Driving, Under-Voltage and Short-Circuit Current Protection
- Fault Output for Under-Voltage and Short-Circuit Current Protection
- Inter-Lock Function to Prevent Short-Circuit
- Shut-Down Input
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- Optimized for 5 kHz Switching Frequency
- Isolation Rating: 1500 V_{rms} / min.

Applications

Motion Control - Home Appliance / Industrial Motor

Related Resources

General Description

FNA51060T3 is a Motion SPM 55 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, inter-lock function, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's robust short-circuit-rated IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.



Figure 1. 3D Package Drawing (Click to Activate 3D Content)

Package Marking and Ordering Information

Device	Device Marking	Package	Packing Type	Quantity
FNA51060T3	FNA51060T3	SPMFA-A20	RAIL	13

Integrated Power Functions

• 600 V - 10 A IGBT inverter for three phase DC / AC power conversion (Please refer to Figure 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting
 control circuit Under-Voltage Lock-Out (UVLO) protection
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: High-active interface, works with 3.3 / 5 V logic, Schmitt trigger input

Pin Configuration

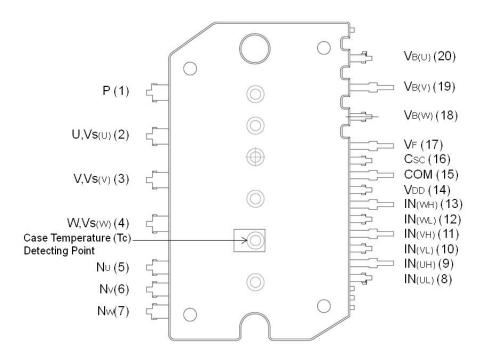


Figure 2. Top View

FNA51060T
F3 Motion
SPM® 55
5 Series

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	Р	Positive DC-Link Input
2	U, V _S (U)	Output for U Phase
3	V, V _S (V)	Output for V Phase
4	W, V _S (W)	Output for W Phase
5	NU	Negative DC-Link Input for U Phase
6	N _V	Negative DC-Link Input for V Phase
7	N _W	Negative DC-Link Input for W Phase
8	IN _(UL)	Signal Input for Low-Side U Phase
9	IN _(UH)	Signal Input for High- ide U Phase
10	IN _(VL)	Signal Input for Low-Side V Phase
11	IN _(VH)	Signal Input for High-Side V Phase
12	IN _(WL)	Signal Input for Low-Side W Phase
13	IN _(WH)	Signal Input for High-Side W Phase
14	V _{DD}	Common Bias Voltage for IC and IGBTs Driving
15	СОМ	Common Supply Ground
16	C _{SC}	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
17	V _F	Fault Output, Shut-Down Input, Temperature Output of Drive IC
18	V _{B(W)}	High-Side Bias Voltage for W-Phase IGBT Driving
19	V _{B(V)}	High-Side Bias Voltage for V-Phase IGBT Driving
20	V _{B(U)}	High-Side Bias Voltage for U-Phase IGBT Driving

Internal Equivalent Circuit and Input/Output Pins

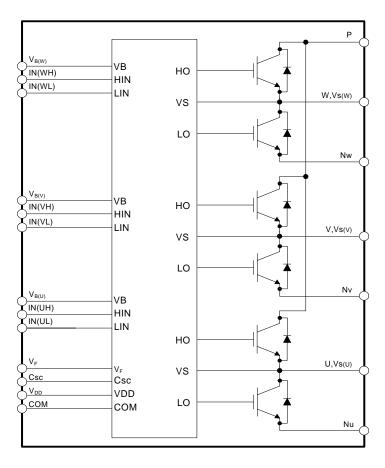


Figure 3. Internal Block Diagram

Note:

- 1. Inverter high-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT.
- 2. Inverter low-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
- 3. Single drive IC has gate driver for six IGBTs and protection functions.
- 4. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Absolute Maximum Ratings (T_J = 25°C, unless otherwise specified.)

Inverter Part

Symbol	Parameter	Conditions	Rating	Unit
V _{PN}	Supply Voltage	Applied between P - N _U , N _V , N _W	450	V
V _{PN(Surge)}	Supply Voltage (Surge) Applied between P - N _U , N _V , N _W		500	V
V _{CES}	Collector - Emitter Voltage		600	V
± I _C	Each IGBT Collector Current	$T_{C} = 25^{\circ}C, T_{J} < 150^{\circ}C$	10	А
± I _{CP}	Each IGBT Collector Current (Peak)	$T_{C} = 25^{\circ}C, T_{J} < 150^{\circ}C, Under 1 ms Pulse Width$	20	A
P _C	Collector Dissipation	T _C = 25°C per Chip	22	W
TJ	Operating Junction Temperature	(Note 5)	-40 ~ 150	°C

Note:

5. The maximum junction temperature rating of the power chips integrated within the Motion SPM $^{\otimes}$ 55 product is 150°C.

Control Part

Symbol	Parameter	Conditions	Rating	Unit
V _{DD}	Control Supply Voltage	Applied between V _{DD} - COM	20	V
V _{BS}	High-Side Control Bias Voltage	Applied between V_B(U) - V_S(U), V_B(V) - V_S(V), V_B(W) - V_S(W)	20	V
V _{IN}	Input Signal Voltage	$\begin{array}{llllllllllllllllllllllllllllllllllll$	-0.3 ~ V _{DD} +0.3	V
V _F	Fault Supply Voltage	Applied between V _F - COM	-0.3 ~ V _{DD} +0.3	V
۱ _F	Fault Current	Sink Current at V _F pin	5	mA
V _{SC}	Current Sensing Input Voltage	Applied between C _{SC} - COM	-0.3 ~ V _{DD} +0.3	V

Total System

Symbol	Parameter	Conditions	Rating	Unit
V _{PN(PROT)}	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{DD} = V_{BS} = 13.5 \sim 16.5 V$ T _J = 150°C, Non-Repetitive, < 2 µs	400	V
T _{STG}	Storage Temperature		-40 ~ 125	°C
V _{ISO}	Isolation Voltage Connect Pins to Heat Sink Plate	AC 60 Hz, Sinusoidal, 1 Minute	1500	V _{rms}

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
R _{th(j-c)Q}	Junction to Case Thermal Resistance	Inverter IGBT part (per 1 / 6 module)	-	-	5.6	°C / W
R _{th(j-c)F}		Inverter FWD part (per 1 / 6 module)	-	-	6.9	°C / W

Note:

6. For the measurement point of case temperature (T $_{\rm C}$), please refer to Figure 2.

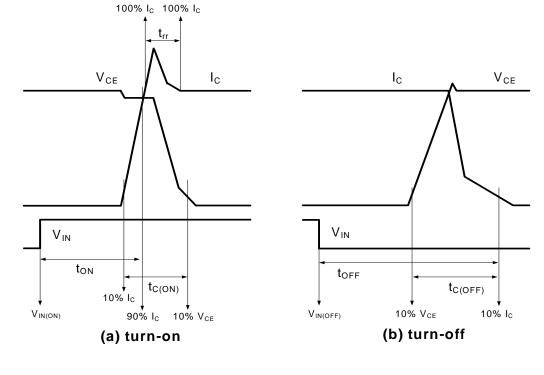
Electrical Characteristics (T_J = 25°C, unless otherwise specified.)

Inverter Part

S	ymbol	Parameter	Con	ditions	Min.	Тур.	Max.	Unit
V _{CE(SAT)}		Collector - Emitter Saturation Voltage	$V_{DD} = V_{BS} = 15 \text{ V}$ $T_J = 25^{\circ}\text{C}$ $V_{IN} = 5 \text{ V}$		-	1.45	1.85	V
			$I_{C} = 10 \text{ A}$ $T_{J} = 150^{\circ}\text{C}$ $V_{IN} = 0 \text{ V}$ $I_{E} = 10 \text{ A}$ $T_{J} = 25^{\circ}\text{C}$ $I_{E} = 10 \text{ A}$		-	1.65	-	V
	V _F	FWDi Forward Voltage V		$T_J = 25^{\circ}C$	-	1.85	2.3	V
			I _F = 10 A	T _J = 150°C	-	1.75	-	V
HS	t _{ON}	Switching Times	$V_{PN} = 400 \text{ V}, V_{DD} = V_{PN}$	/ _{BS} = 15 V, I _C = 10A	-	700	-	ns
	t _{C(ON)}		$T_J = 25^{\circ}C$ $V_{IN} = 0 V \leftrightarrow 5 V$, Indu	uctive load	-	170	-	ns
	t _{OFF}		(Note 7)		-	800	-	ns
	t _{C(OFF)}				-	150	-	ns
	t _{rr}				-	90	-	ns
LS	t _{ON}		$V_{PN} = 400 \text{ V}, \text{ V}_{DD} = V_{PN}$	/ _{BS} = 15 V, I _C = 10A	-	750	-	ns
	t _{C(ON)}		$T_J = 25^{\circ}C$ $V_{IN} = 0 V \leftrightarrow 5 V$, Indu	uctive load	-	250	-	ns
	t _{OFF}		(Note 7) $\sim 3^{\circ}$ (Note 7)		-	800	-	ns
	t _{C(OFF)}				-	100	-	ns
	t _{rr}				-	80	-	ns
	I _{CES}	Collector - Emitter Leakage Current	V _{CE} = V _{CES}		-	-	1	mA

Note:

7. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. t_{C(ON)} and t_{C(OFF)} are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.



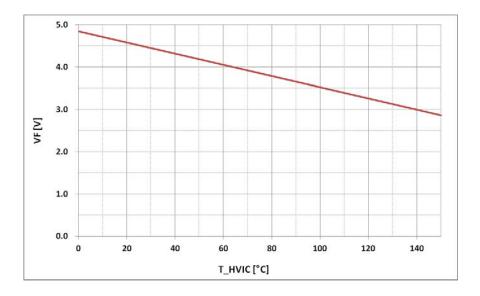


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Symbol	Parameter	Conditions		Min.	Тур.	Max.	Unit
I _{QDD}	Quiescent V _{DD} Supply Current	V_{DD} = 15 V, IN _(UH,VH,WH,UL,VL,WL) = 0 V	V _{DD} - COM	-	2.3	3.4	mA
I _{PDD}	Operating V _{DD} Supply Current	V_{DD} = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input	V _{DD} - COM	-	2.7	4.0	mA
I _{QBS}	Quiescent V _{BS} Supply Current	$V_{BS} = 15 \text{ V}, \text{ IN}_{(UH, VH, WH)} = 0 \text{ V}$	V _{B(U)} - V _{S(U)} , V _{B(V)} - V _{S(V)} , V _{B(W)} - V _{S(W)}	-	60	100	μΑ
I _{PBS}	Operating V _{BS} Supply Current	$V_{DD} = V_{BS} = 15 \text{ V}, f_{PWM} = 20 \text{ kHz},$ duty = 50%, applied to one PWM signal input for high - side		-	430	600	μA
V _{FH}	Fault Output Voltage	$V_{SC} = 0 \text{ V}, \text{ V}_{F} \text{ Circuit: 4.7 k}\Omega \text{ to 5 V Pull-up}$		4.5	-	-	V
V _{FL}		V_{SC} = 1 V, V _F Circuit: 4.7 k Ω to 5 V Pull-up		-	-	0.5	V
V _{SC(ref)}	Short-Circuit Trip Level	V _{DD} = 15 V (Note 4)		0.45	0.5	0.55	V
UV _{DDD}		Detection level Reset level Detection level		10.0	11.5	13.0	V
UV_DDR	Supply Circuit Under-Voltage			10.5	12.0	13.5	V
UV _{BSD}	Protection			9.5	11.0	12.5	V
UV _{BSR}		Reset level		10.0	11.5	13.0	V
I _{FT}	HVIC Temperature Sensing Current	$V_{DD} = V_{BS} = 15 \text{ V}, \text{ T}_{HVIC} = 25^{\circ}\text{C}$		70	95	120	μA
V_{FT}	HVIC Temperature Sensing Voltage	$V_{DD} = V_{BS} = 15 \text{ V}, \text{ T}_{HVIC} = 25^{\circ}\text{C}, 4.$ (Figure. 5)	7 k Ω to 5 V Pull-up	-	4.55		>
t _{FOD}	Fault-Out Pulse Width			40	100	-	μs
V _{FSDL}	Shut-down Low Input	Applied between V _F - COM		-	-	2.4	V
V _{FSDH}	Shut-down High Input			0.8	-	-	V
V _{IN(ON)}	ON Threshold Voltage	Applied between IN(UH), IN(VH), II	$N_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$,	-	-	2.4	V
V _{IN(OFF)}	OFF Threshold Voltage	IN _(WL) - COM		0.8	-	-	V

Note:

8. Short-circuit protection is functioning for all six IGBTs.



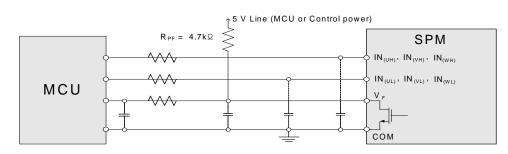


Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
V _{PN}	Supply Voltage	Applied between P - N _U , N _V , N _W	-	300	400	V
V _{DD}	Control Supply Voltage	Applied between V _{DD} - COM	14.0	15	16.5	V
V _{BS}	High - Side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}, \ V_{B(V)}$ - $V_{S(V)}, \ V_{B(W)}$ - $V_{S(W)}$	13.0	15	18.5	V
dV _{DD} / dt, dV _{BS} / dt	Control Supply Variation		-1	-	1	V/μs
t _{dead}	Blanking Time for Preventing Arm - Short	For each input signal	0.5	-	-	μs
f _{PWM}	PWM Input Signal	$-40^{\circ}C < T_{J} < 150^{\circ}C$	-	-	20	kHz
V _{SEN}	Voltage for Current Sensing	Applied between N _U , N _V , N _W - COM (Including surge voltage)	-4		4	V
P _{WIN(ON)}	Minimun Input Pulse	(Note 9)	0.7	-	-	μs
P _{WIN(OFF)}	Width		0.7	-	-	

Note:

9. This product might not make response if input pulse width is less than the recommanded value.



Note:

10. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the SPM 55 product integrates 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 6. Recommended MCU I/O Interface Circuit

Mechanical Characteristics and Ratings

Parameter	Co	Conditions			Max.	Unit
Device Flatness	See Figure 7	See Figure 7		-	100	μm
Mounting Torque	Mounting Screw: - M3	Recommended 0.7 N • m	0.6	0.7	0.8	N • m
	Note Figure 8	Recommended 7.1 kg • cm	5.9	6.9	7.9	kg • cm
Weight			-	6.0	-	g

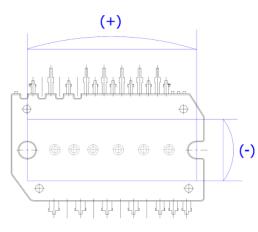


Figure 7. Flatness Measurement Position

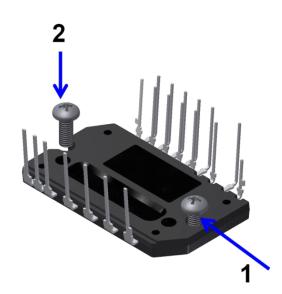


Figure 8. Mounting Screws Torque Order

Note:

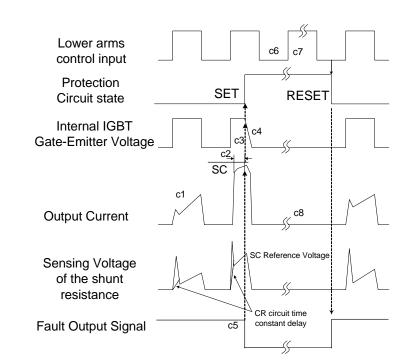
11. Do not make over torque when mounting screws. Much mounting torque may cause package cracks, as well as bolts and Al heat-sink destruction.

12. Avoid one side tightening stress. Figure 10 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the Motion SPM 55 product to be damaged. The Pre-screwing torque is set to 20 ~ 30 % of maximum torque rating.

Time Charts of Protective Function Input Signal Protection RESET SET RESET **Circuit State** UVDDI a1 af Control a3 Supply Voltage a2 a7 a4 **Output Current** a5 Fault Output Signal a1 : Control supply voltage rises: After the voltage rises UV_{DDR}, the circuits start to operate when next input is applied. a2 : Normal operation: IGBT ON and carrying current. a3 : Under voltage detection (UV_{DDD}). a4 : IGBT OFF in spite of control input condition. a5 : Fault output operation starts. a6 : Under voltage reset (UV_{DDR}). a7 : Normal operation: IGBT ON and carrying current. Figure 9. Under-Voltage Protection (Low-Side) Input Signal Protection RESET RESET SET **Circuit State** b5 b1 Control UVBSD b3 Supply Voltage b6 b2 b4 **Output Current** High-level (no fault output) 55 Fault Output Signal b1 : Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied. b2 : Normal operation: IGBT ON and carrying current. b3 : Under voltage detection (UV_{BSD}). b4 : IGBT OFF in spite of control input condition, but there is no fault output signal. b5 : Under voltage reset (UV_{BSR})

b6 : Normal operation: IGBT ON and carrying current

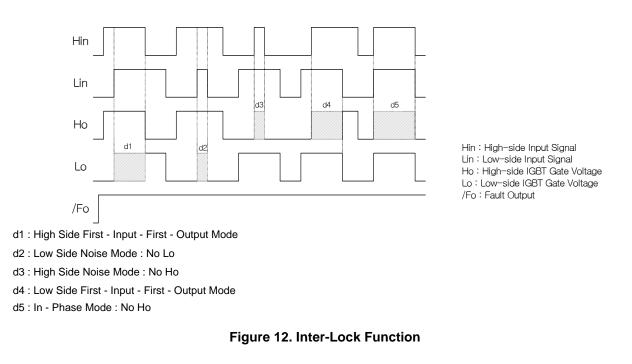
Figure 10. Under-Voltage Protection (High-Side)



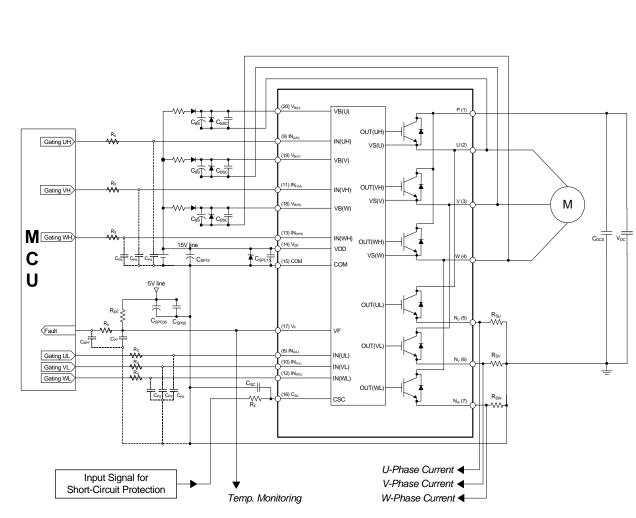
(with the external shunt resistance and CR connection)

- c1 : Normal operation: IGBT ON and carrying current.
- c2 : Short circuit current detection (SC trigger).
- c3 : Hard IGBT gate interrupt.
- c4 : IGBT turns OFF.
- c5 : Input "L" : IGBT OFF state.
- c6 : Input "H": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.
- c7 : IGBT OFF state





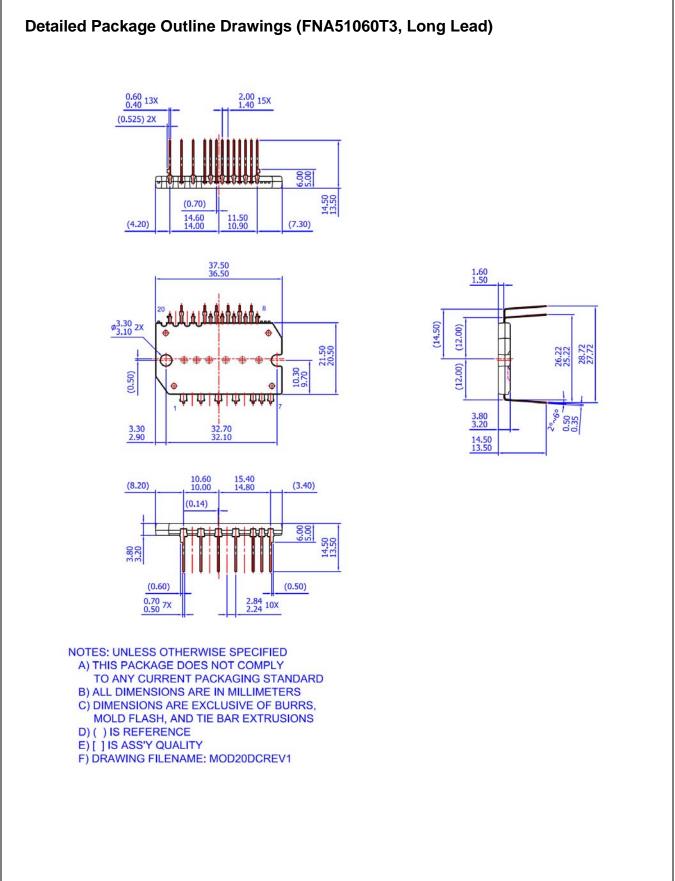
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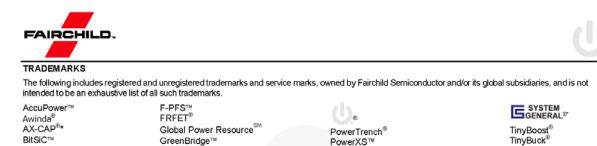


Note:

- 1) To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 ~ 3 cm)
- 2) By virtue of integrating an application specific type of HVIC inside the SPM[®] 55 product, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3) V_F is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 5 mA. Please refer to Figure 14.
- 4) C_{SP15} of around seven times larger than bootstrap capacitor C_{BS} is recommended.
- 5) Input signal is active-HIGH type. There is a 5 k Ω resistor inside the IC to pull down each input signal line to GND. RC coupling circuits is recommanded for the prevention of input signal oscillation. R_SC_{PS} time constant should be selected in the range 50 ~ 150 ns. (Recommended R_S = 100 , C_{PS} = 1 nF)
- 6) To prevent errors of the protection function, the wiring around ${\sf R}_{\sf F}$ and ${\sf C}_{\sf SC}$ should be as short as possible.
- 7) In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 1.5 ~ 2 µs.
- 8) The connection between control GND line and power GND line which includes the N_U, N_V, N_W must be connected to only one point. Please do not connect the control GND to the power GND by the broad pattern. Also, the wiring distance between control GND and power GND should be as short as possible.
- 9) Each capacitor should be mounted as close to the pins of the Motion SPM 55 product as possible.
- 10) To prevent surge destruction, the wiring between the smoothing capacitor and the P and GND pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P and GND pins is recommended.
- 11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.
- 12) The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals. (Recommanded zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15)
- 13) Please choose the electrolytic capacitor with good temperature characteristic in C_{BS}. Also, choose 0.1 ~ 0.2 μ F R-category ceramic capacitors with good temperature and frequency characteristics in C_{BSC}.
- 14) For the detailed information, please refer to the application notes.

Figure 13. Typical Application Circuit





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FACT [®] FAST [®] FastvCore™ FETBench™ FPS™	MotionGrid [®] MTi [®] MTx [®] MVN [®] mWSaver [®] OptoHIT™	SuperSC SuperSC SupreMu SyncFE	SuperSOT™-3 SuperSOT™-8 SupreMOS [®] SyncFET™ Sync-Lock™

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