

FAN53526

3.0 A, 2.4 MHz, Digitally Programmable TinyBuck[®] Regulator

Descriptions

The FAN53526 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5 V to 5.5 V. The output voltage is programmed through an I²C interface capable of operating up to 3.4 MHz.

Using a proprietary architecture with synchronous rectification, the FAN53526 is capable of delivering 3.0 A continuous at over 80% efficiency, maintaining that efficiency at load currents as low as 10 mA. The regulator operates at a nominal fixed frequency of 2.4 MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power-Save Mode with a typical quiescent current of 50 μ A at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 2.4 MHz. In Shutdown Mode, the supply current drops below 1 μ A, reducing power consumption. PFM Mode can be disabled if fixed frequency is desired. The FAN53526 is available in a 15-bump, 1.310 mm x 2.015 mm, 0.4 mm ball pitch WLCSP.

Features

- Fixed-Frequency Operation: 2.4 MHz
- Best-in-Class Load Transient
- Continuous Output Current Capability: 3.0 A
- 2.5 V to 5.5 V Input Voltage Range
- Digitally Programmable Output Voltage:
 - ◆ -0.600 V to 1.39375 V in 6.25 mV Steps
- Programmable Slew Rate for Voltage Transitions
- I²C-Compatible Interface Up to 3.4 Mbps
- PFM Mode for High Efficiency in Light-Load
- Quiescent Current in PFM Mode: 50 μ A (Typical)
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 15-Bump Wafer-Level Chip Scale Package (WLCSP)

Applications

- Application, Graphic, and DSP Processors
 - ◆ ARM[™], Tegra[™], OMAP[™], NovaThor, ARMADA[™], Krait[™], etc.
- Hard Disk Drives, LPDDR3, LPDDR4
- Tablets, Netbooks, Ultra-Mobile PCs
- Smart Phones
- Gaming Devices



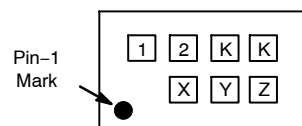
ON Semiconductor[®]

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WLCSP-15
CASE 567QS

MARKING DIAGRAM



- 1, 2 = Two Alphanumeric Characters for Device Mark
- KK = Two Alphanumeric Characters for Lot Rune Code Mark
- . = Pin 1 Indicator
- X = Alphabetical Year Code
- Y = 2-weeks Date Code
- Z = Assembly Plant Code

PIN CONFIGURATION

| | | |
|------------|------------|------------|
| VIN A1 | SW A2 | PGND A3 |
| B1 | B2 | B3 |
| C1 | PGND C2 | AGND C3 |
| VSEL D1 | EN D2 | SDA D3 |
| AGND E1 | SCL E2 | VOUT E3 |

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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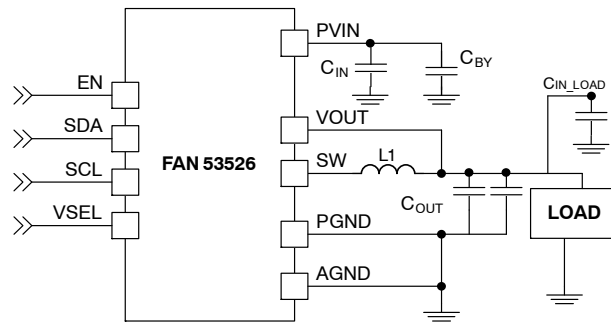


Figure 1. Typical Application

Table 1. ORDERING INFORMATION

| Part Number | Power-Up Defaults | | DVS Range / Step Size | I ² C Slave Address | Temperature Range | Package | Packing Method | Device Marking |
|----------------|-------------------|---------|--------------------------------|--------------------------------|-------------------|---------|----------------|----------------|
| | VSEL0 | VSEL1 | | | | | | |
| FAN53526UC84X | 1.125 | 1.125 | 0.600 V to 1.39375 V / 6.25 mV | C0 | -40 to 85°C | WLCSP | Tape & Reel | F7 |
| FAN53526UC89X | 1.15625 | 1.15625 | | | | | | CL |
| FAN53526UC100X | 1.225 | 1.225 | | | | | | F9 |
| FAN53526UC106X | 1.2625 | 1.2625 | | | | | | C7 |
| FAN53526UC128X | 1.20 | 1.20 | | | | | | F3 |
| FAN53526UC00X | 0.60 | 0.60 | | | | | | GA |
| FAN53526UC64X | 1.00 | 1.00 | | | | | | GG |
| FAN53526UC88X | 1.15 | 1.15 | | | | | | LM |
| FAN53526UC288X | 1.15 | 1.15 | | | | | | LN |
| FAN53526UC168X | 1.125 | 1.125 | | C2 | | | | FR |

RECOMMENDED EXTERNAL COMPONENTS

Table 2. RECOMMENDED EXTERNAL COMPONENTS FOR 3.0 A MAXIMUM LOAD CURRENT

| Component | Description | Vendor | Parameter | Typ. | Unit |
|--|----------------------------------|-----------------------------|-----------|------|------|
| L1 | 330 nH, 2016 Case Size | See Table 3 | C | 47 | μF |
| L1 Alternative (Note 1) | 470 nH 2016 Case Size | | | | |
| C _{OUT1} , C _{OUT2} | 47 μF, 6.3 V, X5R, 0603 | GRM188R60J476ME15 (Murata) | C | 47 | |
| C _{OUT1} , C _{OUT2} Alternative (Note 1) | 22 μF, 10 V, X5R, 0603 | CL10A226MP8NUNB (SAMSUNG) | C | 22 | |
| C _{IN} | 1 Piece; 4.7 μF, 10 V, X5R, 0603 | C1608X5R1A475K (TDK) | C | 4.7 | |
| C _{BY} | 1 Piece; 100 nF, 6.3V, X5R, 0201 | GRM033R60J104KE19D (Murata) | C | 100 | nF |

1. C_{OUT} Alternative and L1 Alternative can be used if not following reference design. C_{BY} is recommended to reduce any high frequency component on VIN bus. C_{BY} is optional and used to filter any high frequency component on VIN bus.

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Table 3. RECOMMENDED INDUCTORS

| Manufacturer | Part # | L (nH) | DCR (mΩ Typ.) | I _{SAT} (Note 2) | L | W | H |
|--------------|---------------------|--------|---------------|---------------------------|-----|-----|-----|
| Toko | DFE201612E-R33N | 330 | 15 | 7.0 | 2.0 | 1.6 | 1.2 |
| Toko | DFE201612E-R47N | 470 | 21 | 6.1 | 2.0 | 1.6 | 1.2 |
| Cyntek | PIFE20161B-R47MS-39 | 470 | 30 | 3.1 | 2.0 | 1.6 | 1.2 |
| SEMCO | CIGT201610UMR47MNE | 470 | 30 | 4.0 | 2.0 | 1.6 | 0.9 |
| SEMCO | CIGT201610UMR47MNE | 470 | 33 | 3.0 | 2.0 | 1.2 | 0.9 |

2. I_{SAT} where the dc current drops the inductance by 30%.

PIN CONFIGURATION

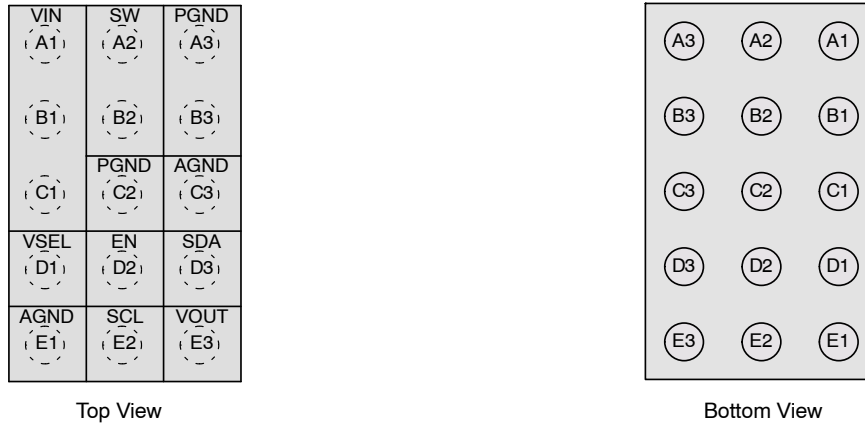


Figure 2. Pin Configuration

Table 4. PIN DEFINITIONS

| Pin # | Name | Description |
|------------|------|--|
| D1 | VSEL | Voltage Select. When this pin is LOW, V _{OUT} is set by the VSEL0 register. When this pin is HIGH, V _{OUT} is set by the VSEL1 register. Polarity of pin in conjunction with the MODE bits in the Control register 02h, will select Forced PWM or Auto PFM/PWM mode of operation. VSEL0=Auto PFM, and VSEL1=FPWM. The VSEL pin has an internal pull-down resistor (250kΩ), which is only activated with a logic low. |
| D2 | EN | Enable. The device is in Shutdown Mode when this pin is LOW. Device keeps register content when EN pin is LOW. The EN Pin has an internal pull-down resistor (250kΩ), which is only activated with a logic low. |
| E2 | SCL | I ² C Serial Clock |
| D3 | SDA | I ² C Serial Data |
| E3 | VOUT | VOUT. Sense pin for V _{OUT} . Connect to C _{OUT} . |
| A3, B3, C2 | PGND | Power Ground. The low-side MOSFET is referenced to this pin. C _{IN} and C _{OUT} should be returned with a minimal path to these pins. |
| C3, E1 | AGND | Analog Ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin. |
| A1, B1, C1 | VIN | Power Input Voltage. Connect to the input power source. Connect to C _{IN} with minimal path. |
| A2, B2 | SW | Switching Node. Connect to the inductor. |

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In

addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Parameter | Min | Max | Unit |
|------------------------|--|------------------|------|--------------------------|------|
| V _{IN} | Voltage on SW, VIN Pins | IC Not Switching | -0.3 | 7.0 | V |
| | | IC Switching | -0.3 | 6.5 | |
| | Voltage on EN Pin | | -0.3 | V _{IN} (Note 3) | |
| | Voltage on All Other Pins | IC Not Switching | -0.3 | V _{IN} (Note 3) | |
| V _{OUT} | Voltage on VOUT Pin | | -0.3 | 6.5 | V |
| V _{INOV_SLEW} | Maximum Slew Rate of V _{IN} > 6.5V, PWM Switching | | | 100 | V/ms |
| ESD | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | | 2000 | | V |
| | Charged Device Model per JESD22-C101 | | 1000 | | |
| T _J | Junction Temperature | | -40 | +150 | °C |
| T _{STG} | Storage Temperature | | -65 | +150 | °C |
| T _L | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

3. Lesser of 7V or V_{IN} + 0.3 V.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal

performance to the datasheet specifications. On Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------|------|------|------|------|
| V _{IN} | Supply Voltage Range | 2.5 | | 5.5 | V |
| I _{OUT} | Output Current | 0 | | 3.0 | A |
| T _A | Operating Ambient Temperature | -40 | | +85 | °C |
| T _J | Operating Junction Temperature | -40 | | +125 | °C |

Table 7. THERMAL PROPERTIES

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|---|------|------|------|------|
| θ _{JA} | Junction-to-Ambient Thermal Resistance (Note 4) | | 42 | | °C/W |

4. Junction-to-ambient thermal resistance is a function of application and board layout. This data is simulated with four-layer 2s2p boards with vias in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed the junction temperature

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ELECTRICAL CHARACTERISTICS

Table 8. ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at $V_{IN}=3.6\text{ V}$, $T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A=25^\circ\text{C}$, $V_{IN}=3.6\text{ V}$, and EN=HIGH. $V_{OUT} = 1.15625\text{ V}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|----------------------------------|--|------|------|------|---------------|
| Power Supplies | | | | | | |
| I_Q | Quiescent Current | $I_{LOAD}=0$ | | 50 | | μA |
| | | $I_{LOAD}=0$, MODE Bit=1 (Forced PWM) | | 15 | | mA |
| I_{SD} | H/W Shutdown Supply Current | EN=GND | | 0.1 | 3.0 | μA |
| | S/W Shutdown Supply Current | EN= V_{IN} , BUCK_ENx=0, $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ | | 2 | 12 | μA |
| V_{UVLO} | Under-Voltage Lockout Threshold | V_{IN} Rising | | 2.32 | 2.45 | V |
| V_{UVHYST} | Under-Voltage Lockout Hysteresis | | | 350 | | mV |

EN, VSEL, SDA, SCL

| | | | | | | |
|----------|--------------------------|--|-----|------|------|---------------|
| V_{IH} | high-Level Input Voltage | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ | 1.1 | | | V |
| V_{IL} | low-Level Input Voltage | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ | | | 0.4 | V |
| I_{IN} | Input Bias Current | Input Tied to GND or VIN | | 0.01 | 1.00 | μA |

V_{OUT} Regulation

| | | | | | | |
|--|-----------------------|---|-------------|----------|------------|-----|
| V_{REG} | V_{OUT} DC Accuracy | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}=0$ to 3.0 A, Auto PFM/PWM | -2.5 | | 2.5 | % |
| | | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}=0$ to 3.0 A, Forced PWM | -1.5 | | 1.5 | |
| | | $V_{IN}=3.8\text{ V}$, $V_{OUT}=0.6\text{ V}$, $I_{OUT(DC)}=500\text{ mA}$, Auto PFM/PWM | -2.3 -14 | | -0.5 -3 | mV |
| $\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$ | Load Regulation | $I_{OUT(DC)}=1$ to 3 A | | -0.01 | | %/A |
| $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ | Line Regulation | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT(DC)}=1.5\text{ A}$ | | 0.01 | | %/A |
| V_{TRSP} | Transient Response | I_{LOAD} Step 0.01 A \leftrightarrow 1.5 A, $t_r=t_f=200\text{ ns}$, $V_{OUT}=1.15625\text{ V}$ | | ± 50 | | mV |
| | | I_{LOAD} Step 0 A \leftrightarrow 500 mA, $t_r=t_f=100\text{ ns}$, $V_{IN}=3.8\text{ V}$, $V_{OUT}=0.6\text{ V}$ | | ± 16 | | |

Power Switch / Protection

| | | | | | | |
|-------------|-----------------------------|-------------------|------|------|------|------------------|
| I_{LIMPK} | P-MOS Peak Current Limit | | 4.00 | 4.75 | 5.50 | A |
| T_{LIMIT} | Thermal Shutdown | | | 150 | | $^\circ\text{C}$ |
| T_{HYST} | Thermal Shutdown Hysteresis | | | 17 | | $^\circ\text{C}$ |
| V_{SDWN} | Input OVP Shutdown | Rising Threshold | | 6.15 | | V |
| | | Falling Threshold | 5.50 | 5.73 | | |

Frequency Control

| | | | | | | |
|----------|----------------------|--|------|------|------|-----|
| f_{SW} | Oscillator Frequency | | 2.05 | 2.40 | 2.75 | MHz |
|----------|----------------------|--|------|------|------|-----|

DAC

| | | | | | | |
|--|--|--|--|---|-----|------|
| | Resolution | | | 7 | | Bits |
| | Differential Nonlinearity ⁽⁵⁾ | | | | 0.5 | LSB |

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Table 8. ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at $V_{IN}=3.6\text{ V}$, $T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A=25^\circ\text{C}$, $V_{IN}=3.6\text{ V}$, and $EN=HIGH$. $V_{OUT} = 1.15625\text{ V}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-------------------|---|---|------|------|------|---------------|
| Soft-Start | | | | | | |
| t_{SS} | Regulator Enable to Regulated V_{OUT} | $R_{LOAD} > 5\Omega$, $V_{OUT}=1.15625\text{V}$, From EN Rising Edge to 95% V_{OUT} | | 150 | | μs |

5. Monotonicity assured by design.

Table 9. I²C TIMING SPECIFICATIONS

Minimum and maximum values are at $V_{IN}=3.6\text{ V}$, $T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A=25^\circ\text{C}$, $V_{IN}=3.6\text{ V}$, and $EN=HIGH$. $V_{OUT} = 1.15625\text{ V}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|---|---|------|------|------|---------------|
| Power Supplies | | | | | | |
| f_{SCL} | SCL Clock Frequency | Standard Mode | | | 100 | kHz |
| | | Fast Mode | | | 400 | |
| | | Fast Mode Plus | | | 1000 | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | | 3400 | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | | 1700 | |
| t_{BUF} | Bus-Free Time between STOP and START Conditions | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| | | Fast Mode Plus | | 0.5 | | |
| $t_{HD;STA}$ | START or REPEATED START Hold Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | |
| | | Fast Mode Plus | | 260 | | ns |
| | | High-Speed Mode | | 160 | | |
| t_{LOW} | SCL LOW Period | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| | | Fast Mode Plus | | 0.5 | | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 160 | | ns |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 320 | | |
| t_{HIGH} | SCL HIGH Period | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | |
| | | Fast Mode Plus | | 260 | | ns |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 60 | | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 120 | | |
| $t_{SU;STA}$ | Repeated START Setup Time | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 600 | | |
| | | Fast Mode Plus | | 260 | | ns |
| | | High-Speed Mode | | 160 | | |

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Table 9. I²C TIMING SPECIFICATIONS

Minimum and maximum values are at $V_{IN}=3.6\text{ V}$, $T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A=25^\circ\text{C}$, $V_{IN}=3.6\text{ V}$, and EN=HIGH. $V_{OUT} = 1.15625\text{ V}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-----------------------|--|---|-------------|------|------|---------------|
| Power Supplies | | | | | | |
| $t_{SU;DAT}$ | Data Setup Time | Standard Mode | | 250 | | ns |
| | | Fast Mode | | 100 | | |
| | | Fast Mode Plus | | 50 | | |
| | | High-Speed Mode | | 10 | | |
| $t_{HD;DAT}$ | Data Hold Time | Standard Mode | 0 | | 3.45 | μs |
| | | Fast Mode | 0 | | 900 | |
| | | Fast Mode Plus | 0 | | 450 | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | 0 | | 70 | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | 0 | | 150 | |
| t_{RCL} | SCL Rise Time | Standard Mode | $20+0.1C_B$ | | 1000 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 20 | 160 | |
| t_{FCL} | SCL Fall Time | Standard Mode | $20+0.1C_B$ | | 300 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 10 | 40 | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 20 | 80 | |
| t_{RCL1} | Rise Time of SCL After a RE-PEATED START Condition and After ACK Bit | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 10 | 80 | ns |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 20 | 160 | |
| t_{RDA} | SDA Rise Time | Standard Mode | $20+0.1C_B$ | | 1000 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 20 | 160 | |
| t_{FDA} | SDA Fall Time | Standard Mode | $20+0.1C_B$ | | 300 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High-Speed Mode, $C_B \leq 100\text{ pF}$ | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400\text{ pF}$ | | 20 | 160 | |
| $t_{SU;STO}$ | Stop Condition Setup Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 120 | | |
| | | High-Speed Mode | | 160 | | |
| C_B | Capacitive Load for SDA and SCL | | | | 400 | pF |

Timing Diagrams

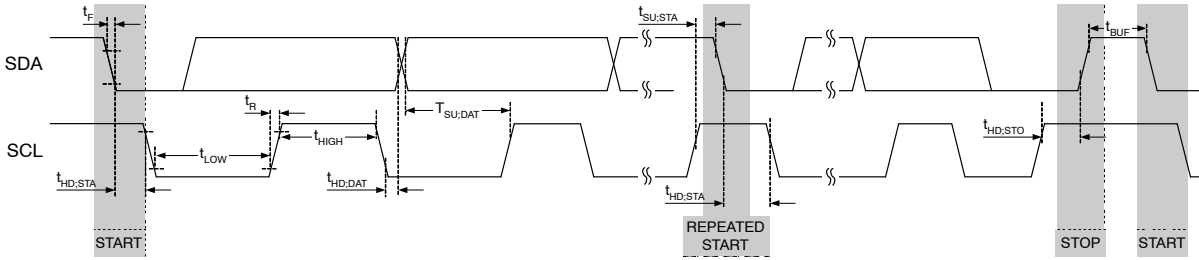
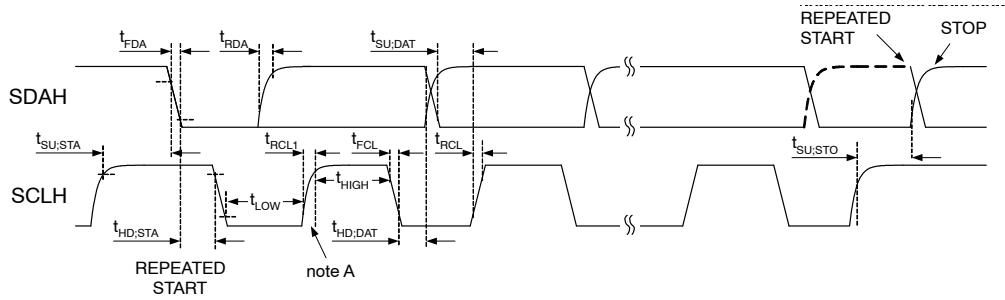




Figure 3. I²C Interface Timing for Fast Plus, Fast, and Slow Modes



 = MCS Current Source Pull-up
 = R_p Resistor Pull-up

Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 4. I²C Interface Timing for High-Speed Mode

TYPICAL CHARACTERISTICS

(Unless otherwise specified, Auto PFM/PWM Mode, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.15625\text{ V}$, $V_{SEL} = EN = V_{IN}$, $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1 and Table 2. Efficiency test conditions; I_{LOAD} : 1 mA to 3 A, $L = 330\text{ nH}$, DFE201612E-R33N (Toko). $C_{IN} = 4.7\text{ }\mu\text{F}$, 0603, C1608X5R1A475K (TDK), $C_{OUT} \times 2 = 2X47\text{ }\mu\text{F}$, 0603, GRM188R60J476ME (Murata).)

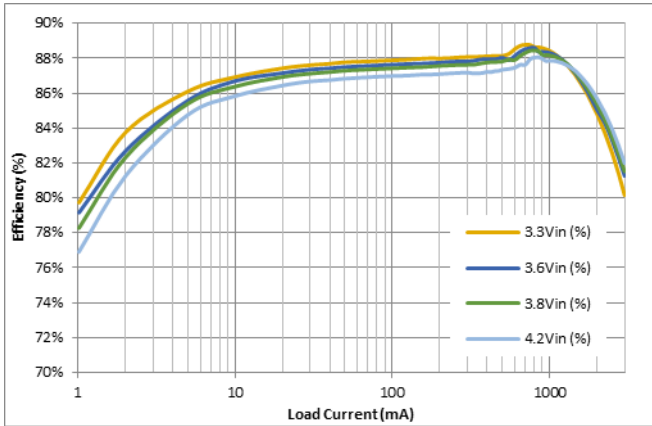


Figure 5. Efficiency vs. Load Current and Input Voltage, $V_{OUT}=1.15625\text{ V}$

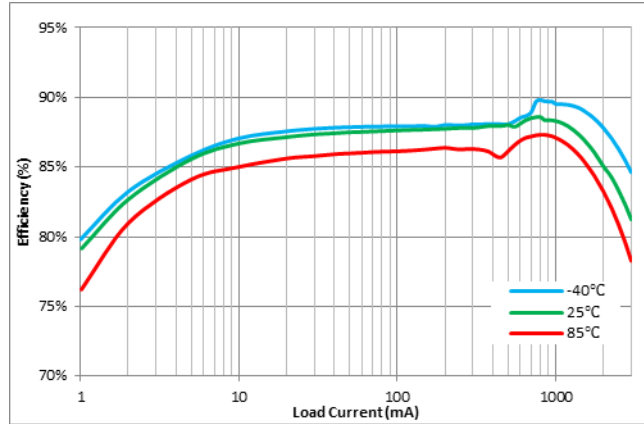


Figure 6. Efficiency vs. Load Current and Temperature, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.15625\text{ V}$

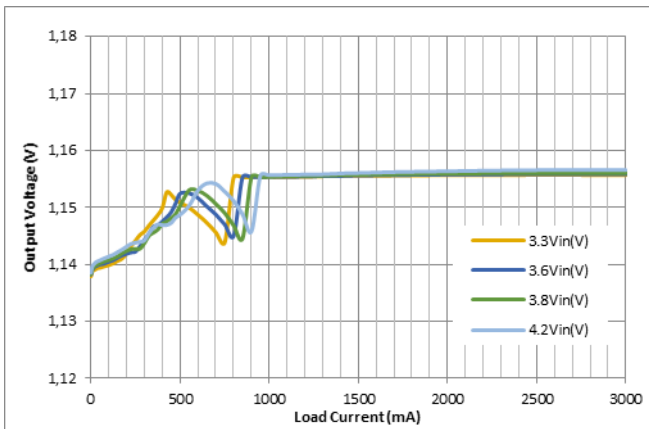


Figure 7. Output Regulation vs. Load Current and Input Voltage, $V_{OUT}=1.15625\text{ V}$

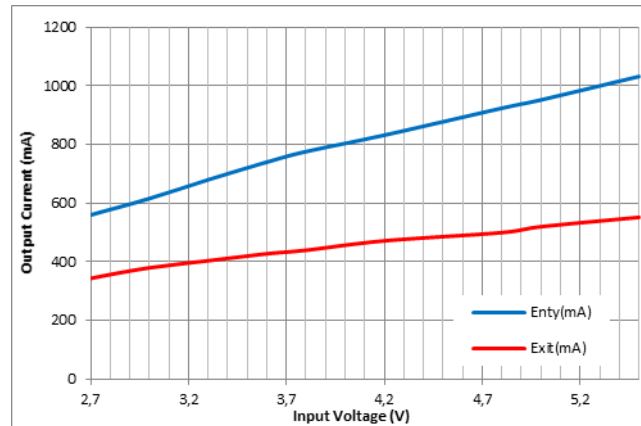


Figure 8. PWM Entry / Exit Level vs. Input Voltage, $V_{OUT}=1.15625\text{ V}$

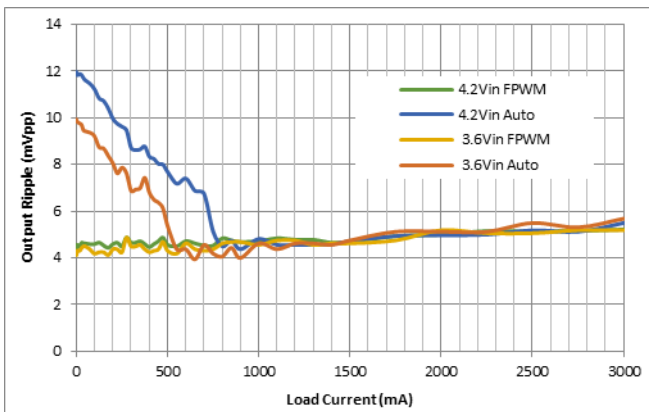


Figure 9. Output Ripple vs. Load Current, $V_{IN}=4.2\text{ V}$ and 3.6 V , $V_{OUT}=1.15625\text{ V}$, Auto and Forced PWM

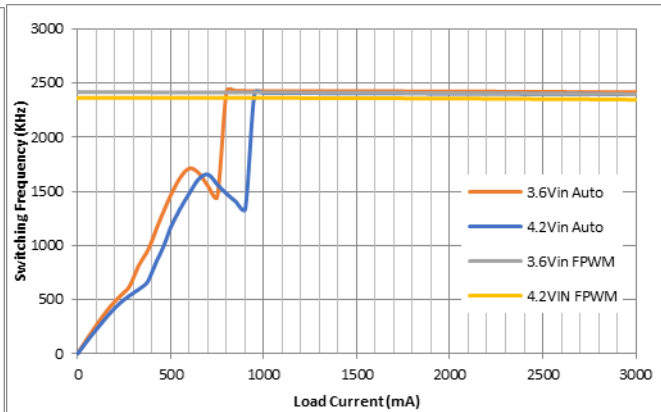


Figure 10. Frequency vs. Load Current, $V_{IN}=4.2\text{ V}$ and 3.6 V , $V_{OUT}=1.15625\text{ V}$, Auto PWM

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise specified, Auto PFM/PWM Mode, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.15625\text{ V}$, $VSEL = EN = V_{IN}$, $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1 and Table 2. Efficiency test conditions; I_{LOAD} : 1 mA to 3 A, $L = 330\text{ nH}$, DFE201612E-R33N (Toko). $C_{IN} = 4.7\text{ }\mu\text{F}$, 0603, C1608X5R1A475K (TDK), $C_{OUT} \times 2 = 2 \times 2X47\text{ }\mu\text{F}$, 0603, GRM188R60J476ME (Murata).)

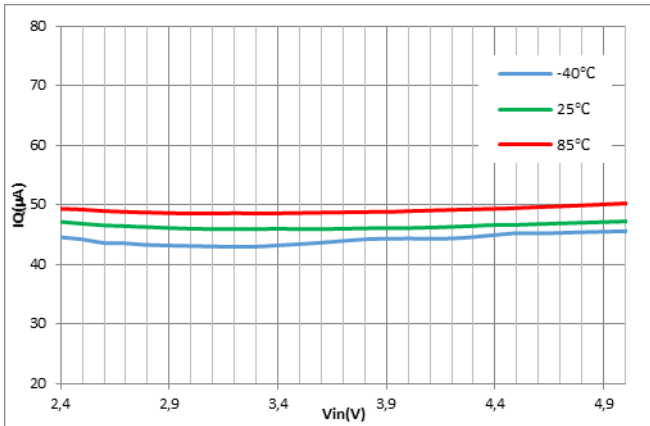


Figure 11. Quiescent Current vs. Input Voltage and Temperature, Auto Mode, $V_{OUT}=1.15625\text{ V}$

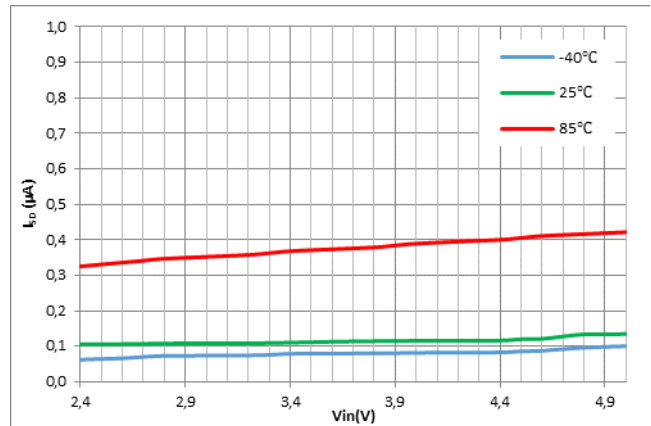


Figure 12. Efficiency vs. Load Current and Temperature, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.15625\text{ V}$

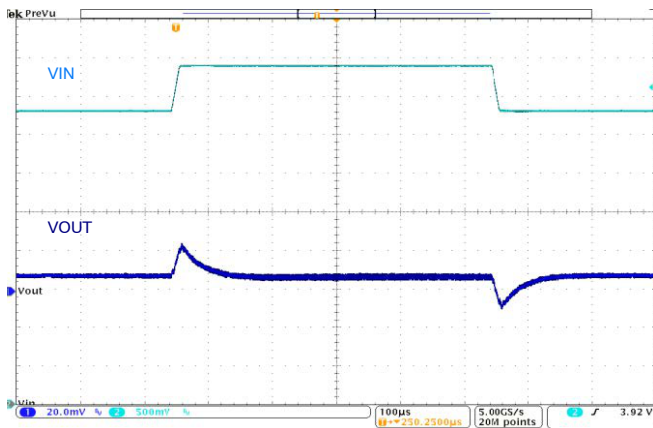


Figure 13. Line Transient, $3.6\text{--}4.2\text{ V}_{IN}$, 1.15625 V_{OUT} , $10\text{ }\mu\text{s}$ Edge at 1 A Load

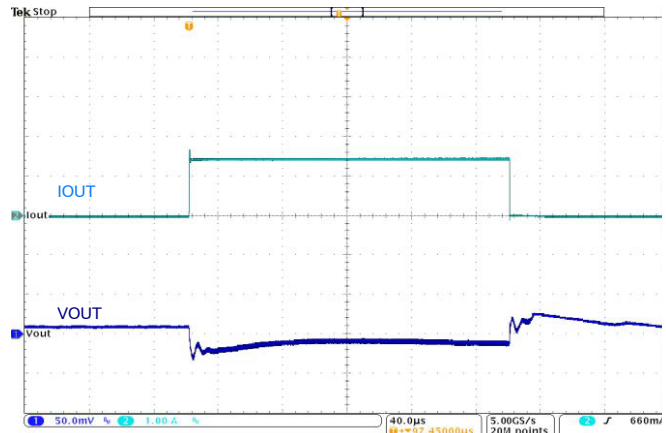


Figure 14. Load Transient, 3.6 V_{IN} , 1.15625 V_{OUT} , $0.01\text{--}1.5\text{ A}$, 120 ns Edge

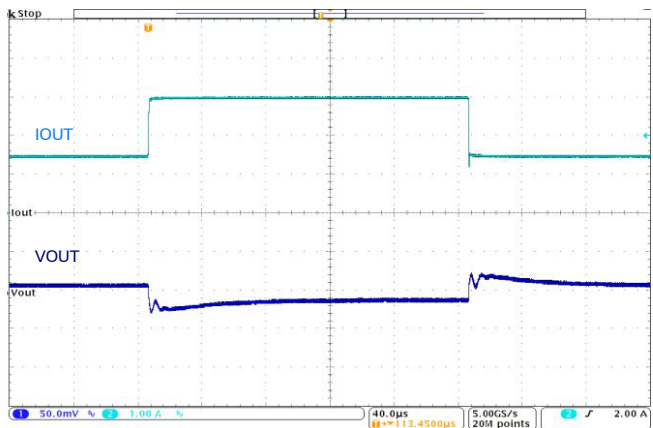


Figure 16. Load Transient, 3.6 V_{IN} , 1.15625 V_{OUT} , $1.5\text{--}3\text{ A}$, 120 ns Edge

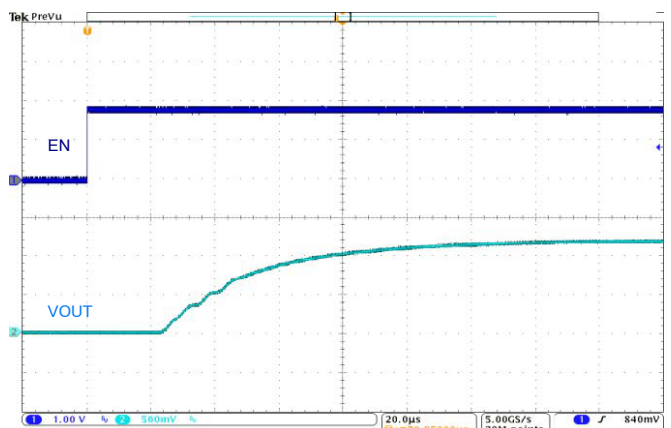


Figure 15. Startup, $5\text{ }\Omega$ Load, $V_{OUT} = 1.15625\text{ V}$, $V_{IN} = 3.6\text{ V}$

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise specified, Auto PFM/PWM Mode, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.15625\text{ V}$, $V_{SEL} = EN = V_{IN}$, $T_A = 25^\circ\text{C}$; circuit and components according to Figure 1 and Table 2. Efficiency test conditions; I_{LOAD} : 1 mA to 3 A, $L = 330\text{ nH}$, DFE201612E-R33N (Toko). $C_{IN} = 4.7\text{ }\mu\text{F}$, 0603, C1608X5R1A475K (TDK), $C_{OUT} \times 2 = 2 \times 2X47\text{ }\mu\text{F}$, 0603, GRM188R60J476ME (Murata).)

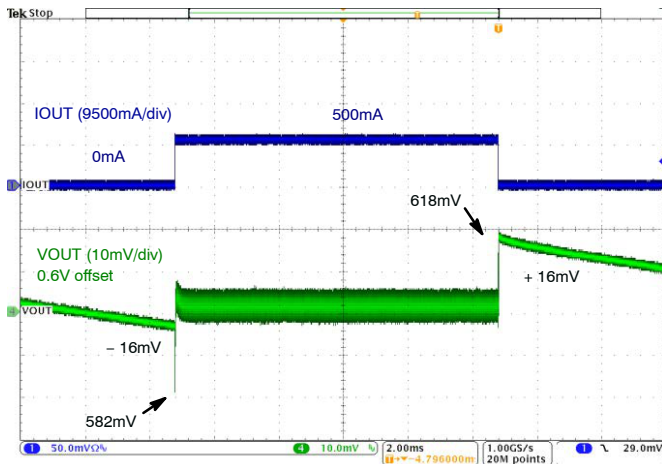


Figure 17. Load Transient, 3.8 V_{IN} , 0.6 V_{OUT} , 0–500 mA, 100 ns Edge, 47 μF C_{OUT}

Operating Description

The FAN53526 is a step-down switching voltage regulator that delivers a programmable output voltage from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53526 is capable of delivering 3.0 A at over 80% efficiency. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 330 nH or 470 nH for the output inductor and 44 μF for the output capacitor. High efficiency is maintained at light load with single-pulse PFM.

An I²C-compatible interface allows transfers up to 3.4 Mbps. This communication interface can be used to:

- Dynamically re-program the output voltage in 6.25 mV increments;
- Reprogram the mode to enable or disable PFM;
- Control voltage transition slew rate; or
- Enable / disable the regulator.

Control Scheme

The FAN53526 uses a proprietary non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53526 operates in Discontinuous Current Mode (DCM) single-pulse PFM, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and CCM Modes.

PFM can be disabled by programming the MODE bits in the CONTROL register in combination with the state of the VSEL pin. See table in the Control Register, 02h.

Enable and Soft-Start

When the EN pin is LOW; the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I²C can be written to or read from as long as input voltage is above the UVLO. The registers keep the content when the EN pin is LOW. The registers are reset to default values during a Power On Reset (POR). When the OUTPUT_DISCHARGE bit in the Control register is enabled (logic HIGH) and the EN pin is LOW or the BUCK_ENx bit is LOW, an 11 W load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft-start cycle. During soft-start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited, allowing the IC to start into a pre-charged capacitive load.

If large values of output capacitance are used, the regulator may fail to start. The maximum C_{OUT} capacitance for starting with a heavy constant-current load is approximately:

$$C_{OUTMAX} \approx (I_{LMPK} - I_{LOAD}) \cdot \frac{320\mu}{V_{OUT}} \quad (\text{eq. 1})$$

where C_{OUTMAX} is expressed in μF and I_{LOAD} is the load current during soft-start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters

tri-state before reattempting soft-start 1700 μs later. This limits the duty cycle of full output current during soft-start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH. These options start after a POR, regardless of the state of the VSEL pin.

Table 10. HARDWARE AND SOFTWARE ENABLE

| Pins | | BITS | | | |
|------|------|----------|----------|--------|----------|
| EN | VSEL | BUCK_EN0 | BUCK_EN1 | Output | Mode |
| 0 | X | X | X | OFF | Shutdown |
| 1 | 0 | 0 | X | OFF | Shutdown |
| 1 | 0 | 1 | X | ON | Auto |
| 1 | 1 | X | 0 | OFF | Shutdown |
| 1 | 1 | X | 1 | ON | FPWM |

VSEL Pin and I²C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output is given as:

$$V_{OUT} = 0.600\text{V} + \text{NSELx} \cdot 6.25\text{mV} \quad (\text{eq. 2})$$

For example, if NSEL = 1010000 (80 decimal), then $V_{OUT} = 0.600 + 0.5 = 1.100\text{ V}$.

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to

VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages, as shown in Table 8.

Transition Slew Rate Limiting

When transitioning from a low to high voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the Control register, as shown in Table 5.

Table 11. TRANSITION SLEW RATE

| Decimal | Bin | Slew Rate | |
|---------|-----|-----------|-------------------|
| 0 | 000 | 64.00 | mV/ μs |
| 1 | 001 | 32.00 | mV/ μs |
| 2 | 010 | 16.00 | mV/ μs |
| 3 | 011 | 8.00 | mV/ μs |
| 4 | 100 | 4.00 | mV/ μs |
| 5 | 101 | 2.00 | mV/ μs |
| 6 | 110 | 1.00 | mV/ μs |
| 7 | 111 | 0.50 | mV/ μs |

Transitions from high to low voltage rely on the output load to discharge V_{OUT} to the new set point. Once the high-to-low transition begins, the IC stops switching until V_{OUT} has reached the new set point.

Under-Voltage Lockout (UVLO)

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises HIGH enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

Input Over-Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (~ 6.2 V), the IC stops switching to protect the circuitry from internal spikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching

this point, the high-side switch turns off, preventing high currents from causing damage. 16 consecutive current limit cycles in current limit, cause the regulator to shut down and stay off for about 1700 μ s before attempting a restart.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 17°C hysteresis.

Monitor Register (Reg05)

The Monitor register indicates of the regulation state of the IC. If the IC is enabled and is regulating, its value is (1000 0001).

Table 12. I²C SLAVE ADDRESS

| Hex | Bits | | | | | | | |
|-----|------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| C2 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | |

Other slave addresses can be assigned. Contact an On Semiconductor representative.

Bus Timing

As shown in Figure 18 data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow sufficient time for the data to set up before the next SCL rising edge.

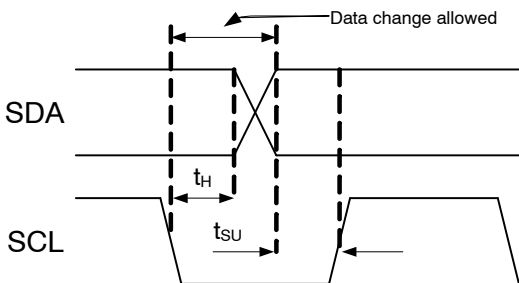


Figure 18. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 19.

I²C Interface

The serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I²C Bus® specifications. The SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is C0 for all options except FAN53526UC168X, which has a hex slave address of C2.

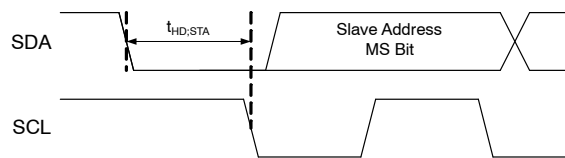


Figure 19. START Bit

A transaction ends with a STOP condition, defined as SDA transitioning from 0 to 1 with SCL high, as shown in Figure 20.

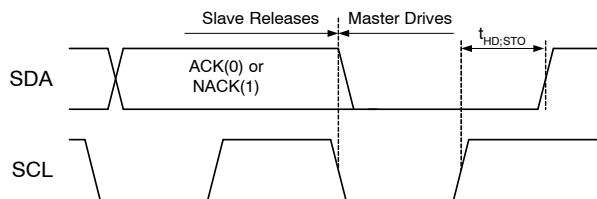


Figure 20. STOP Bit

During a read from the FAN53526, the master issues a REPEATED START after sending the register address and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 21.

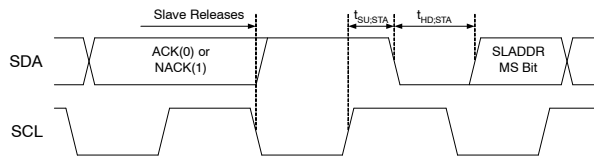


Figure 21. REPEATED START Timing

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical; except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition (Figure 19). The master code is sent in Fast or Fast-Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 21) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 20) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 21).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as:

- Master Drives Bus and
- Slave Drives Bus

All addresses and data are MSB first.

Table 13. I²C BIT DEFINITIONS FOR FIGURE 22 AND FIGURE 23

| Symbol | Definition |
|-----------|--|
| S | START, see Figure 19 |
| P | STOP, see Figure 20 |
| R | REPEATED START, see Figure 21 |
| A | ACK. The slave drives SDA to 0 acknowledge the preceding packet. |
| \bar{A} | NACK. The slave sends a 1 to NACK the preceding packet. |

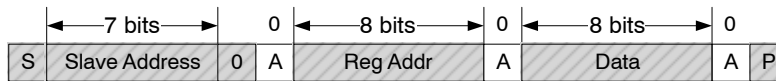


Figure 22. Write Transaction

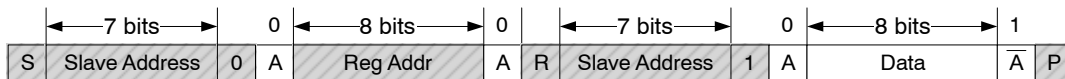


Figure 23. Write Transaction Followed by a Read Transaction

REGISTER DESCRIPTION

Table 14. REGISTER MAP

| Hex Address | Name | Function | Binary | Hex |
|-------------|---------|--|----------|-----|
| 00 | VSEL0 | Controls V _{OUT} settings when VSEL pin = LOW | 1XXXXXXX | XX |
| 01 | VSEL1 | Controls V _{OUT} settings when VSEL pin = HIGH | 1XXXXXXX | XX |
| 02 | CONTROL | Determines whether V _{OUT} output discharge is enabled and also the slew rate of positive transitions | 1000010 | 82 |
| 03 | ID1 | Read-only register identifies vendor and chip type | 10000001 | 81 |
| 04 | ID2 | Read-only register identifies die revision | 00001000 | 08 |
| 05 | MONITOR | Indicates device status | 00000000 | 00 |

Table 15. BIT DEFINITIONS

| Bit | Name | Type | Value | Description | | | | | | | | | | | | | | | |
|-------------------------------------|------------------|--------------|----------|---|----------|--------|-----------|-----|----|--------------|-----|----|------------|------|----|--------------|------|----|------------|
| VSEL0 Register Address: 00 | | | | | | | | | | | | | | | | | | | |
| 7 | BUCK_EN0 | R/W | 1 | Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent. | | | | | | | | | | | | | | | |
| 6:0 | NSEL0 | R/W | XXX XXXX | Sets V _{OUT} value from 0.600 to 1.39375 V (see Eq.2). | | | | | | | | | | | | | | | |
| VSEL1 Register Address: 01 | | | | | | | | | | | | | | | | | | | |
| 7 | BUCK_EN1 | R/W | 1 | Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent. | | | | | | | | | | | | | | | |
| 6:0 | NSEL1 | R/W | XXX XXXX | Sets V _{OUT} value from 0.600 to 1.39375 V (see Eq.). | | | | | | | | | | | | | | | |
| CONTROL Register Address: 02 | | | | | | | | | | | | | | | | | | | |
| 7 | OUTPUT_DISCHARGE | R/W | 0 | When the regulator is disabled, V _{OUT} is not discharged. | | | | | | | | | | | | | | | |
| | | | 1 | When the regulator is disabled, V _{OUT} discharges through an internal pull-down. | | | | | | | | | | | | | | | |
| 6:4 | SLEW | R/W | 000 –111 | Sets the slew rate for positive voltage transitions (see Table 4) | | | | | | | | | | | | | | | |
| 3 | Reserved | | 0 | Always reads back 0. | | | | | | | | | | | | | | | |
| 2 | RESET | R/W | 0 | Setting to 1 resets all registers to default values. Always reads back 0. | | | | | | | | | | | | | | | |
| 1:0 | MODE | R/W | 10 | In combination with the VSEL pin, these two bits set the operation of the buck to be either in Auto-PFM/PWM Mode during light load or Forced PWM mode. See table below. Mode of Operation <table border="1"> <thead> <tr> <th>VSEL Pin</th> <th>Binary</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>X0</td> <td>Auto PFM/PWM</td> </tr> <tr> <td>Low</td> <td>X1</td> <td>Forced PWM</td> </tr> <tr> <td>High</td> <td>0X</td> <td>Auto PFM/PWM</td> </tr> <tr> <td>High</td> <td>1X</td> <td>Forced PWM</td> </tr> </tbody> </table> | VSEL Pin | Binary | Operation | Low | X0 | Auto PFM/PWM | Low | X1 | Forced PWM | High | 0X | Auto PFM/PWM | High | 1X | Forced PWM |
| VSEL Pin | Binary | Operation | | | | | | | | | | | | | | | | | |
| Low | X0 | Auto PFM/PWM | | | | | | | | | | | | | | | | | |
| Low | X1 | Forced PWM | | | | | | | | | | | | | | | | | |
| High | 0X | Auto PFM/PWM | | | | | | | | | | | | | | | | | |
| High | 1X | Forced PWM | | | | | | | | | | | | | | | | | |
| ID1 Register Address: 03 | | | | | | | | | | | | | | | | | | | |
| 7:5 | VENDOR | R | 100 | Signifies On Semiconductor as the IC vendor. | | | | | | | | | | | | | | | |
| 4 | Reserved | R | 0 | Always reads back 0. | | | | | | | | | | | | | | | |
| 3:0 | DIE_ID | R | 0001 | DIE ID – FAN53525/6. | | | | | | | | | | | | | | | |
| ID2 Register Address: 04 | | | | | | | | | | | | | | | | | | | |
| 7:4 | Reserved | R | 0000 | Always reads back 0000. | | | | | | | | | | | | | | | |
| 3:0 | DIE_REV | R | 1000 | FAN53526 Die Revision | | | | | | | | | | | | | | | |
| MONITOR Register Address: 05 | | | | | | | | | | | | | | | | | | | |
| 7 | PGOOD | R | 0 | 1: Buck is enabled and soft-start is completed. | | | | | | | | | | | | | | | |

Table 15. BIT DEFINITIONS

| Bit | Name | Type | Value | Description |
|-----|-------------|------|-------|--|
| 6 | UVLO | R | 0 | 1: Signifies the VIN is less than the UVLO threshold. |
| 5 | OVP | R | 0 | 1: Signifies the VIN is greater than the OVP threshold. |
| 4 | POS | R | 0 | 1: Signifies a positive voltage transition is in progress and the output voltage has not yet reached its new setpoint. |
| 3 | NEG | R | 0 | 1: Signifies a negative voltage transition is in progress and the output voltage has not yet reached its new setpoint. |
| 2 | RESET-STAT | R | 0 | 1: Indicates that a register reset was performed. This bit is cleared after register 5 is read. |
| 1 | OT | R | 0 | 1: Signifies the VIN is less than the UVLO threshold. |
| 0 | BUCK_STATUS | R | 0 | 1: Signifies the VIN is greater than the OVP threshold. |

APPLICATION INFORMATION

Selecting the Inductor

The output inductor must meet both the required inductance and the energy-handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \right) \quad (\text{eq. 3})$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (\text{eq. 4})$$

The FAN53526 is optimized for operation with $L=330$ nH, but is stable with inductances up to 1.0 μ H (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so decreases the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical

size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin-effect losses:

$$I_{RMS} = \sqrt{I_{OUT(DC)}^2 + \frac{\Delta I^2}{12}} \quad (\text{eq. 5})$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs and the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs and the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 16. EFFECTS OF INDUCTOR VALUE (FROM 330NH RECOMMENDED) ON REGULATOR PERFORMANCE

| $I_{MAX(LOAD)}$ | ΔV_{OUT} (Eq.(7)) | Transient Response |
|-----------------|---------------------------|--------------------|
| Increase | Decrease | Degraded |

Inductor Current Rating

The current-limit circuit can allow substantial peak currents to flow through L1 under worst-case conditions. If it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

For space-constrained applications, a lower current rating for L1 can be used. The FAN53526 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor. Refer to Table 2 for the recommended inductors.

Output Capacitor and V_{OUT} Ripple

If space is at a premium, 0603 capacitors may be used.

Increasing C_{OUT} has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT} , is calculated by:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \quad (\text{eq. 6})$$

where C_{OUT} is the effective output capacitance.

The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT} . Equation 6 is only valid for CCM operation, which occurs in PWM Mode.

The FAN53526 can be used with either 2 x 22 μ F (0603) or 2 x 47 μ F (0603) output capacitor configuration. If a tighter ripple and transient specification is needed from the FAN53526, then the 2 x 47 μ F is recommended.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square-wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square-wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \cdot \frac{ESL_{COUT}}{L1} \tag{eq. 7}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain $C_{OUT}=20 \mu$ F, a single 22 μ F 0805 would produce twice the square wave ripple as two x 10 μ F 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805 s have lower ESL than 1206 s. If low output ripple is a chief concern, some vendors produce 0508 capacitors with ultra-low ESL. Placing additional small-value capacitors near the load also reduces the high-frequency ripple components.

Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN and PGND pins to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between CIN and the power source lead to reduce under-damped ringing that can occur between the inductance of the power source leads and C_{IN} .

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction-to-ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53526, θ_{JA} is 42°C/W when mounted on its four-layer with vias evaluation board in still air with 2 oz. outer layer copper weight and 1 oz. inner layer.

For long-term reliable operation, the junction temperature (T_J) should be maintained below 125°C.

To calculate maximum operating temperature (<125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN} , V_{OUT} , and load conditions.
2. Calculate total power dissipation using:

$$P_T = V_{OUT} \cdot I_{LOAD} \cdot \left(\frac{1}{\eta} - 1 \right) \tag{eq. 8}$$

3. Estimate inductor copper losses using:

$$P_L = I_{LOAD}^2 \cdot DCR_L \tag{eq. 9}$$

4. Determine IC losses by removing inductor losses (step 3) from total dissipation:

$$P_{IC} = P_T - P_L \tag{eq. 10}$$

5. Determine device operating temperature:

$$\Delta T = P_{IC} \cdot \theta_{JA} \quad T_{IC} = T_A + \Delta T \tag{eq. 11}$$

and

Note that the $R_{DS(ON)}$ of the power MOSFETs increases linearly with temperature at about 1.4%/°C. This causes the efficiency (η) to degrade with increasing die temperature.

Layout Recommendations

1. The input capacitor (C_{IN}) should be connected as close as possible to the VIN and GND pins. Connect to VIN and GND using only top metal. Do not route through vias.
2. Place the inductor (L) as close as possible to the IC. Use short wide traces for the main current paths.
3. The output capacitor (C_{OUT}) should be as close as possible to the IC. Connection to GND should be on top metal. Feedback signal connection to VOUT should be routed away from noisy components and traces (e.g. SW line). For remote sensing application, place one or all output capacitors near the load and if there are also output capacitors placed near the inductor, the maximum trace resistance between the inductor and the load should not exceed 30 m Ω .

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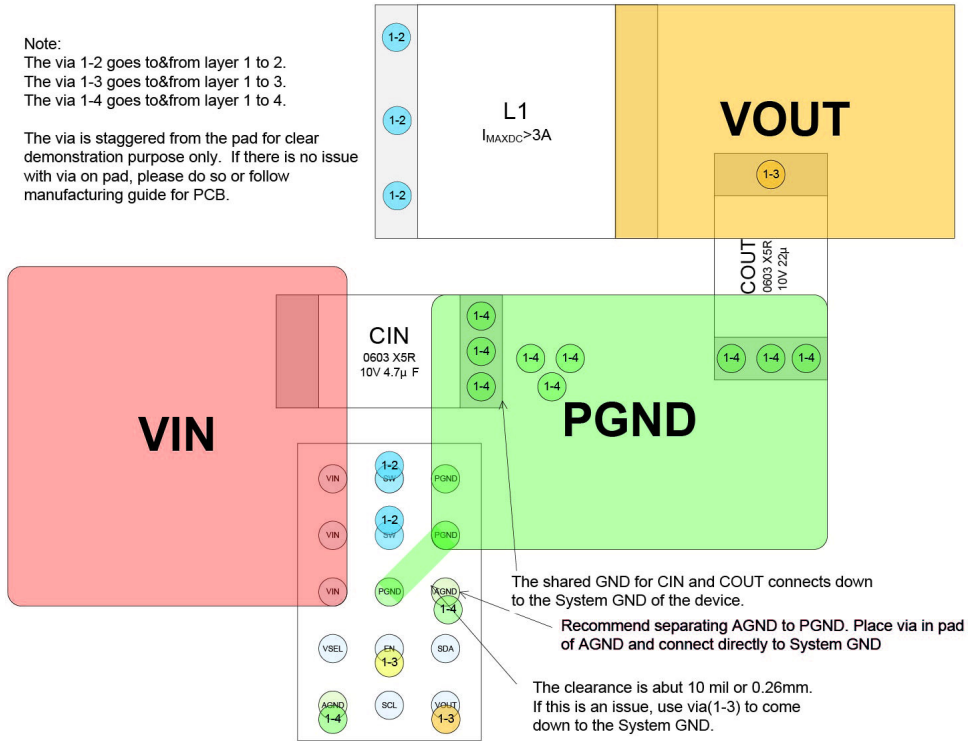


Figure 24. Guidance for Layer 1

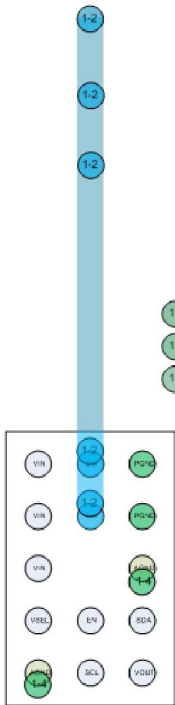


Figure 25. Layer 2

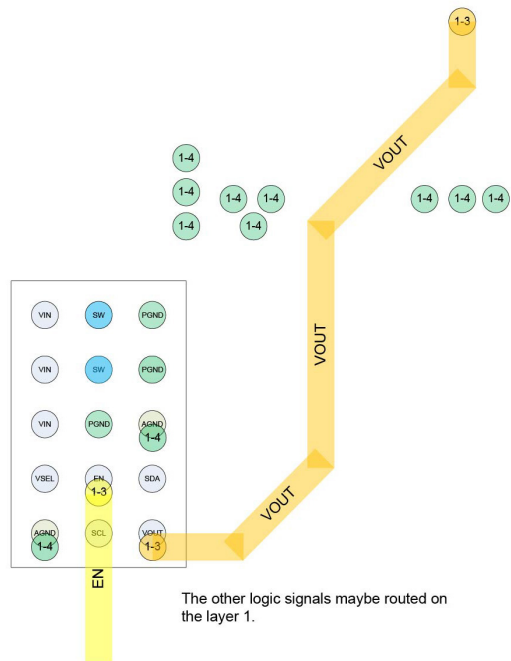


Figure 26. Layer 3

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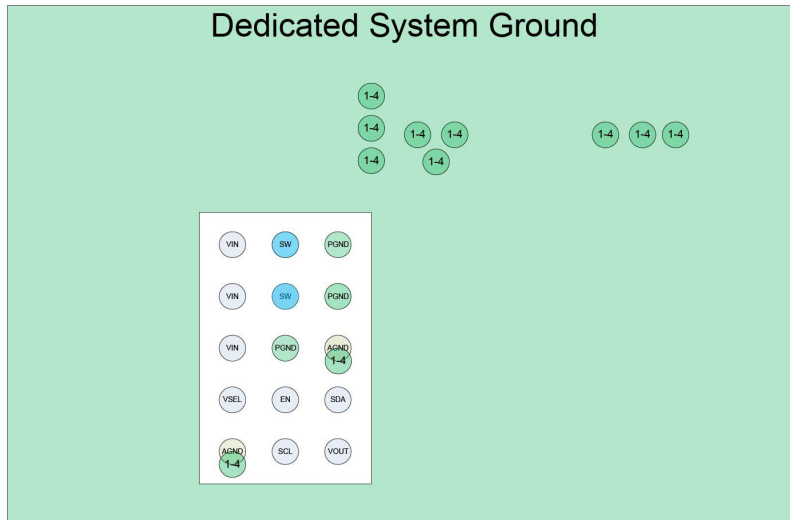


Figure 27. Layer 4

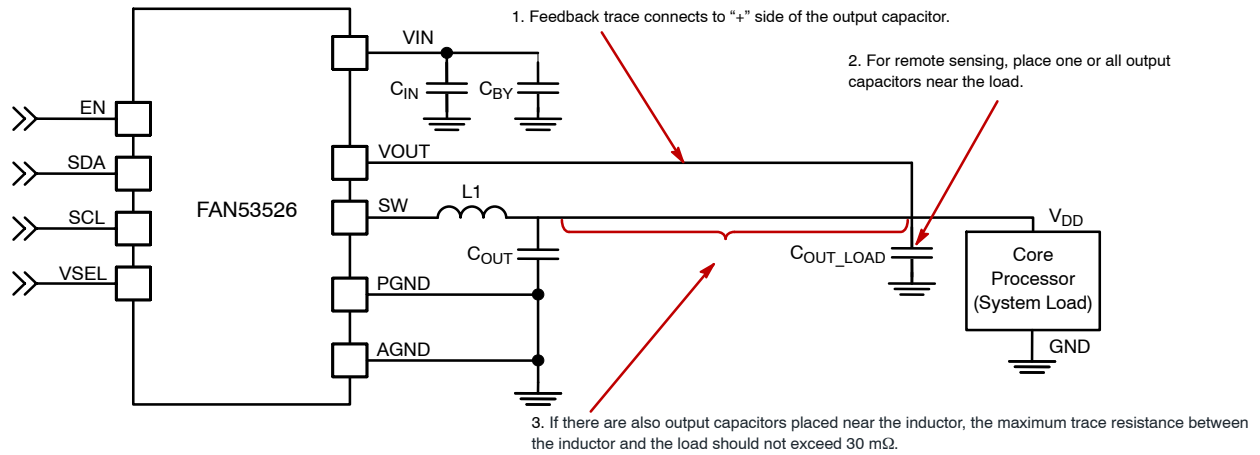


Figure 28. Remote Sensing Schematic

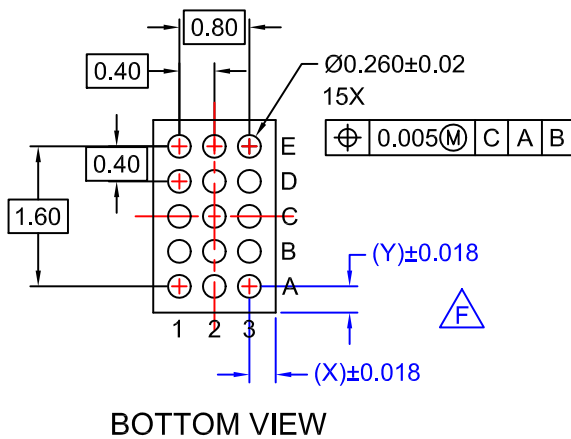
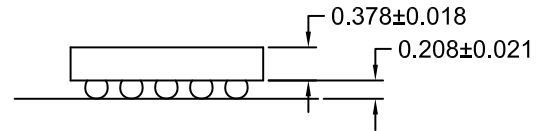
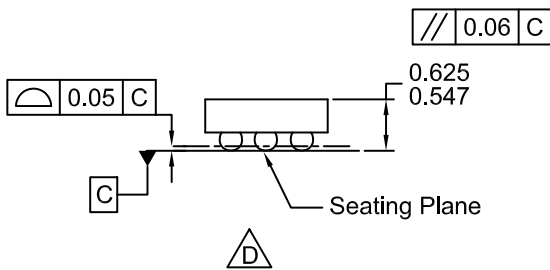
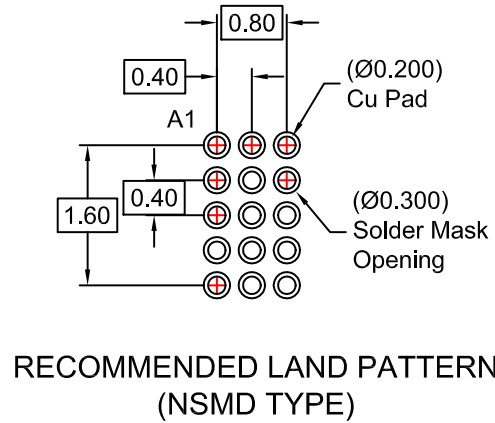
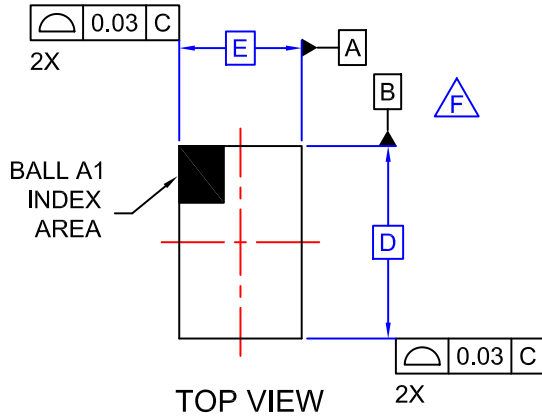
Table 17. PRODUCT SPECIFIC DIMENSIONS

| D | E | X | Y |
|-----------------|-----------------|----------|-----------|
| 2.015 0 ± 03 mm | 1.310 ± 0.03 mm | 0.255 mm | 0.2075 mm |

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CASE 567QS
ISSUE O

DATE 31 OCT 2016



NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5 - 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

| | | |
|-------------------------|----------------------------------|--|
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