

Quad 2-Input OR Gate with LSTTL-Compatible Inputs

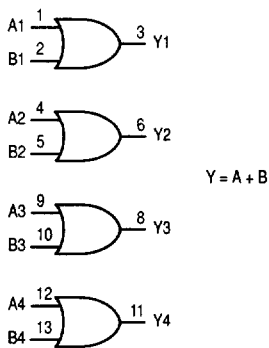
High-Performance Silicon-Gate CMOS

The MC54/74HCT32A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT32A is identical in pinout to the LS32.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 64 FETs or 16 Equivalent Gates

LOGIC DIAGRAM

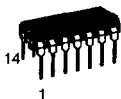


PIN 14 = VCC
PIN 7 = GND

MC54/74HCT32A



J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 646-06

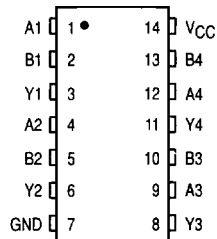


D SUFFIX
SOIC PACKAGE
CASE 751A-03

ORDERING INFORMATION

MC54HCTXXAJ	Ceramic
MC74HCTXXAN	Plastic
MC74HCTXXAD	SOIC

PIN ASSIGNMENT



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FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H



MC54/74HCT32A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

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DC ELECTRICAL CHARACTERISTICS FOR THE MC54/74HCT32A (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} Volts	Guaranteed Limits						Unit	
				-55 to 25°C		≤ 85°C		≤ 125°C			
				Min	Max	Min	Max	Min	Max		
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 5.5	2.0 2.0		2.0 2.0		2.0 2.0		V	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 5.5		0.8 0.8		0.8 0.8		0.8 0.8	V	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	5.5	3.98		3.84		3.7			
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1		
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5		±0.1			±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5		1.0		10		40	μA	
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5		≥ -55°C		25°C to 125°C				
					2.9	2.4			mA		

NOTE: Information on typical parametric values can be found in Chapter 2.

AC CHARACTERISTICS FOR THE MC54/74HCT32A ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Fig.	Guaranteed Limits						Unit
			- 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y	1, 2		20		25		30	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output	1, 2		15		19		22	ns
C_{in}	Maximum Input Capacitance			10		10		10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2.

C_{PD}	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF
		15		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

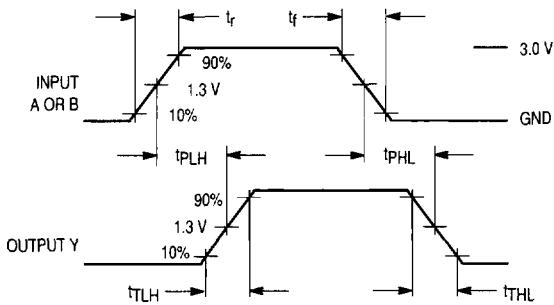
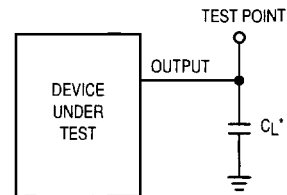


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

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**EXPANDED LOGIC DIAGRAM
(1/4 OF THE DEVICE)**

