

Quad 2-Input NOR Gate

The MC74VHC02 is an advanced high speed CMOS 2-input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 3.6ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 2\mu A$ (Max) at $T_A = 25^\circ C$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 0.8V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 40 FETs or 10 Equivalent Gates

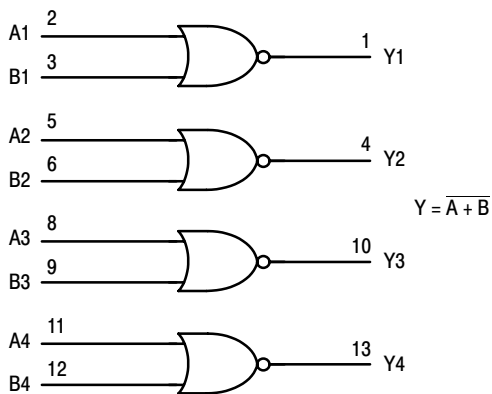


Figure 1. LOGIC DIAGRAM

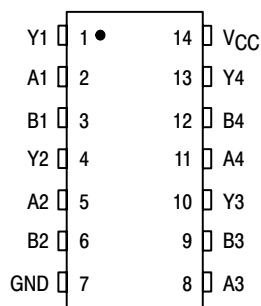


Figure 2. PIN ASSIGNMENT

MC74VHC02



D SUFFIX
14-LEAD SOIC PACKAGE
CASE 751A-03



DT SUFFIX
14-LEAD TSSOP PACKAGE
CASE 948G-01



M SUFFIX
14-LEAD SOIC EIAJ PACKAGE
CASE 965-01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage	- 0.5 to + 7.0	V
V _{out}	DC Output Voltage	- 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	- 20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature	- 40	+ 85	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 3.3V ± 0.3V V _{CC} = 5.0V ± 0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7			1.50 V _{CC} × 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} × 0.3		0.50 V _{CC} × 0.3	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OH} = - 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V _{in} = V _{IH} or V _{IL} I _{OH} = - 4mA I _{OH} = - 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		5.6 8.1	7.9 11.4	1.0 1.0	9.5 13.0	ns
C _{in}	Maximum Input Capacitance			4 10			10	

C _{PD}	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V _{CC} = 5.0V		pF
		15		

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.3	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

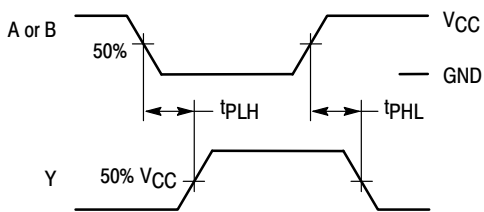
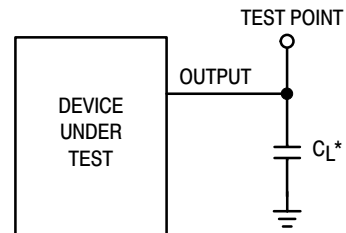


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

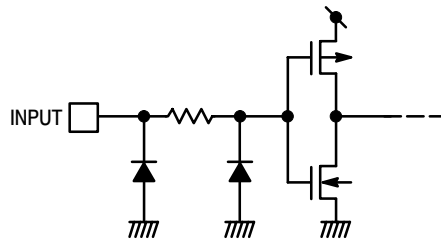


Figure 5. Input Equivalent Circuit