

# MC14049B, MC14050B

## Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage,  $V_{DD}$ .

The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{DD}$  supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS-to-TTL/DTL converter ( $V_{DD} = 5.0\text{ V}$ ,  $V_{OL} \leq 0.4\text{ V}$ ,  $I_{OL} \geq 3.2\text{ mA}$ ).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- $V_{IN}$  can exceed  $V_{DD}$
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
$V_{out}$	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient) per Pin	$\pm 45$	mA
$P_D$	Power Dissipation, per Package (Note 3.) (Plastic) (SOIC)	825 740	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the  $V_{SS}$  pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $V_{SS} \leq V_{in} \leq 18\text{ V}$  and  $V_{SS} \leq V_{out} \leq V_{DD}$  are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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**MARKING DIAGRAMS**

**PDIP-16 P SUFFIX CASE 648**

**SOIC-16 D SUFFIX CASE 751B**

**TSSOP-16 DT SUFFIX CASE 948F**

**SOEIAJ-16 F SUFFIX CASE 966**

xx = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week

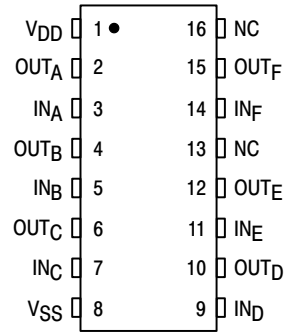
### ORDERING INFORMATION

Device	Package	Shipping
MC14049BCP	PDIP-16	2000/Box
MC14049BD	SOIC-16	2400/Box
MC14049BDR2	SOIC-16	2500/Tape & Reel
MC14049BF	SOEIAJ-16	See Note 1.
MC14050BCP	PDIP-16	2000/Box
MC14050BD	SOIC-16	2400/Box
MC14050BDR2	SOIC-16	2500/Tape & Reel
MC14050BDTEL	TSSOP-16	2000/Tape & Reel
MC14050BF	SOEIAJ-16	See Note 1.
MC14050BFEL	SOEIAJ-16	See Note 1.

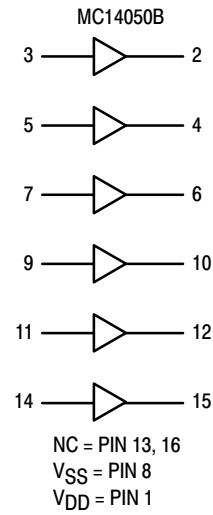
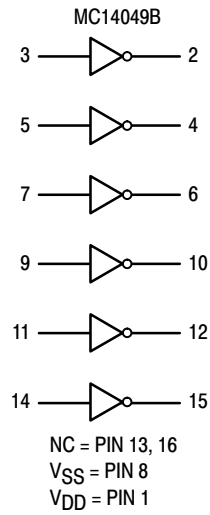
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14049B, MC14050B

## PIN ASSIGNMENT



## LOGIC DIAGRAM



# MC14049B, MC14050B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		+ 25°C			+ 125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>in</sub> = 0	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current	Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	I <sub>OH</sub>	5.0	-1.6	—	-1.25	-2.5	—	-1.0	—	mAdc
		10	-1.6	—	-1.30	-2.6	—	-1.0	—		
		15	-4.7	—	-3.75	-10	—	-3.0	—		
	Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OL</sub>	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
			10	10	—	8.0	16	—	6.6	—	
			15	30	—	24	40	—	19	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	10	20	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc	
		10	—	2.0	—	0.004	2.0	—	60		
		15	—	4.0	—	0.006	4.0	—	120		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, per package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.8 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.5 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.3 μA/kHz) f + I <sub>DD</sub>							μAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at + 25°C

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

Where: I<sub>T</sub> is in μA (per Package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency and k = 0.002.

# MC14049B, MC14050B

## AC SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = +25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time $t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	160 80 60	ns
Output Fall Time $t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$ $t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$ $t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	80 40 30	140 80 60	ns
Propagation Delay Time $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	40 20 15	80 40 30	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

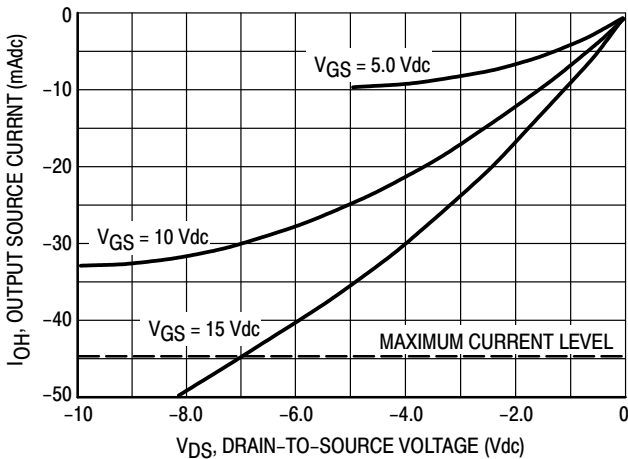
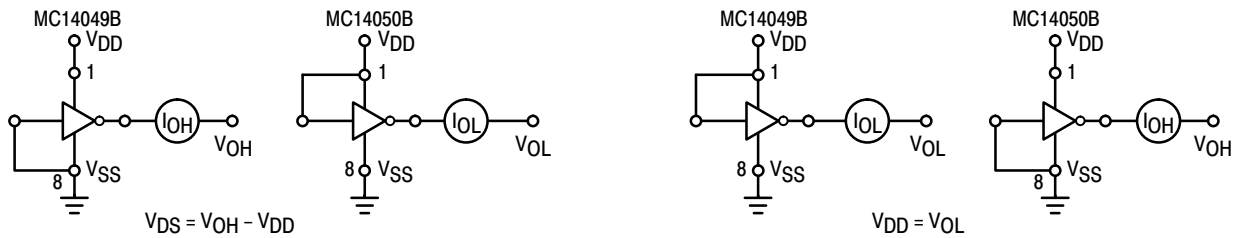


Figure 1. Typical Output Source Characteristics

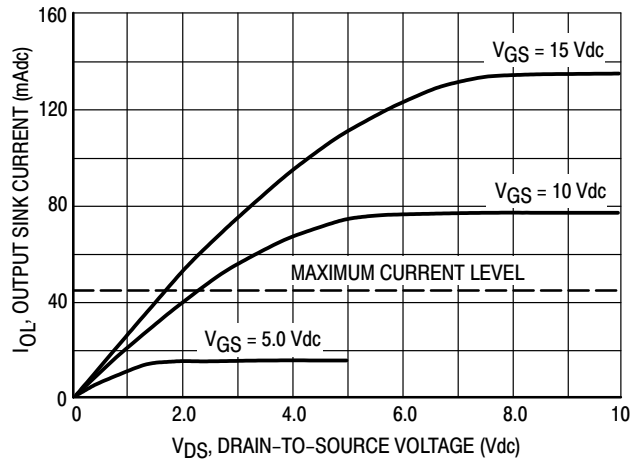


Figure 2. Typical Output Sink Characteristics

# MC14049B, MC14050B

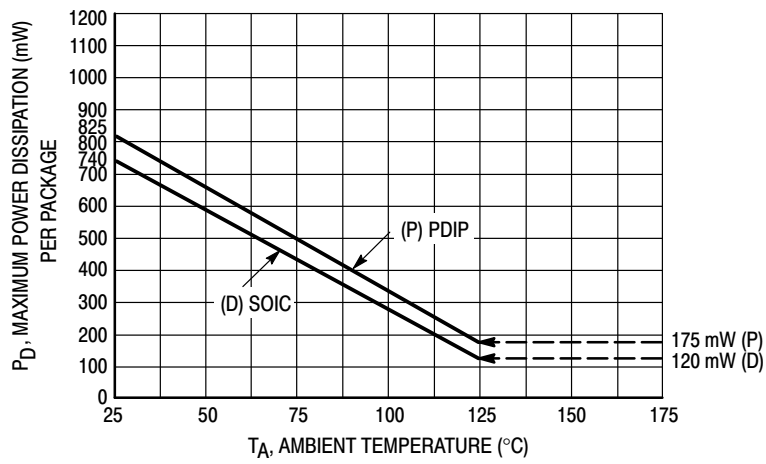


Figure 3. Ambient Temperature Power Derating

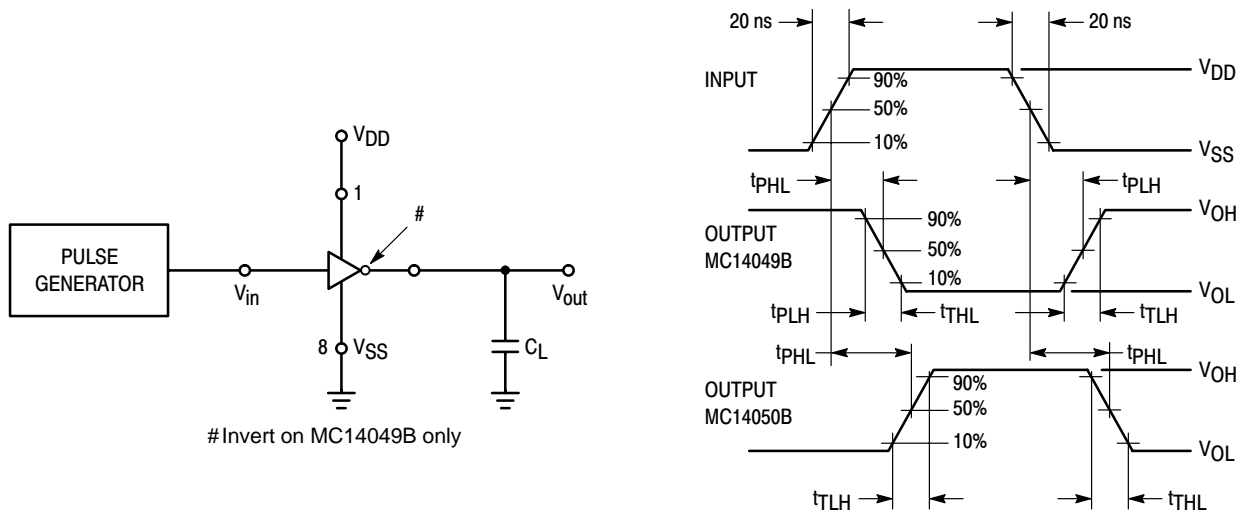


Figure 4. Switching Time Test Circuit and Waveforms