MC14040B

12-Bit Binary Counter

The MC14040B 12−stage binary counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−driving circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin−for−Pin Replacement for CD4040B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
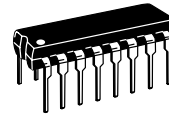
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
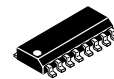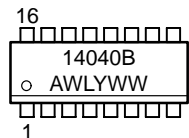
ON Semiconductor™

http://onsemi.com
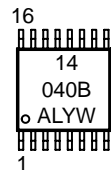
MARKING DIAGRAMS

PDIP−16 P SUFFIX CASE 648

```
16
MC14040BCP
AWLYYWW
1
```

SOIC−16 D SUFFIX CASE 751B

```
16
14040B
AWLYWW
1
```

TSSOP−16 DT SUFFIX CASE 948F

```
16
14
040B
ALYW
1
```

SOEIAJ−16 F SUFFIX CASE 966

```
16
MC14040B
ALYW
1
```
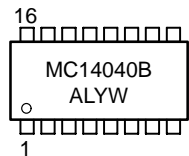
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14040BCP	PDIP−16	2000/Box
MC14040BD	SOIC−16	2400/Box
MC14040BDR2	SOIC−16	2500/Tape & Reel
MC14040BDT	TSSOP−16	96/Rail
MC14040BF	SOEIAJ−16	See Note 1.
MC14040BFEL	SOEIAJ−16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.
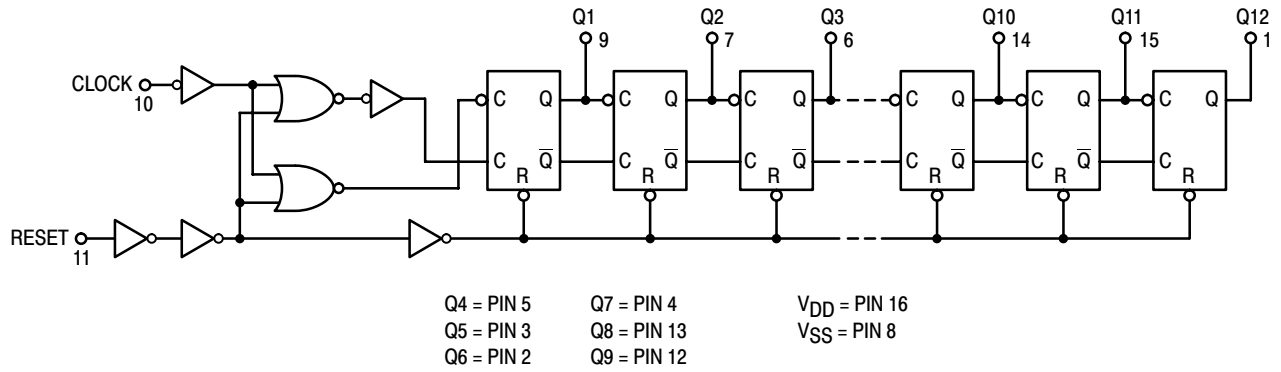
MC14040B

PIN ASSIGNMENT

Q12	1 ●	16	V_{DD}
Q6	2	15	Q11
Q5	3	14	Q10
Q7	4	13	Q8
Q4	5	12	Q9
Q3	6	11	R
Q2	7	10	C
V_{SS}	8	9	Q1

TRUTH TABLE

Clock	Reset	Output State
⌐	0	No Change
⌐	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM

Q4 = PIN 5   Q7 = PIN 4 V_{DD} = PIN 16
Q5 = PIN 3   Q8 = PIN 13 V_{SS} = PIN 8
Q6 = PIN 2   Q9 = PIN 12

MC14040B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	–55°C		25°C			125°C		Unit
			Min	Max	Min	Typ [4.]	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0	–3.0	—	–2.4	–4.2	—	–1.7	—	mAdc
		5.0	–0.64	—	–0.51	–0.88	—	–0.36	—	
		10	–1.6	—	–1.3	–2.25	—	–0.9	—	
		15	–4.2	—	–3.4	–8.8	—	–2.4	—	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.42~\mu A/kHz)~f + I_{DD}$							µAdc
		10	$I_T = (0.85~\mu A/kHz)~f + I_{DD}$							
		15	$I_T = (1.43~\mu A/kHz)~f + I_{DD}$							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50~pF) + (C_L - 50)~Vfk$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.
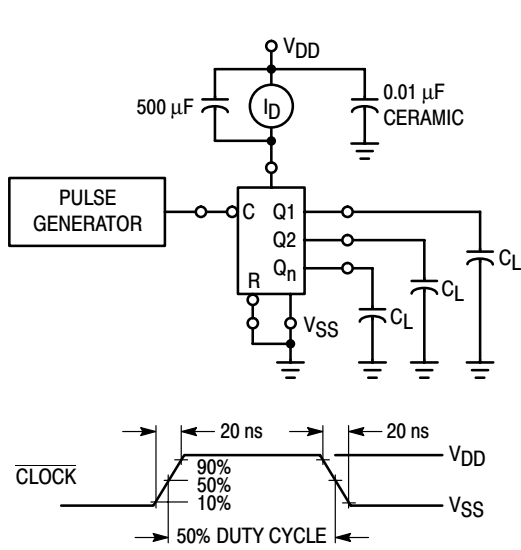
MC14040B

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	260 115 80	520 230 160	ns
Clock to Q12 t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 ns		5.0 10 15	— — —	1625 720 500	3250 1440 1000	ns
Propagation Delay Time Reset to Q_n t_{PHL} = (1.7 ns/pF) C_L + 485 ns t_{PHL} = (0.86 ns/pF) C_L + 182 ns t_{PHL} = (0.5 ns/pF) C_L + 145 ns	t_{PHL}	5.0 10 15	— — —	370 155 115	740 310 230	ns
Clock Pulse Width	t_{WH}	5.0 10 15	385 150 115	140 55 38	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	No Limit			ns
Reset Pulse Width	t_{WH}	5.0 10 15	960 360 270	320 120 80	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	130 50 30	65 25 15	— — —	ns

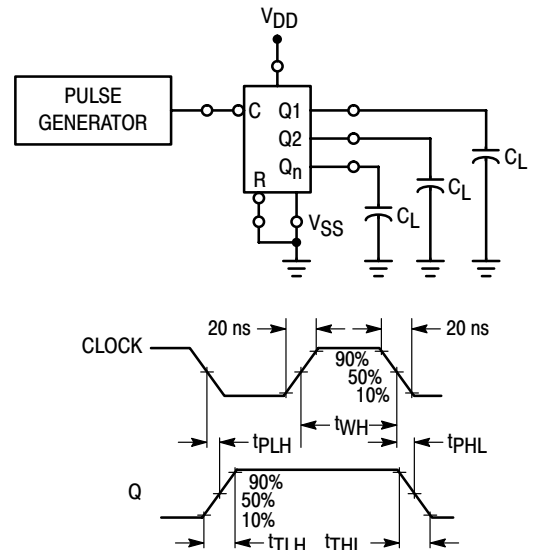7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
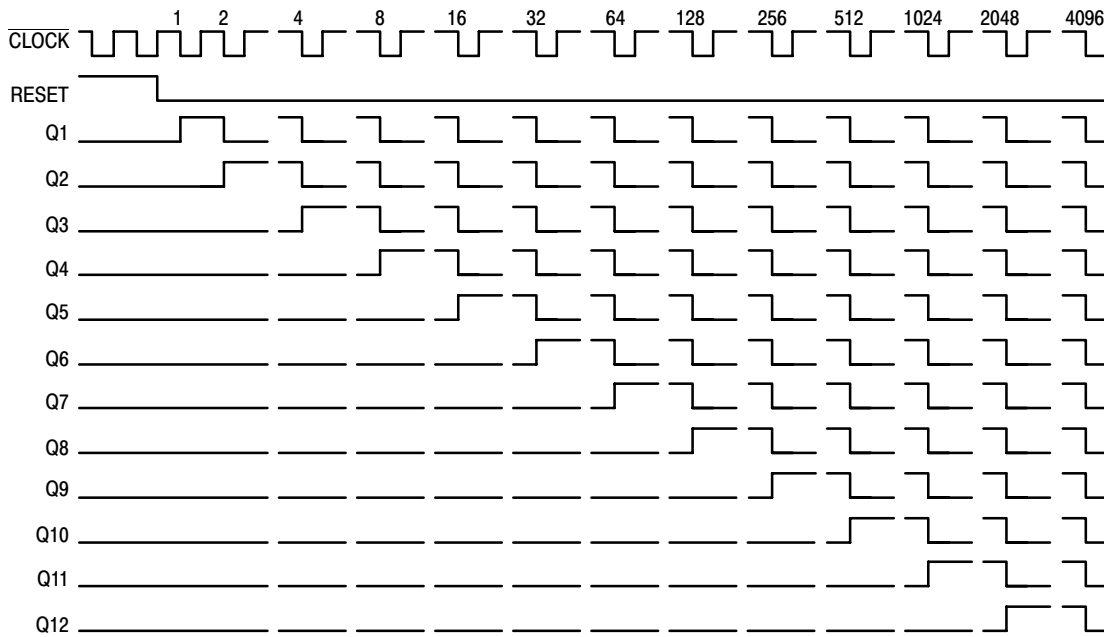
MC14040B

Figure 1. Power Dissipation Test Circuit and Waveform

Figure 2. Switching Time Test Circuit and Waveforms

Figure 3. Timing Diagram

MC14040B

APPLICATIONS INFORMATION

TIME–BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.
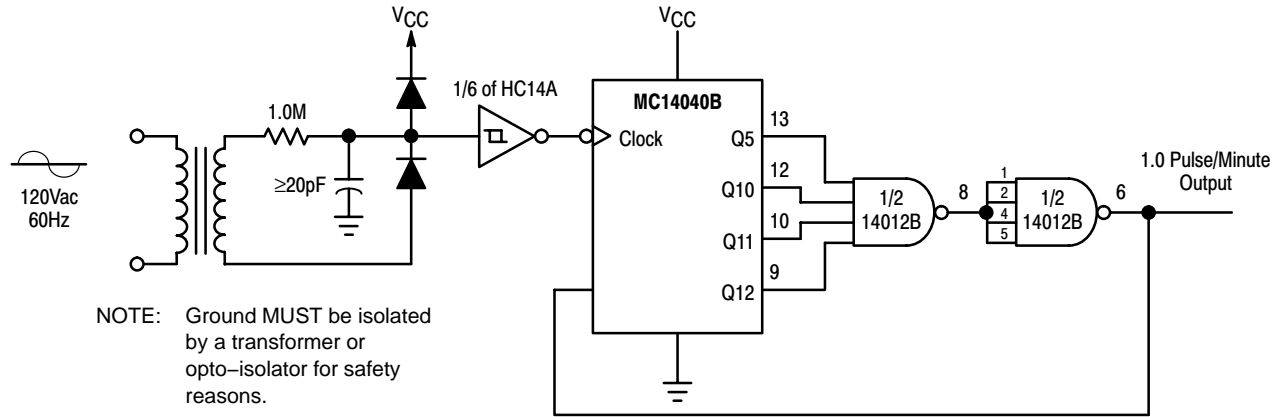

Figure 4. Time–Base Generator