



OCTAL BIDIRECTIONAL TRANSCEIVER WITH 8-BIT PARITY GENERATOR CHECKER (3-STATE OUTPUTS)

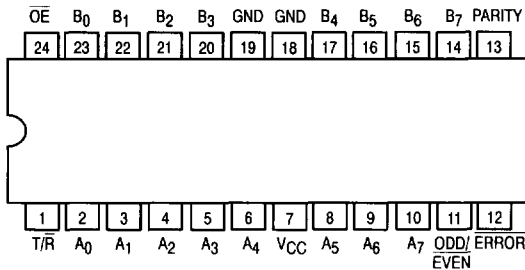
The MC74F657A and MC74F657B are Octal Bidirectional Transceivers with an 8-bit parity Generator/Checker and 3-state outputs.

The A and B options are faster versions of the F657 and contain eight non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker. These devices are intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A ports and 64 mA at the B ports. The Transmit/Receiver (T/R) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

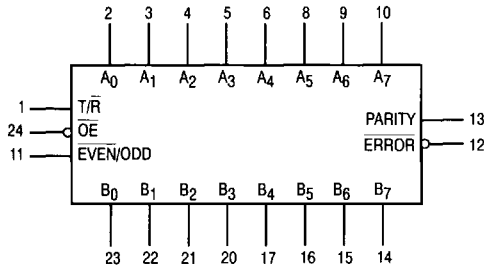
- High-Impedance NPN Base Input for Reduced Loading (20 μ A in HIGH and LOW States)
- Ideal in Applications Where High Output Drive and Light Bus Loading are Required (I_{OL} is 20 μ A versus Fast std of 600 μ A)
- Combines F245 and F280A Functions in One Package
- 3-State Outputs
- B Outputs, PARITY, ERROR, Sink 64 mA and Source 15 mA
- 15 mA Source Current
- Input Diodes for Termination Effects
- Glitchless Outputs During Power Up and Power Down
- High Impedance Outputs During Power Off
- ESD Protection > 4000 Volts

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PIN ASSIGNMENT



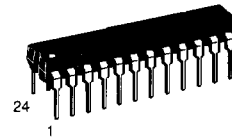
LOGIC SYMBOL



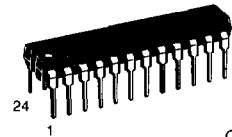
MC74F657A,B

**OCTAL BIDIRECTIONAL
TRANSCEIVER WITH 8-BIT PARITY
GENERATOR CHECKER
(3-STATE OUTPUTS)**

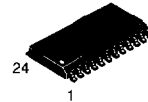
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 758-01**



**N SUFFIX
PLASTIC
CASE 724-03**



**DW SUFFIX
SOIC
CASE 751E-03**

ORDERING INFORMATION

MC74FXXXAJ/BJ	Ceramic
MC74FXXXAN/BN	Plastic
MC74FXXXADW/BDW	SOIC

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GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-3.0/-15	mA
I _{OL}	Output Current — Low	74			24/64	mA

FUNCTION TABLE

Number of Inputs That are High	Inputs			Input/Output	Outputs	
	OE	T/R	Even/Odd	Parity	Error	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	L	Receive

Number of Inputs That are High	Inputs			Input/Output	Outputs	
	OE	T/R	Even/Odd	Parity	Error	Outputs Mode
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't Care	H	X	X	Z	Z	Z

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = HIGH impedance state.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions			
			Min	Typ	Max					
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage			
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage			
V _{IK}	Input Clamp Diode Voltage			-0.73	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA			
V _{OH}	Output HIGH Voltage	All Outputs	74	2.4			V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V	
				2.7	3.4				V _{CC} = 4.75 V	
		B0-B7 PARITY, ERROR	74	2.0			V	I _{OH} = -15 mA	V _{CC} = 4.5 V	
V _{OL}	Output LOW Voltage	A0-A7	74		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN	
		B0-B7 PARITY, ERROR	74		0.4	0.55	V	I _{OL} = 64 mA		
I _{IH}	Input HIGH Current	T/ \bar{R} , \overline{OE} , $\overline{EVEN/ODD}$				100	μ A	V _{CC} = 0 V, V _{IN} = 7.0 V		
		A0-A7				2.0	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V		
		B0-B7, PARITY				1.0		V _{CC} = 5.5 V, V _{IN} = 5.5 V		
		$\overline{EVEN/ODD}$					20	μ A	V _{CC} = MAX, V _{IN} = 2.7 V	
		T/ \bar{R} , \overline{OE}					40			
I _{IL}	Input LOW Current	$\overline{EVEN/ODD}$				-20	μ A	V _{CC} = MAX, V _{IN} = 0.5 V		
		T/ \bar{R} , \overline{OE}				-40				
I _{IH} +I _{OZH}	Off-State Current HIGH Level Voltage Applied	A0-A7 B0-B7 PARITY				70	μ A	V _{CC} = MAX, V _{OUT} = 2.7 V		
I _{IL} +I _{OZL}	Off-State Current LOW Level Voltage Applied					-70		V _{CC} = MAX, V _{OUT} = 0.5 V		
I _{OZH}	Off-State Output Current, High-Level Voltage Applied	ERROR				50	μ A	V _{CC} = MAX, V _{OUT} = 2.7 V		
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied					-50		V _{CC} = MAX, V _{OUT} = 0.5 V		
I _{OS}	Output Short Circuit Current (Note 2)	A _n Outputs		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V		
		PARITY, B _n Outputs, ERROR		-100		-225				
I _{CC}	Total Supply Current	I _{CCH}			90	135	mA	V _{CC} = MAX		
		I _{CCL}			106	150				
		I _{CCZ}			98	145				

NOTES:

- For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at one time, nor for more than 1 second.

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F657A

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	2.0		7.0	2.0	7.5	ns
		2.0		7.0	2.0	7.5	
t _{PLH} t _{PHL}	Propagation Delay A _n to PARITY	6.0		13	5.5	14	ns
		6.5		13	6.5	14	
t _{PLH} t _{PHL}	Propagation Delay EVEN/ODD to PARITY, ERROR	4.5		10.5	4.5	11	ns
		4.5		10.5	4.5	11.5	
t _{PLH} t _{PHL}	Propagation Delay B _n to ERROR	7.0		18	6.5	19	ns
		7.0		18	6.5	19	
t _{PLH} t _{PHL}	Propagation Delay PARITY to ERROR	8.0		14	7.0	15	ns
		7.0		14	7.0	15	
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	3.0		8.0	3.0	9.0	ns
		4.0		9.0	4.0	10	
t _{PHZ} t _{PLZ}	Output Disable Time from HIGH or LOW Level	2.0		7.5	2.0	8.0	ns
		2.0		6.0	2.0	6.5	

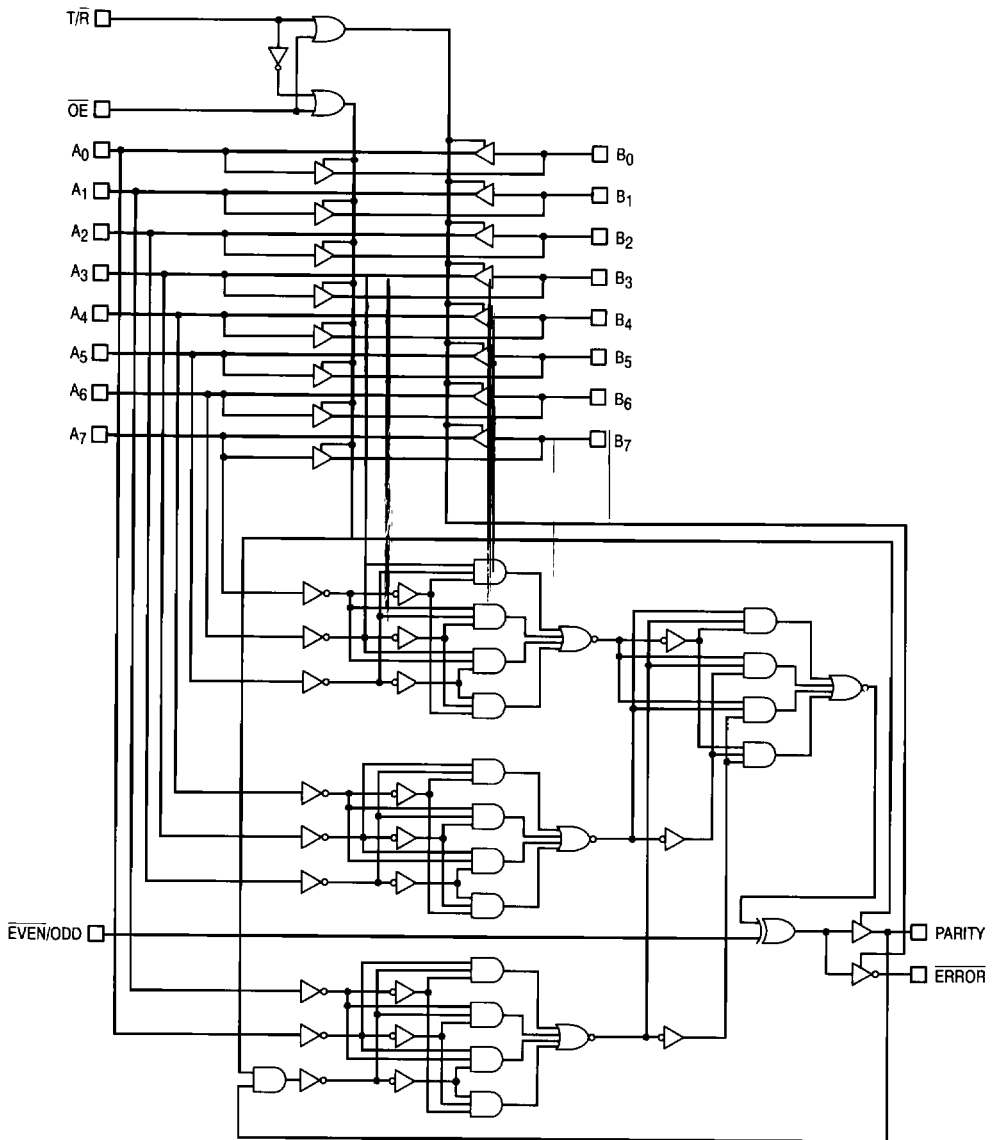
F657B

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	2.0		6.0	2.0	6.5	ns
		2.0		6.0	2.0	6.5	
t _{PLH} t _{PHL}	Propagation Delay A _n to PARITY	4.5		11.5	4.5	13	ns
		4.5		11.5	4.5	13	
t _{PLH} t _{PHL}	Propagation Delay EVEN/ODD to PARITY, ERROR	2.0		7.5	2.0	8.5	ns
		2.0		7.5	2.0	8.5	
t _{PLH} t _{PHL}	Propagation Delay B _n to ERROR	4.0		15	3.5	16	ns
		4.0		15	3.5	16	
t _{PLH} t _{PHL}	Propagation Delay PARITY to ERROR	5.0		11	4.0	12	ns
		5.0		11	4.0	12	
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	2.0		7.0	2.0	8.0	ns
		2.0		7.0	2.0	8.0	
t _{PHZ} t _{PLZ}	Output Disable Time from HIGH or LOW Level	2.0		6.0	2.0	6.5	ns
		2.0		6.0	2.0	6.5	

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LOGIC DIAGRAM



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