FAIRCHILD SEMICONDUCTOR™

March 1998

74F379
Quad Parallel Register with Enable

General Description

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs
- Guaranteed 4000V minimum ESD protection

Features

- Edge triggered D-type inputs

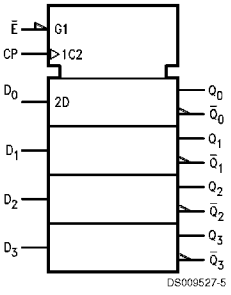
Ordering Code:

Commercial	Military	Package Number	Package Description
74F379PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F379DM (QB)	J16A	16-Lead Ceramic Dual-In-Line
74F379SC (Note 1)		M16A	16-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F379SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F379FM (QB)	W16A	16-Lead Cerpack
	54F379LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols

IEEE/IEC



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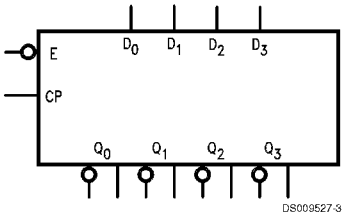

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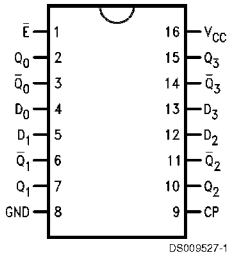
Connection Diagrams

Pin Assignment
DIP, SOIC and Flatpak



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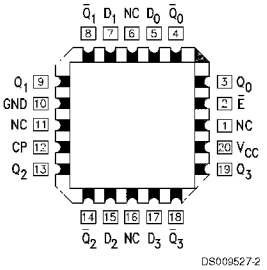
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
D_0–D_3	Data Inputs	1.0/1.0	20 µA/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs	50/33.3	–1 mA/20 mA

Functional Description

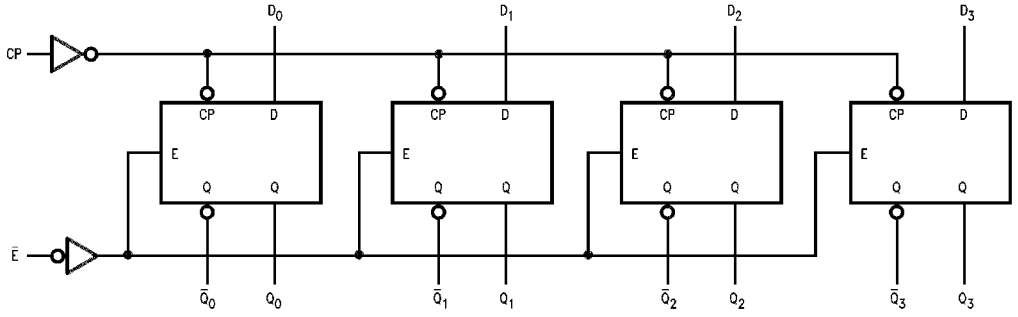
The 'F379 consists of four edge-triggered D-Type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ is input HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⌐	X	NC	NC
L	⌐	H	H	L
L	⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltge (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter			54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage			2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage					−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F	10% V_{CC}	2.5					I_{OH} = −1 mA
		74F	5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F	10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F				20.0	µA	Max	V_{IN} = 2.7V
		74F				5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F				100	µA	Max	V_{IN} = 7.0V
		74F				7.0			
I_{CEX}	Output HIGH Leakage Current	54F				250	µA	Max	V_{OUT} = V_{CC}
		74F				50			
V_{ID}	Input Leakage Test	74F		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current					−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current			−60		−150	mA	Max	V_{OUT} = 0V
I_{CCL}	Power Supply Current				28	40	mA	Max	V_O = LOW

AC Electrical Characteristics

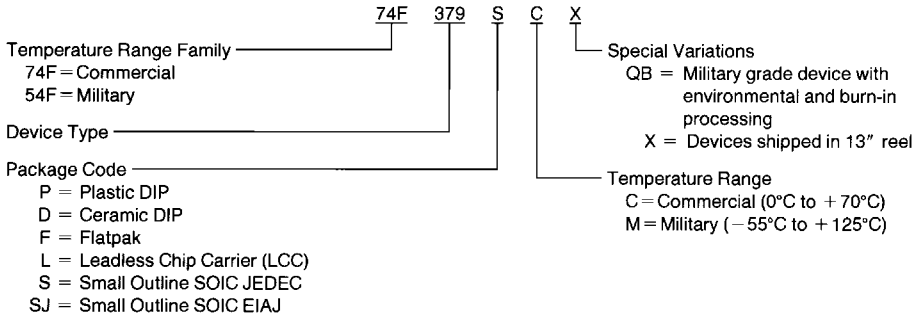
Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units
f_{max}	Maximum Clock Frequency	100	140		75		100		MHz
t_{PLH}	Propagation Delay	3.5	5.0	6.5	3.0	8.5	3.5	7.5	ns
t_{PHL}	CP to Q_n, $\overline{Q}_n$	5.0	6.5	8.5	4.0	10.0	5.0	9.5	

AC Operating Requirements

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	3.0		4.0			3.0	ns
$t_s(L)$	D_n to CP	3.0		4.0			3.0	
$t_h(H)$	Hold Time, HIGH or LOW	1.0		2.0			1.0	
$t_h(L)$	D_n to CP	1.0		2.0			1.0	
$t_s(H)$	Setup Time, HIGH or LOW	6.0		8.0			6.0	ns
$t_s(L)$	$\overline{E}$ to CP	6.0		8.0			6.0	
$t_h(H)$	Hold Time, HIGH or LOW	0		0			0	
$t_h(L)$	$\overline{E}$ to CP	0		0			0	
$t_w(H)$	CP Pulse Width	4.0		5.0			4.0	ns
$t_w(L)$	HIGH or LOW	5.0		7.0			5.0	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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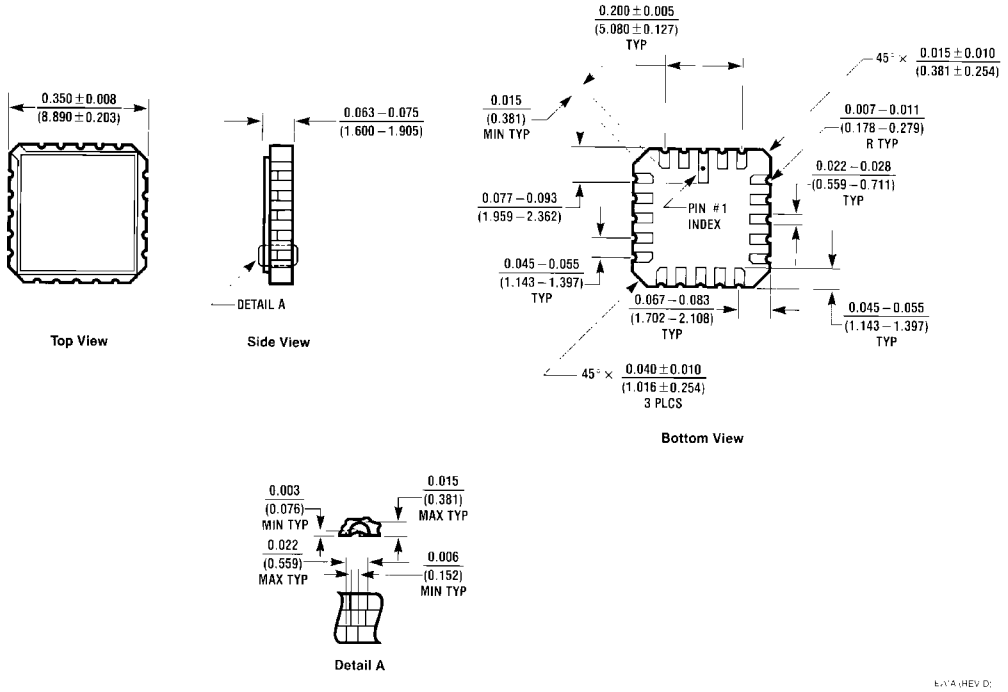
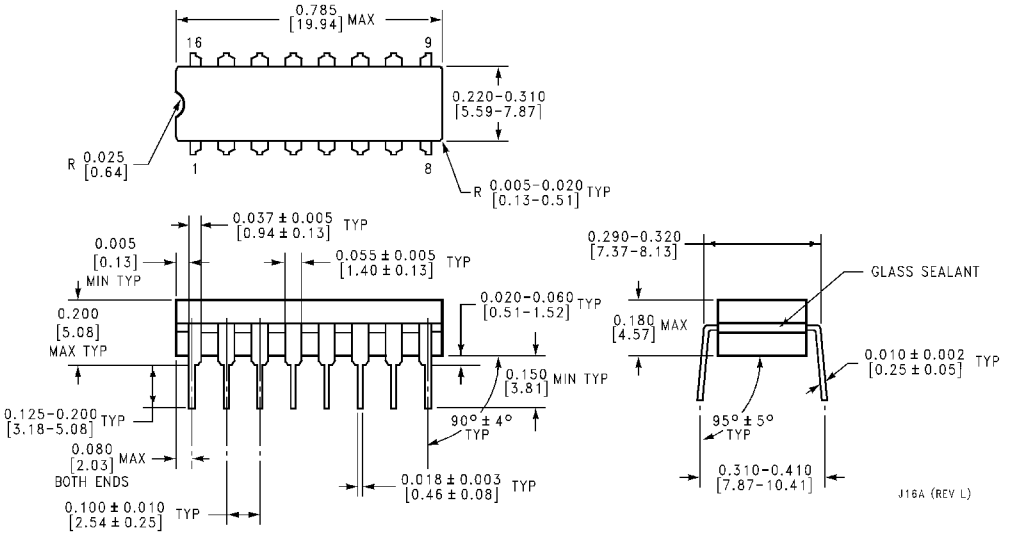
Physical Dimensions inches (millimeters) unless otherwise noted

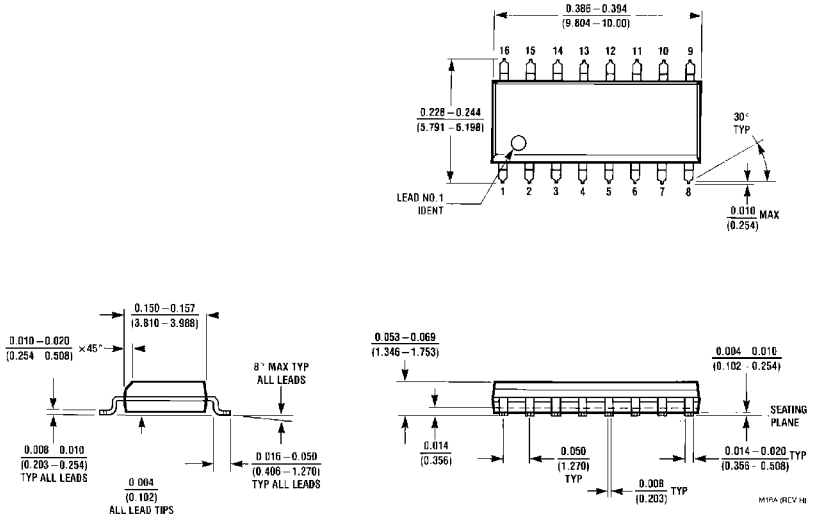


20-Lead Ceramic Leadless Chip Carrier (L)
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

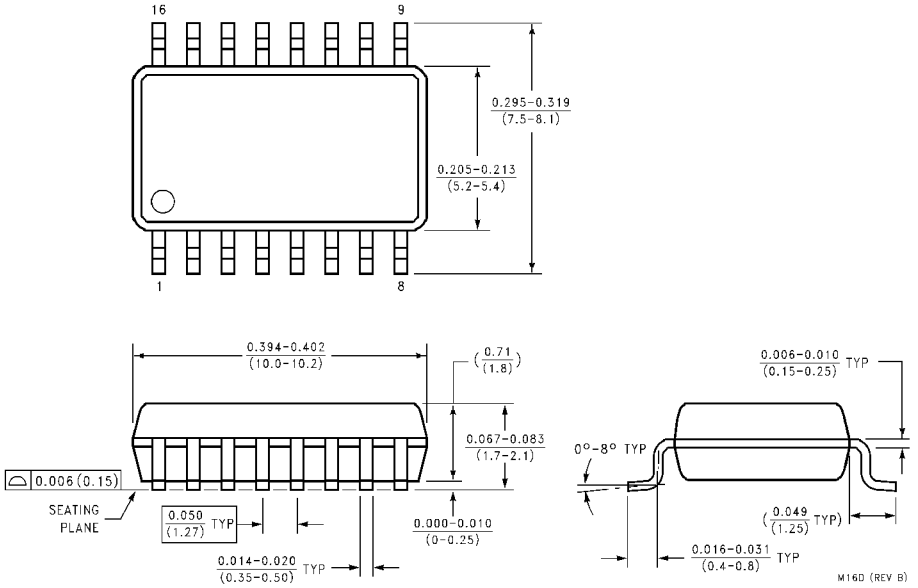


16-Lead Ceramic Dual-In-Line Package (D)
Package Number J16A

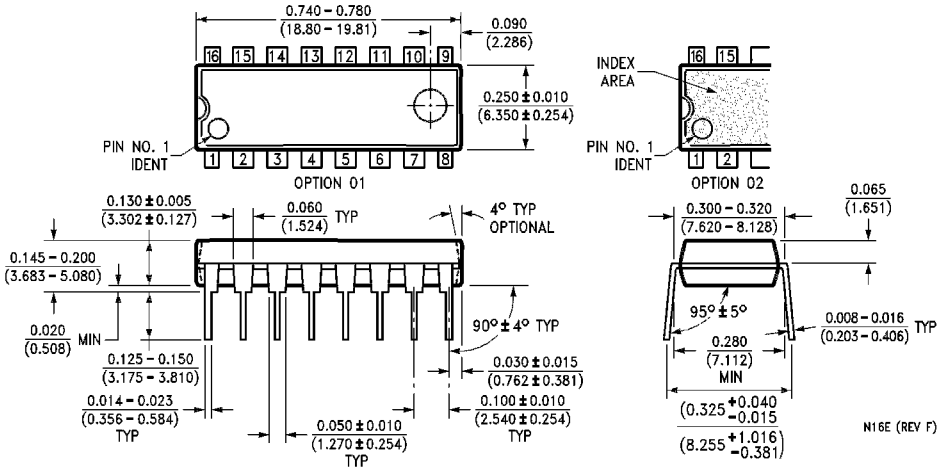


16-Lead (0.150" Wide) Molded Small Outline Integrated Circuit (S)
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

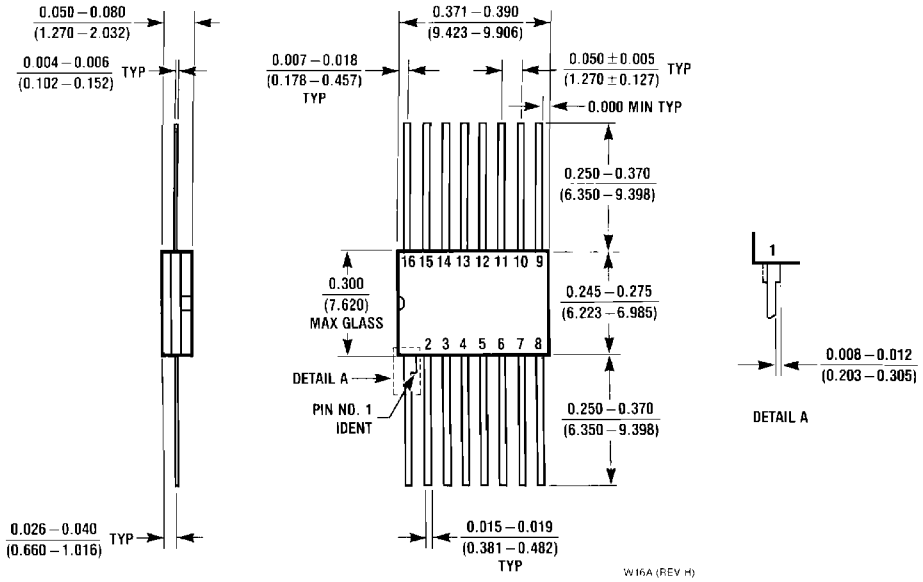


16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M16D



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flatpak (F)
Package Number W16A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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