

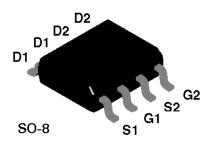
# NDS8961 Dual N-Channel Enhancement Mode Field Effect Transistor

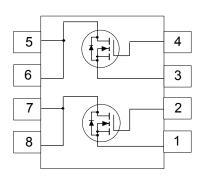
# **General Description**

SO-8 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

# **Features**

- High density cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	NDS8961	Units
DSS	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
D	Drain Current - Continuous (Note 1a)	3.1	А
	- Pulsed	10	
$P_{D}$	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
$T_J$ , $T_{STG}$	Operating and Storage Temperature Range	-55 to 150	°C
THERMA	L CHARACTERISTICS		
R <sub>BJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R <sub>⊕JC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS						•
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
DSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V				1	μΑ
			T <sub>J</sub> = 55°C			10	μΑ
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate - Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V				-100	nA
ON CHAR	ACTERISTICS (Note 2)						•
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.6	3	V
			T <sub>J</sub> = 125°C	0.7	1.2	2	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.1 \text{ A}$			0.072	0.1	Ω
			T <sub>J</sub> = 125°C		0.107	0.18	
		$V_{GS} = 4.5 \text{ V}, I_D = 2.6 \text{ A}$	<u> </u>		0.116	0.15	
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V		10			Α
		$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$		4			
FS	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 3.1 \text{ A}$			4.3		S
OYNAMIC	CHARACTERISTICS			-			•
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$			190		pF
Coss	Output Capacitance				120		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				40		pF
WITCHIN	IG CHARACTERISTICS (Note 2)						
D(on)	Turn - On Delay Time	$V_{DD} = 10 \text{ V}, I_{D} = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$			7	15	ns
r	Turn - On Rise Time				15	30	ns
D(off)	Turn - Off Delay Time				14	28	ns
, f	Turn - Off Fall Time				3	6	ns
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 10 V,			7.1	10	nC
$Q_{gs}$	Gate-Source Charge	$I_D = 3.1 \text{ A}, V_{GS} = 10 \text{ V}$			1.2		nC
$Q_{gd}$	Gate-Drain Charge				1.9		nC

<b>ELECTRICAL CHARACTERISTICS</b> (T <sub>A</sub> = 25°C unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I <sub>s</sub>	Maximum Continuous Drain-Source Diode Forward Current				1.3	Α	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)		0.79	1.2	V	

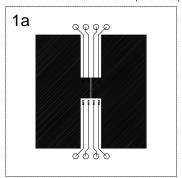
#### Notes

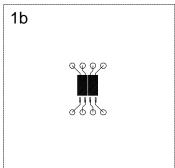
1. R<sub>BA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BA</sub> is guaranteed by design while R<sub>BCA</sub> is determined by the user's board design.

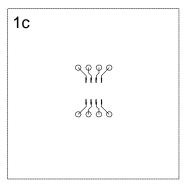
$$P_D(t) = \frac{T_J - T_A}{R_{\theta,JA}(t)} = \frac{T_J - T_A}{R_{\theta,JC} + R_{\theta,CA}(t)} = I_D^2(t) \times R_{DS(ON)} g_{T_J}$$

Typical  $R_{_{BJA}}$  for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



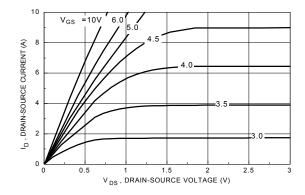




Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2.0%.

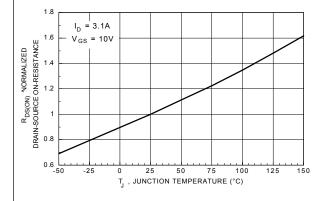
# **Typical Electrical Characteristics**



2.5 V<sub>GS</sub> = 3.5V V

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.



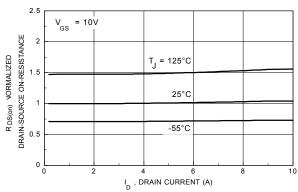
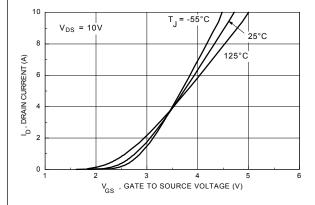


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Drain Current and Temperature.



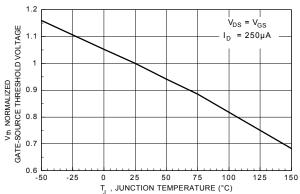


Figure 5. Transfer Characteristics.

Figure 6. Gate Threshold Variation with Temperature.

# **Typical Electrical Characteristics**

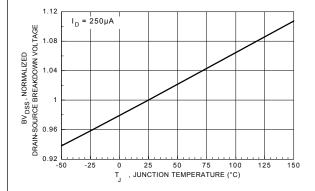


Figure 7. Breakdown Voltage Variation with Temperature.

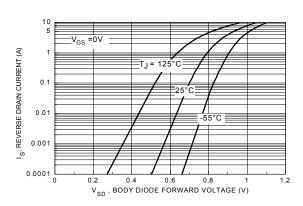


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

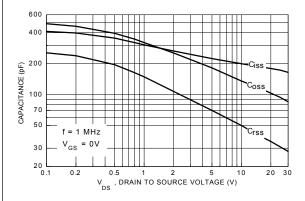


Figure 9. Capacitance Characteristics.

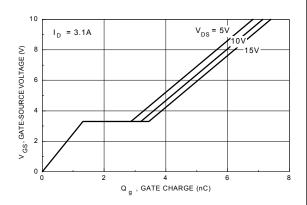


Figure 10. Gate Charge Characteristics.

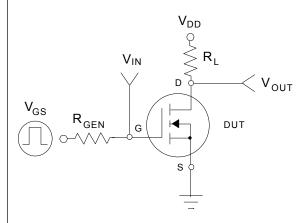


Figure 11. Switching Test Circuit.

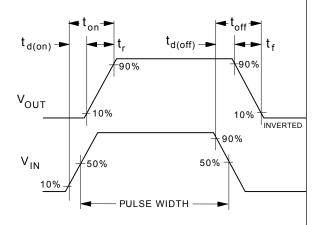


Figure 12. Switching Waveforms.

# **Typical Electrical and Thermal Characteristics**

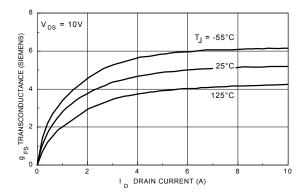


Figure 13. Transconductance Variation with Drain Current and Temperature.

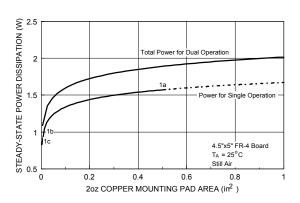


Figure 14. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

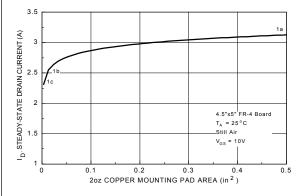


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

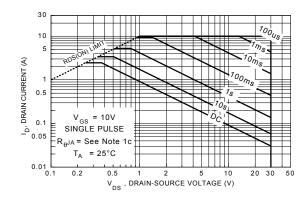


Figure 16. Maximum Safe Operating Area.

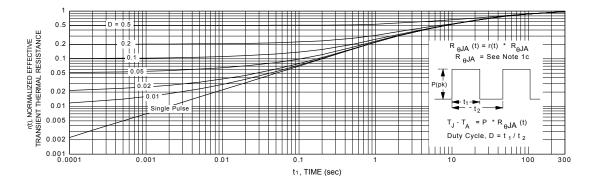


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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