

## RMPA39000

### 37–40 GHz GaAs MMIC Power Amplifier

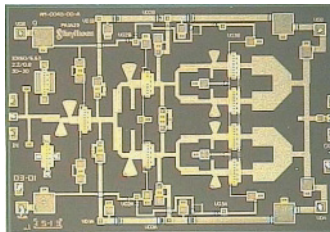
#### General Description

The Fairchild Semiconductor RMPA39000 is a high efficiency power amplifier designed for use in point to point and point to multi-point radios, and various communications applications. The RMPA39000 is a 3-stage GaAs MMIC amplifier utilizing our advanced 0.15 $\mu$ m gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.

#### Features

- 24dB small signal gain (typ.)
- 29dBm saturated power out (typ.)
- Circuit contains individual source vias
- Chip size 4.28mm x 2.90mm x 50 $\mu$ m

#### Device



#### Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Positive DC Voltage (+5V Typical)	+6	V
Vg	Negative DC Voltage	-2	V
Vdg	Simultaneous (Vd–Vg)	+8	V
I <sub>D</sub>	Positive DC Current	1092	mA
P <sub>IN</sub>	RF Input Power (from 50 $\Omega$ source)	+20	dBm
T <sub>C</sub>	Operating Baseplate Temperature	-30 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +125	°C
R <sub>JC</sub>	Thermal Resistance (Channel to Backside)	17	°C/W

**Electrical Characteristics** 50Ω system, Vd = +5V, Quiescent current (Idq) = 700mA

Parameter	Min	Typ	Max	Units
Frequency Range	37		40	GHz
Gain Supply Voltage (Vg) <sup>1</sup>		-0.15		V
Gain Small Signal at Pin = 0dBm	20	24		dB
Gain Variation vs. Frequency		±1		dB
Power Output at 1dB Compression		28		dBm
Power Output Saturated (Pin = +13dBm)	27.5	29		dBm
Drain Current at Pin = 0dBm		700		mA
Drain Current at P1dB Compression		730		mA
Drain Current at Psat (Pin = +13dBm)		750		mA
Power Added Efficiency (PAE) at P1dB		17		%
OIP3 (17dBm/Tone) (10 MHz Tone Sep.)		36		dBm
Input Return Loss (Pin = -10dBm)		8		dB
Output Return Loss (Pin = -10dBm)		7		dB

**Note:**

1. Typical range of the negative gate voltage is -0.5V to 0.0V to set typical Idq of 700mA.



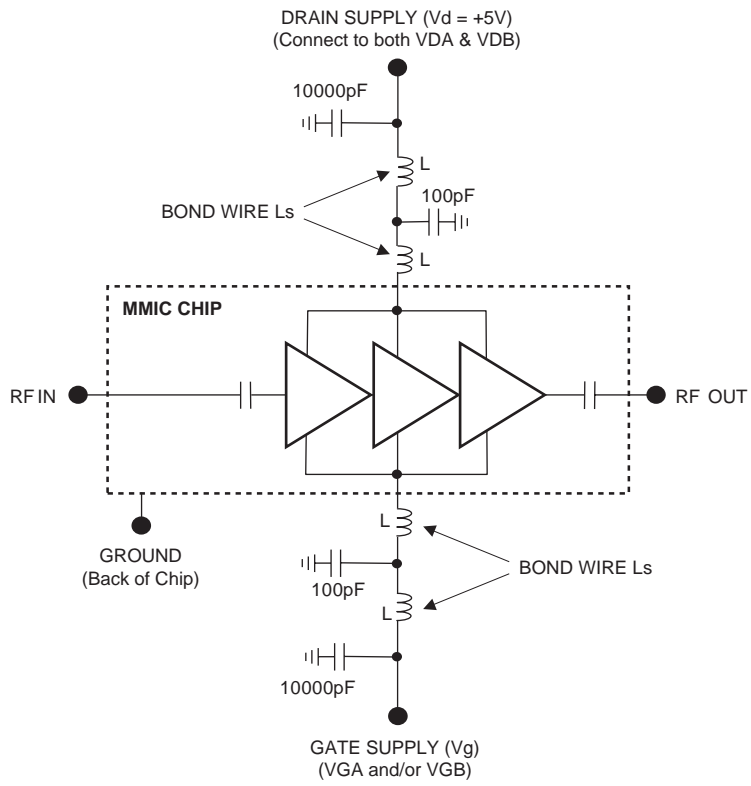
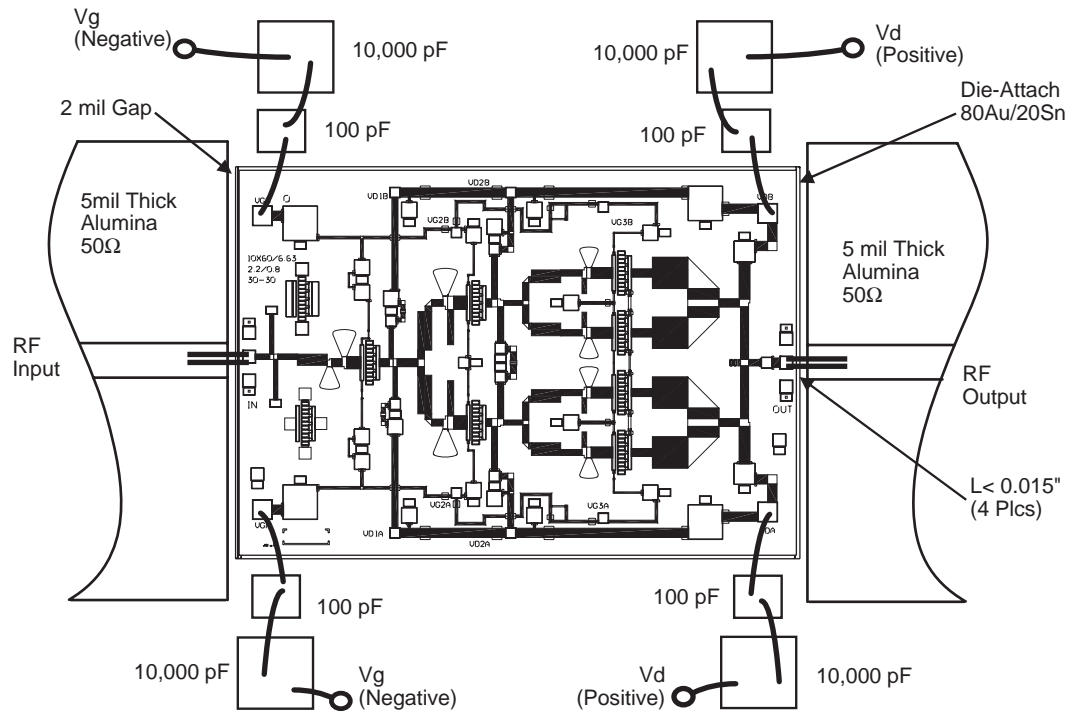


Figure 3. Recommended Application Schematic Circuit Diagram



**Note:**  
 Use 0.003" x 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. Vd should be biased from 1 supply on both sides as shown. Vg can be biased from either or both sides from 1 supply.

**Figure 4. Recommended Assembly and Bonding Diagram**

## Recommended Procedure for Biasing and Operation

**CAUTION: LOSS OF GATE VOLTAGE ( $V_g$ ) WHILE DRAIN VOLTAGE ( $V_d$ ) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.**

The following sequence of steps must be followed to properly test the amplifier.

**Step 1:** Turn off RF input power.

**Step 2:** Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to  $V_g$ .

**Step 3:** Slowly apply positive drain bias supply voltage of +5V to  $V_d$ .

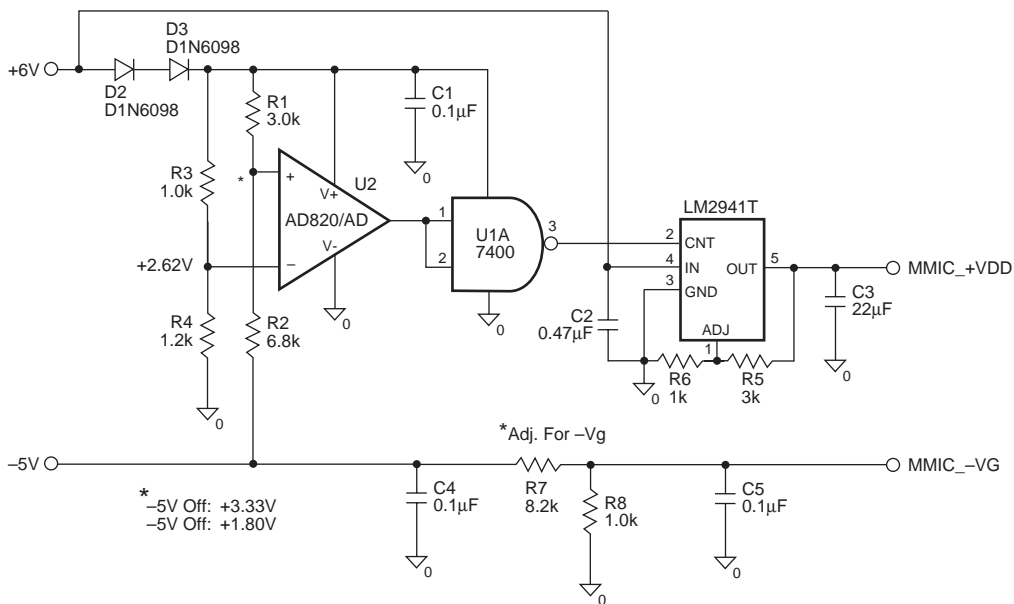
**Step 4:** Adjust gate bias voltage to set the quiescent current of  $I_{dq} = 700\text{mA}$ .

**Step 5:** After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

**Step 6:** Follow turn-off sequence of:

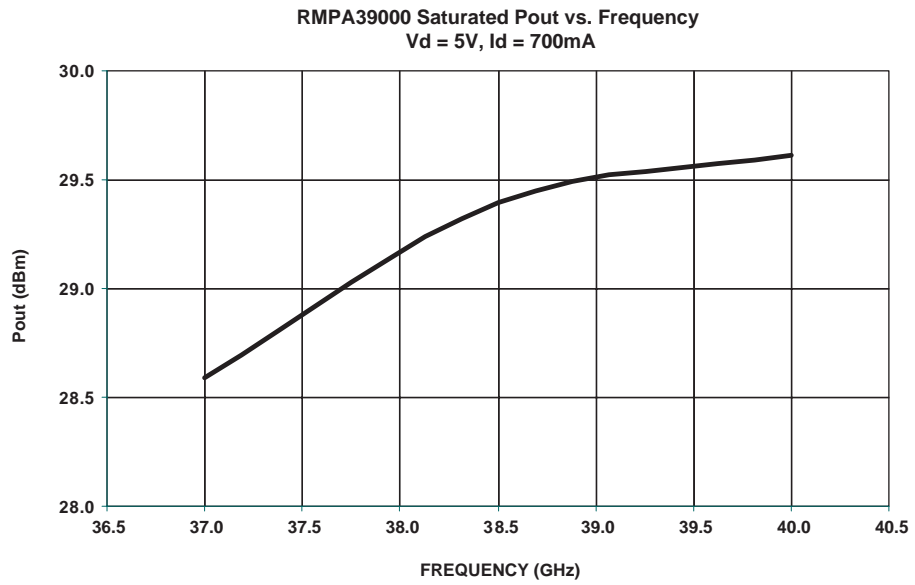
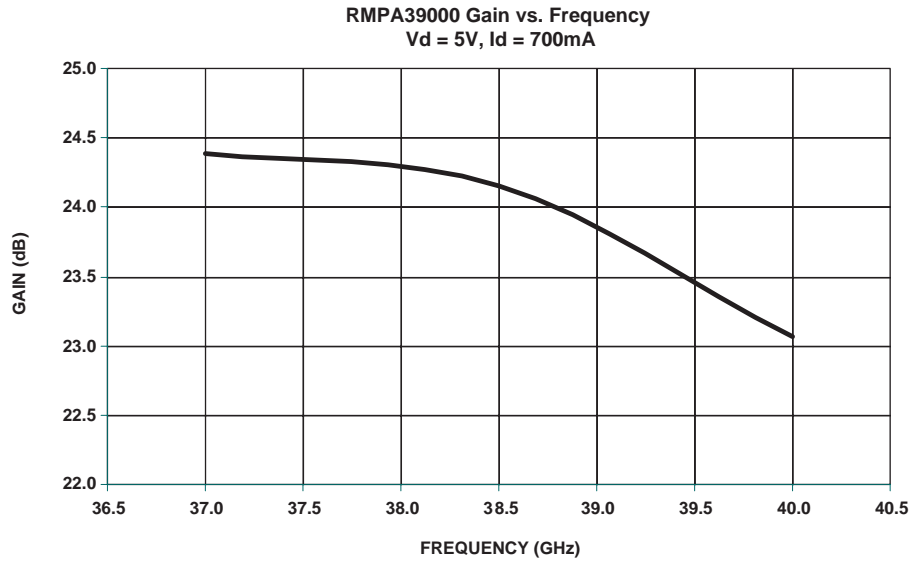
- (i) Turn off RF input power,
- (ii) Turn down and off drain voltage ( $V_d$ ),
- (iii) Turn down and off gate bias voltage ( $V_g$ ).

**Note:** An example auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below.

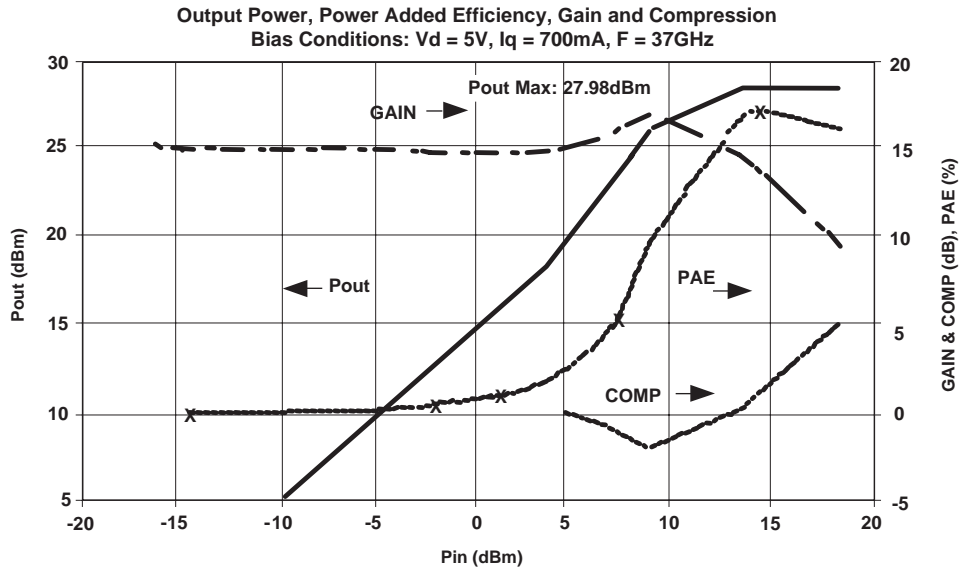
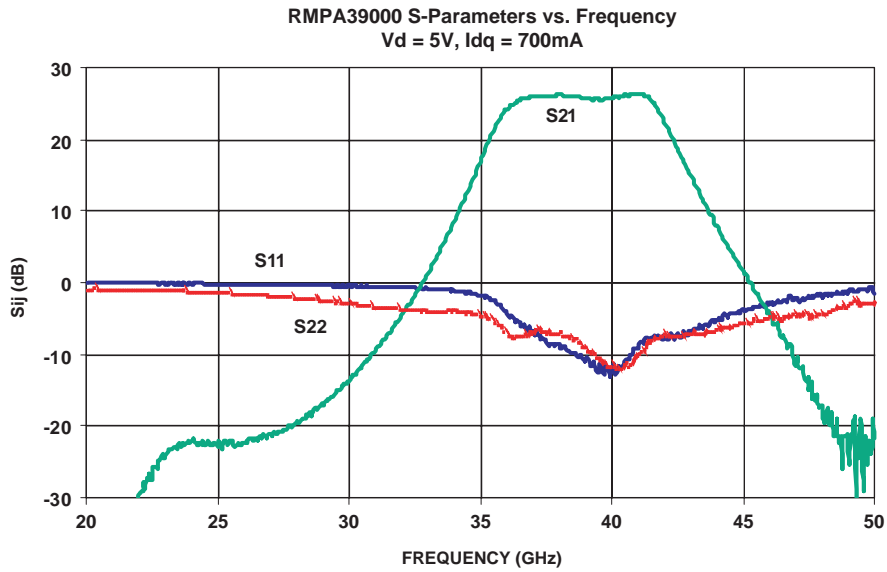


**Figure 5. Application Information Auto-Bias Circuit**

### Typical Characteristics

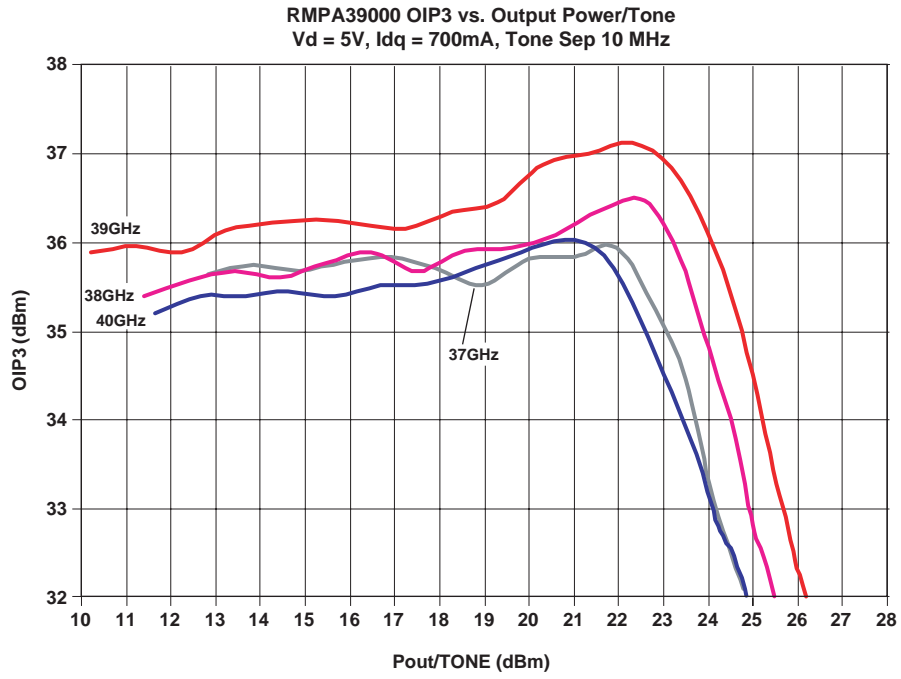


Typical Characteristics (Continued)





### Typical Characteristics (Continued)



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EcoSPARK™	HiSeC™	MSX™	Quiet Series™	TINYOPTO™
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EnSigna™	i-Lo™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	µSerDes™	UltraFET®
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