FAIRCHILD SEMICONDUCTOR®

May 2003

FDN363N

N-Channel PowerTrench® MOSFET
100V, 1A, 240mΩ

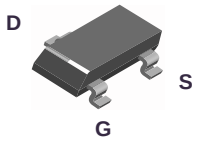
Features

- $r_{DS(ON)}$ = 200mΩ (Typ.), V_{GS} = 10V, I_D = 1A
- Q_g(tot) = 4nC (Typ.), V_{GS} = 10V
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

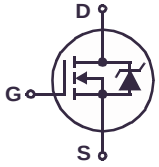
Formerly developmental type 82720

Applications

- DC/DC converters



SuperSOT-3



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, V_{GS} = 10V, $R_{\theta JA}$= 250°C/W)	1	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	8.5	mJ
P_D	Power dissipation	0.5	W
	Derate above 25°C	4	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case SSOT-3	75	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SSOT-3 (Note 2)	250	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SSOT-3 (Note 3)	270	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDN363N	FDN363N	SSOT-3	7''	8mm	3000 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V	-	-	1	µA
		V_{GS} = 0V, T_A = 125°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 1A, V_{GS} = 10V	-	0.200	0.240	Ω
		I_D = 0.5A, V_{GS} = 6V	-	0.250	0.350	
		I_D = 1A, V_{GS} = 10V, T_C = 150°C	-	0.400	0.480	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	200	-	pF
C_{OSS}	Output Capacitance		-	35	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	8	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 50V, I_D = 1A, I_g = 1.0mA	-	4	5.2	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V; V_{DD} = 50V, I_D = 1A, I_g = 1.0mA	-	0.5	0.65	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50V, I_D = 1A, I_g = 1.0mA	-	1.1	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 50V, I_D = 1A, I_g = 1.0mA	-	0.6	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50V, I_D = 1A, I_g = 1.0mA	-	1.0	-	nC
Resistive Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 50V, I_D = 1A, V_{GS} = 10V, R_{GS} = 100Ω	-	-	33	ns
$t_{d(ON)}$	Turn-On Delay Time		-	17	-	ns
t_r	Rise Time		-	15	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	36	-	ns
t_f	Fall Time		-	21	-	ns
t_{OFF}	Turn-Off Time		-	-	86	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 1A	-	-	1.25	V
		I_{SD} = 0.5A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 1A, dI_{SD}/dt = 100A/µs	-	-	35	ns
Q_{RR}	Reverse Recovery Charge	I_{SD} = 1A, dI_{SD}/dt = 100A/µs	-	-	35	nC

Notes:
1: Starting T_J = 25°C, L = 0.68mH, I_{AS} = 5A.
2: $R_{\theta JA}$ is 250 °C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.
3: $R_{\theta JA}$ is 270 °C/W when mounted on a minimum pad.

Typical Characteristics T_A = 25°C unless otherwise noted

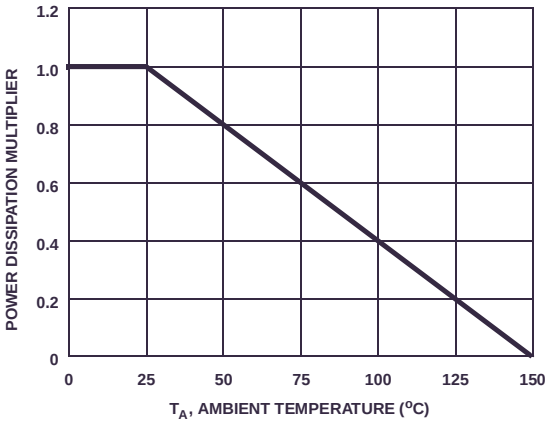


Figure 1. Normalized Power Dissipation vs Ambient Temperature

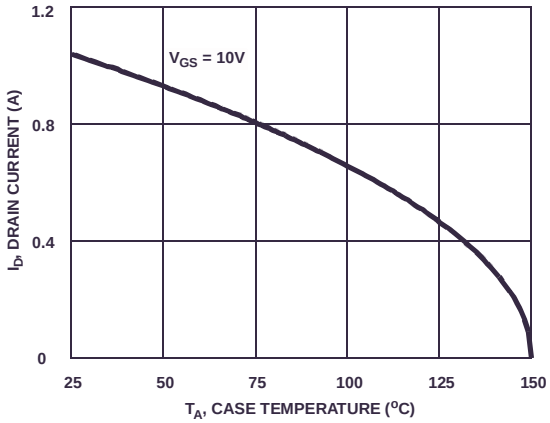


Figure 2. Maximum Continuous Drain Current vs Case Temperature

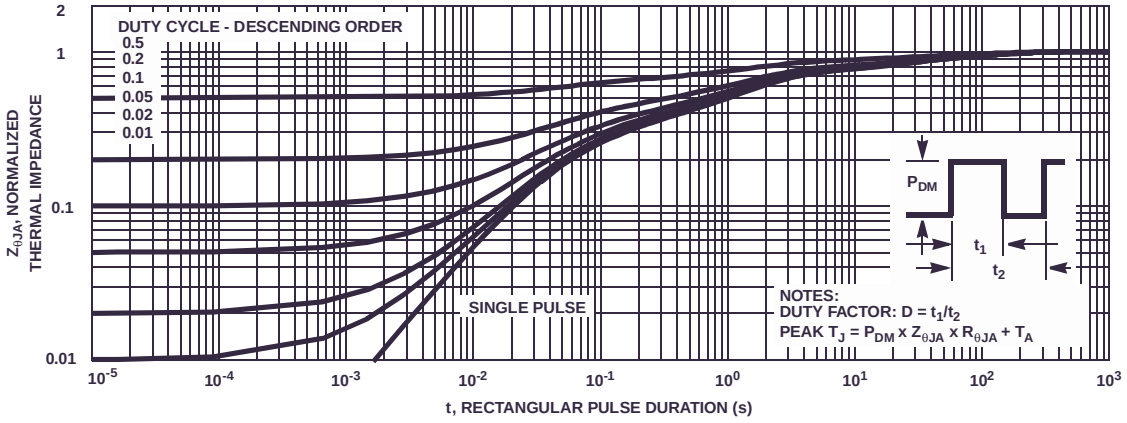


Figure 3. Normalized Maximum Transient Thermal Impedance

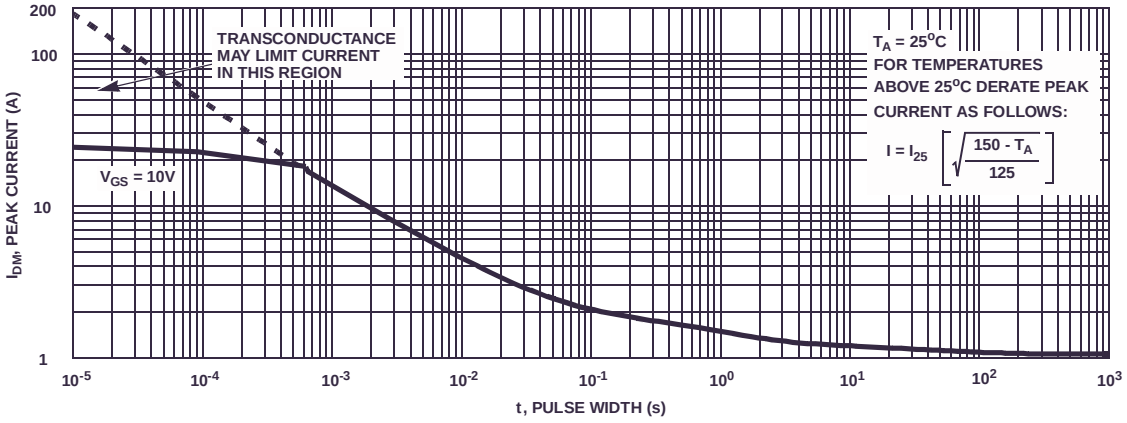


Figure 4. Peak Current Capability

Typical Characteristics T_A = 25°C unless otherwise noted

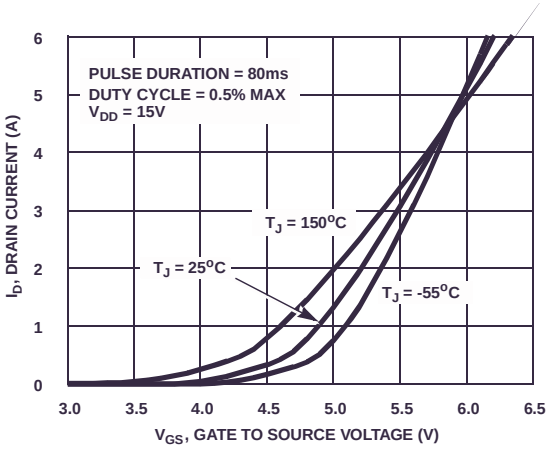


Figure 5. Transfer Characteristics

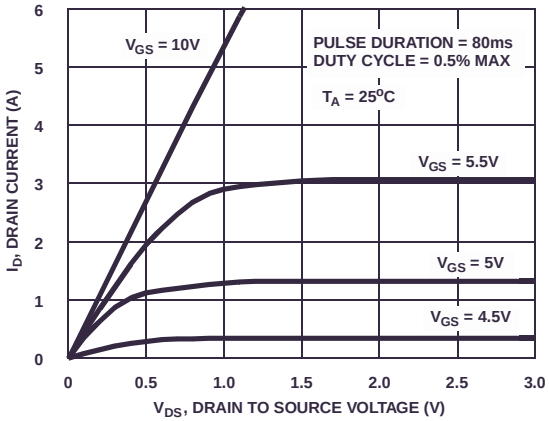


Figure 6. Saturation Characteristics

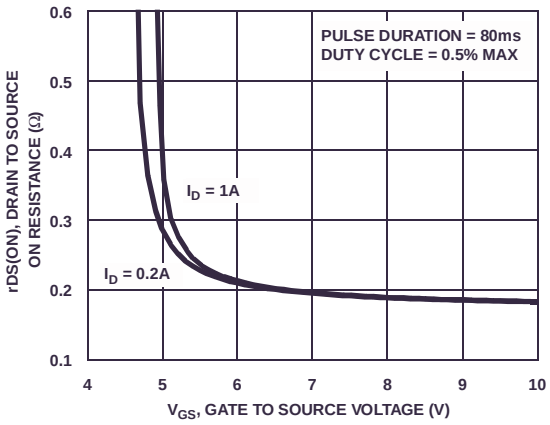


Figure 7. Drain to Source On Resistance vs Gate Voltage and Drain Current

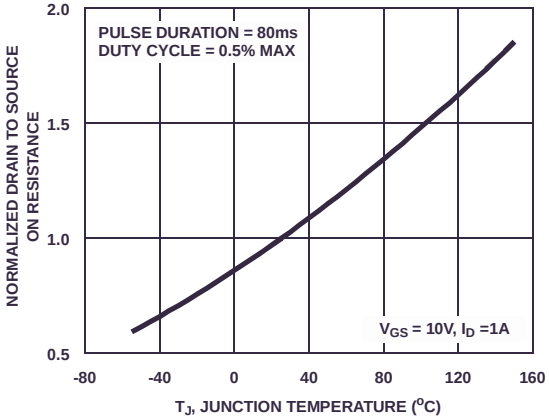


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

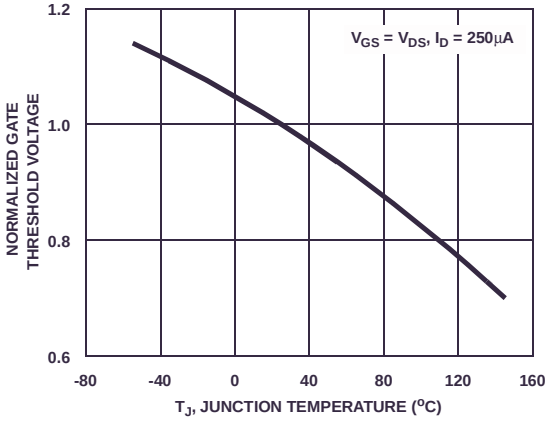


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

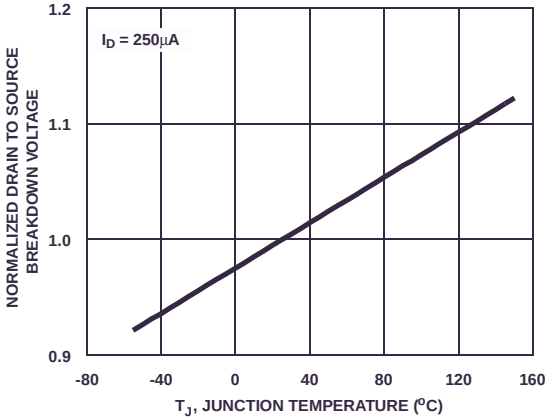


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Typical Characteristics T_A = 25°C unless otherwise noted

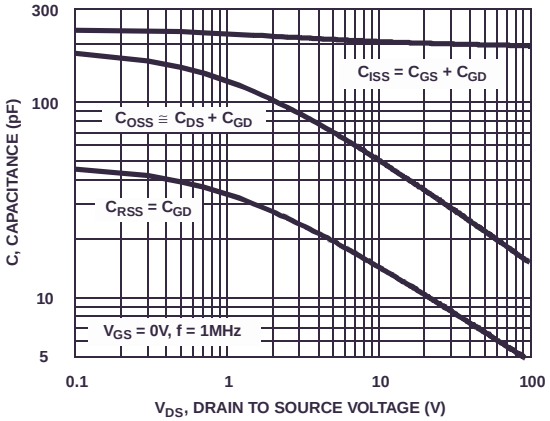


Figure 11. Capacitance vs Drain to Source Voltage

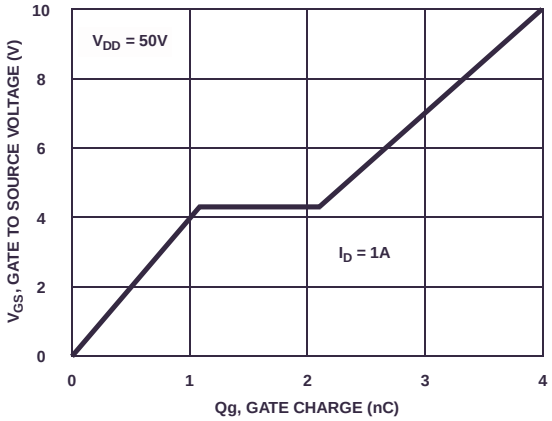


Figure 12. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

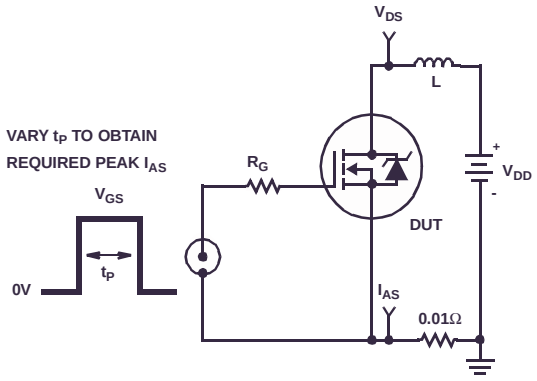


Figure 13. Unclamped Energy Test Circuit

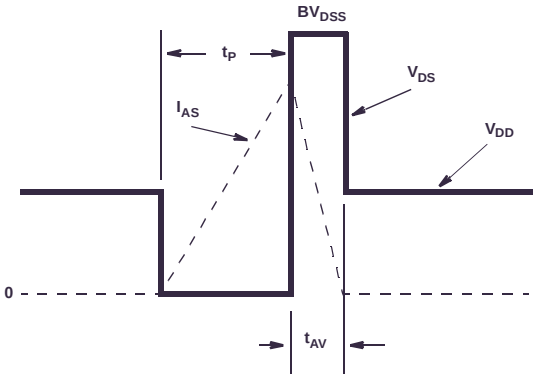


Figure 14. Unclamped Energy Waveforms

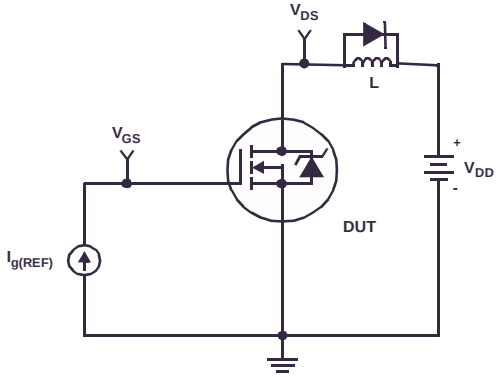


Figure 15. Gate Charge Test Circuit

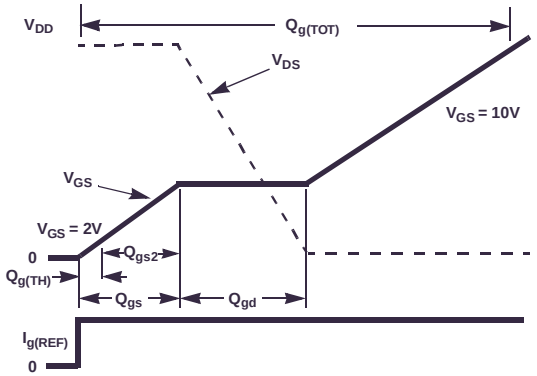


Figure 16. Gate Charge Waveforms

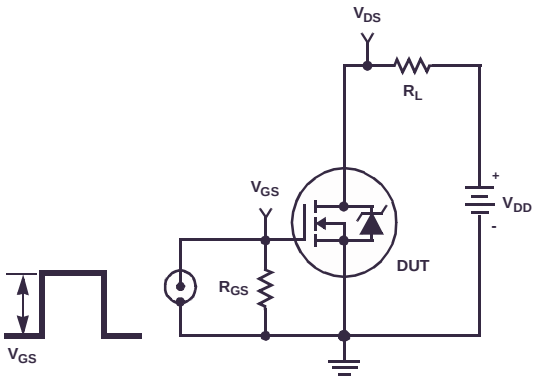


Figure 17. Switching Time Test Circuit

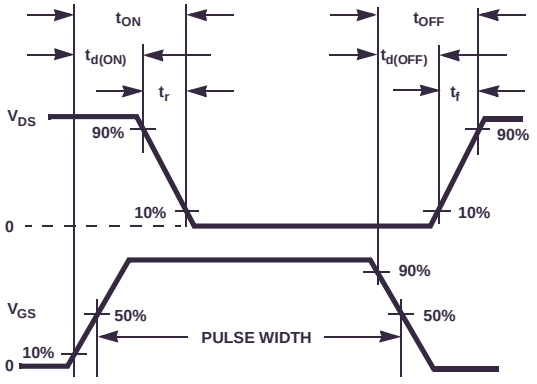
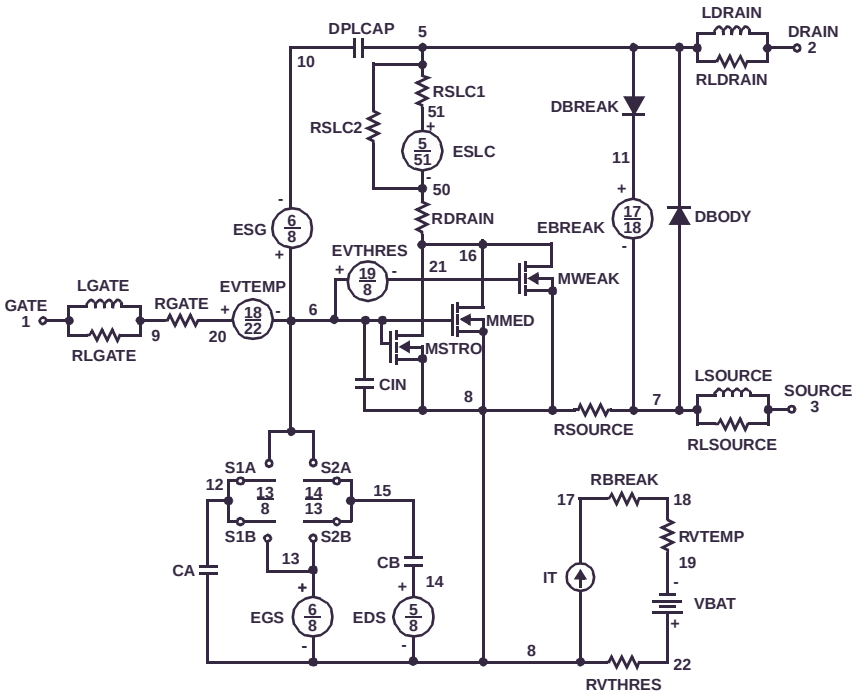


Figure 18. Switching Time Waveforms

PSPICE Electrical Model

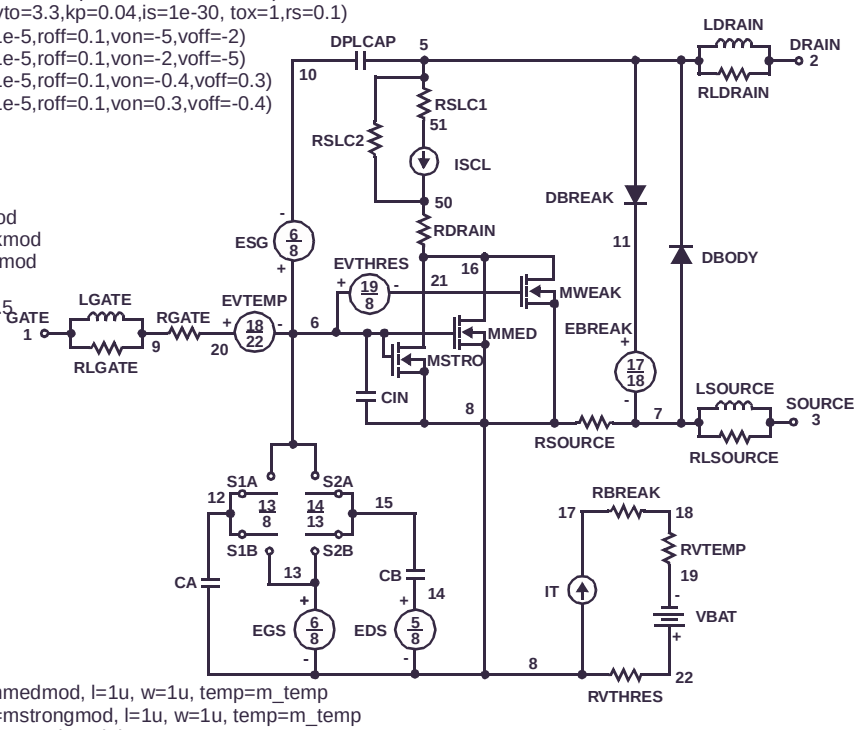
```
.SUBCKT FDN363N  2 1 3 ;       rev May 2003
Ca  12  8 3.5e-10
Cb 15 14 1.2e-10
Cin 6 8 0.19e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 105.5
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 0.7e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 0.23e-9

RLgate 1 9 7.0
RLdrain 2 5 10
RLsource 3 7 2.3

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 13e-3
Rgate 9 20 1.65
RSLC1 5 51 RSLCMOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 160e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*25),2.5))}

.MODEL DbodyMOD D (IS=2.3E-13  RS=2.5e-2 TRS1=2.0e-3 TRS2=4.5e-7
+ CJO=1.4e-10 M=0.56 TT=3.5e-8 XTI=4.2)
.MODEL DbreakMOD D (RS=0.6 TRS1=1.4e-3 TRS2=-5.0e-5)
.MODEL DplcapMOD D (CJO=4.8e-11 IS=1.0e-30 N=10 M=0.5)

.MODEL MstroMOD NMOS (VTO=4.52 KP=17 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)
.MODEL MmedMOD NMOS (VTO=3.72 KP=1.2 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.65 T_ABS=25)
.MODEL MweakMOD NMOS (VTO=3.3 KP=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=16.5 RS=0.1 T_ABS=25)

.MODEL RbreakMOD RES (TC1=1.0e-3 TC2=-1.1e-8)
.MODEL RdrainMOD RES (TC1=3.2e-2 TC2=1.1e-4)
.MODEL RSLCMOD RES (TC1=1.0e-3 TC2=2.9e-6)
.MODEL RsourceMOD RES (TC1=4e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-4.1e-3 TC2=-1.4e-5)
.MODEL RvtempMOD RES (TC1=-3.0e-3 TC2=1.3e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-2.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-5.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.4 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.4)

.ENDS
```



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV May 2003
template FDN363N n2,n1,n3 =m_temp
electrical n2,n1,n3
number m_temp=25
{
var i iscl
dp..model dbodymod =  (isl=2.3e-13,rs=2.5e-2,trs1=2.0e-3,trs2=4.5e-7,cjo=1.4e-10,m=0.56,tt=3.5e-8,xti=4.2)
dp..model dbreakmod = (rs=0.6,trs1=1.4e-3,trs2=-5e-5)
dp..model dplcapmod =  (cjo=4.8e-11,isl=10e-30,nl=10,m=0.5)
m..model mstrongmod = (type=_n,vto=4.52,kp=17,is=1e-30, tox=1)
m..model mmedmod = (type=_n,vto=3.72,kp=1.2,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.3,kp=0.04,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-5,voff=-2)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-2,voff=-5)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-0.4,voff=0.3)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=0.3,voff=-0.4)
c.ca n12 n8 = 3.5e-10
c.cb n15 n14 = 1.2e-10
c.cin n6 n8 = 0.19e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 105.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 0.7e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 0.23e-9

res.rlgate n1 n9 = 7.0
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 2.3
```




```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

res.rbreak n17 n18  = 1, tc1=1.0e-3,tc2=-1.1e-8
res.rdrain n50 n16  = 13e-3, tc1=3.2e-2,tc2=1.1e-4
res.rgate n9 n20 = 1.65
res.rslc1 n5 n51  = 1.0e-6, tc1=1.0e-3,tc2=2.9e-6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7  = 160e-3, tc1=4e-3,tc2=1e-6
res.rvthres n22 n8  = 1, tc1=-4.1e-3,tc2=-1.4e-5
res.rvtemp n18 n19  = 1, tc1=-3.0e-3,tc2=1.3e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/25))** 2.5))
}
}
```

SPICE Thermal Model

REV 20 May 2003

FDN363N_JA Junction Ambient
Copper Area=0.02sq.in

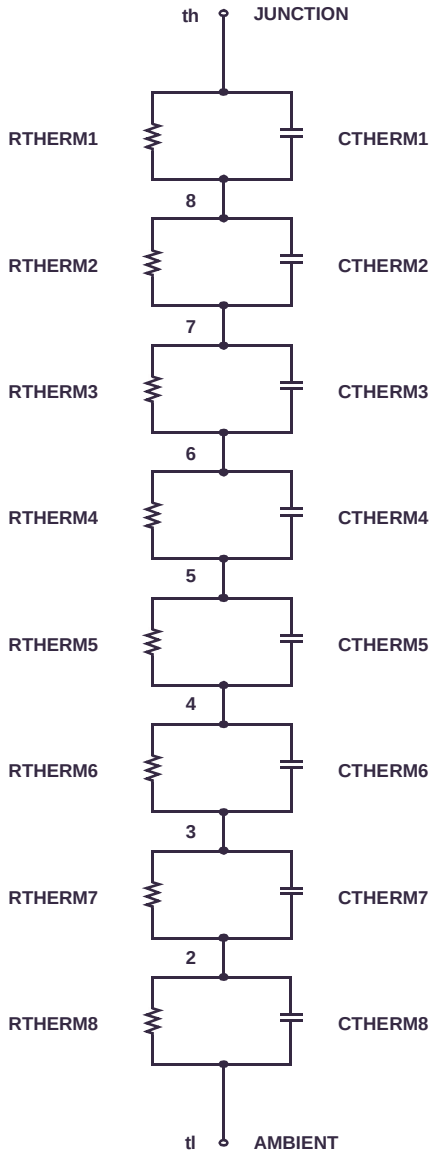
CTHERM1 Junction 8 1.8e-3
CTHERM2 8 7 2.1e-3
CTHERM3 7 6 4.0e-3
CTHERM4 6 5 4.4e-2
CTHERM5 5 4 5.3e-2
CTHERM6 4 3 5.6e-2
CTHERM7 3 2 6.7e-1
CTHERM8 2 Ambient 3.0

RTHERM1 Junction 8 16.0
RTHERM2 8 7 20.5
RTHERM3 7 6 29.4
RTHERM4 6 5 29.5
RTHERM5 5 4 30.0
RTHERM6 4 3 31.0
RTHERM7 3 2 31.3
RTHERM8 2 Ambient 33.0

SABER Thermal Model

SABER thermal model FDN363N
Copper Area=0.02sq.in
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 = 1.8e-3
ctherm.ctherm2 8 7 = 2.1e-3
ctherm.ctherm3 7 6 = 4.0e-3
ctherm.ctherm4 6 5 = 4.4e-2
ctherm.ctherm5 5 4 = 5.3e-2
ctherm.ctherm6 4 3 = 5.6e-2
ctherm.ctherm7 3 2 = 6.7e-1
ctherm.ctherm8 2 tl = 3.0

rtherm.rtherm1 th 8 = 16.0
rtherm.rtherm2 8 7 = 20.5
rtherm.rtherm3 7 6 = 29.4
rtherm.rtherm4 6 5 = 29.5
rtherm.rtherm5 5 4 = 30.0
rtherm.rtherm6 4 3 = 31.0
rtherm.rtherm7 3 2 = 31.3
rtherm.rtherm8 2 tl = 33.0
}



TRADEMARKS

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ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E^2CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I^2C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.