FAN5063

ACPI Dual Switch Controller

Features

- Implements ACPI control with PWROK, $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$
- Switch and linear regulator controller for 3.3V Dual (PCI)
- Linear regulator controller and linear regulator for VADJ Dual output adjustable from 2.5V to 3.5V
- Break-before-Make
- Drives all N-Channel MOSFETs plus NPN
- Latched overcurrent protection for outputs
- Power-up softstarts for the linear regulators
- UVLO guarantees correct operation for all conditions
- 16 pin SOIC package

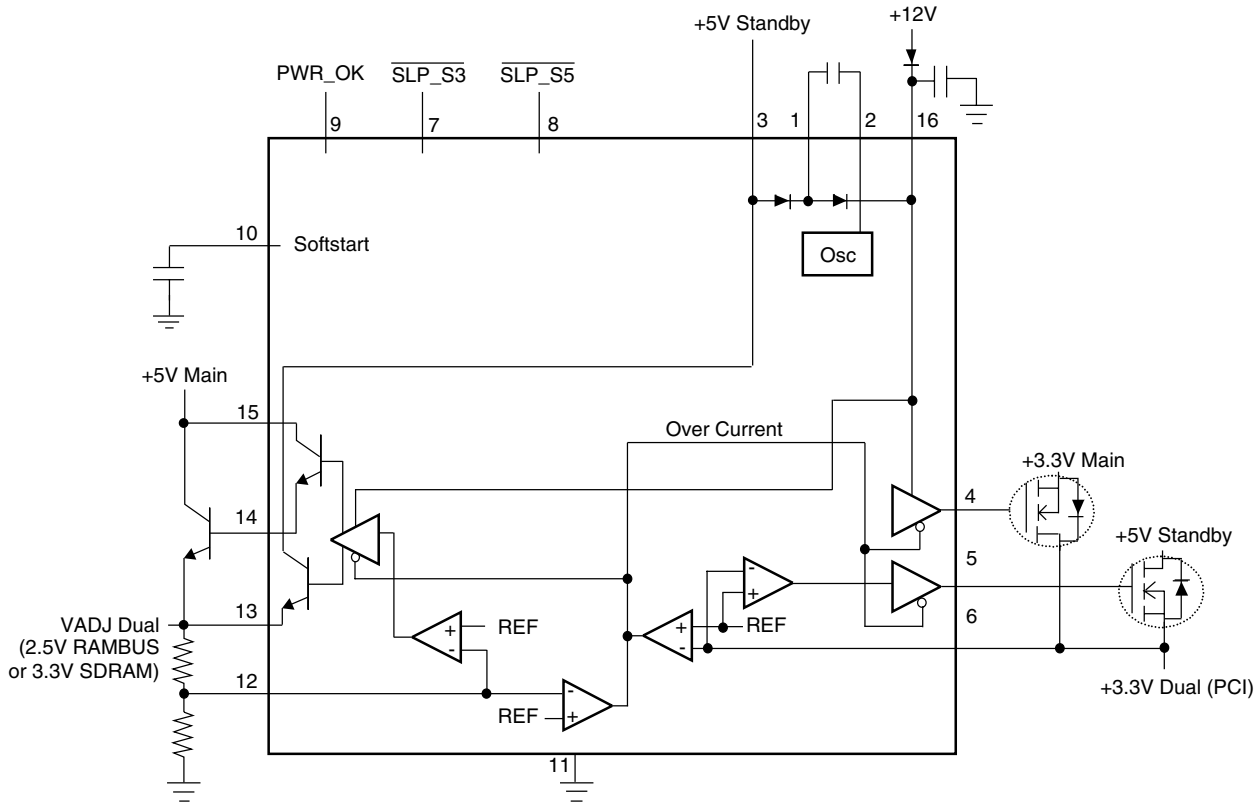
Description

The FAN5063 is an ACPI Switch Controller for the Camino, Whitney and Tehama Platforms. It is controlled by PWROK, $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$, and provides 3.3V Dual for PCI and VADJ Dual output for SDRAM or RAMBUS with 200mA minimum base current for an external NPN transistor. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The FAN5063 also offers integrated Current Limiting that protects each output, and softstart for the linear regulators. The FAN5063 is available in a 16 pin SOIC.

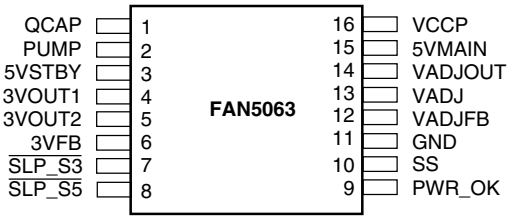
Applications

- Camino Platform ACPI Controller
- Whitney Platform ACPI Controller
- Tehama Platform ACPI Controller

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	QCAP	**Charge pump cap.** Attach flying capacitor between this pin and PUMP to generate high voltage from standby power.
2	PUMP	**Charge pump switcher.**
3	5VSTBY	**5V Standby.** Apply +5V standby on this pin to run the circuit in standby mode.
4	3VOUT1	**3.3V main gate control.** Attach this pin to a transistor powering 3.3V dual from the 3.3V main supply.
5	3VOUT2	**3.3V standby gate control.** Attach this pin to a transistor powering 3.3V dual from the 5V standby supply.
6	3VFB	**3.3V voltage Feedback.** Pin 6 is used as the input for the voltage feedback control loop for 3.3V dual.
7	$\overline{\text{SLP\_S3}}$	**$\overline{\text{SLP\_S3}}$.** Control signal governing the Soft Off state S3. Internal current source pulls this line high if left open.
8	$\overline{\text{SLP\_S5}}$	**$\overline{\text{SLP\_S5}}$.** Control signal governing the Soft Off state S5. Internal current source pulls this line high if left open.
9	PWR_OK	**PWR_OK.** Control signal for switches. Internal current source pulls this line high if left open.
10	SS	**Softstart.** Attach a capacitor to this pin to determine the softstart rate.
11	GND	**Ground.** Connect this pin to ground.
12	VADJFB	**Adjustable Dual Voltage Feedback.** Pin 12 is used as the input for the voltage feedback loop for the adjustable dual voltage.
13	VADJ	**Adjustable Dual Voltage**. Pin 13 sources VADJ during standby.
14	VADJOUT	**Adjustable Dual Voltage Base Control.** Attach this pin to an NPN transistor powering VADJ from the 5V Main.
15	5VMAIN	**5V Main.** Apply +5V Main on this pin to run the VADJ base drive.
16	VCCP	**Main Power.** Apply +12V through a diode on this pin to run the circuit in normal mode. Bypass with a 0.1µF capacitor. When 12V is not present, this pin produces voltage doubled 5V standby.

Absolute Maximum Ratings

V_{CCP}	15V
All Other Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction to Ambient Θ_{JA}	85°C/W
Thermal Resistance Junction-to-case, Θ_{JC}	24°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
+3.3VMAIN		3.135	3.3	3.465	V
+5VMAIN		4.75	5	5.25	V
+5VSTBY		4.75	5	5.25	V
+12V		11.4	12	12.6	V
Ambient Operating Temperature		0		70	°C

Electrical Specifications

($V_{+5VSTBY}$ = $V_{+5VMAIN}$ =5V, $V_{+3.3V}$ = 3.3V, V+12V = 12V and T_A = +25°C using circuit in Figure 4, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
+3.3V DUAL						
V_{Out1}, On		•	10			V
V_{Out1}, Off	I = 10µA	•			200	mV
V_{Out2}, On	Standby	•	5			mA
Total Output Voltage Variation[1]	3VOUT2 On	•	3.135	3.3	3.465	V
Maximum Drive Current	3VOUT1 On	•	100			mA
Minimum Load Current	3VOUT2 On	•			50	mA
Overcurrent Limit: Undervoltage				80		%Vout
Overcurrent Delay Time				150		µsec
Output Driver Deadtime	See Figure 2: Main → Standby	•	2		6	µsec
	: Standby → Main	•	200		1000	nsec
VADJ DUAL						
I_B	V_O > 3.3V	•	100			mA
	$V_O \leq$ 3.3V	•	150			mA
Total Voltage Variation[1]	$R_1 = R_2$ = 10KΩ	•	2.375	2.5	2.625	V
Vadj Output Voltage Range			1.25		3.5	V
Overcurrent Limit				80		%Vref
Overcurrent Delay Time				150		µsec
Output Driver Overlap Time	See Figure 2	•	1		5	µsec
Common Functions						
Charge Pump Frequency				250		KHz
+5VSTBY UVLO				4.5		V
+5VSTBY UVLO Hysteresis				0.5		V
+12V UVLO				7.5		V
+12V UVLO Hysteresis				800		mV
+5VSTBY Current	MAIN Power Present			10	25	mA
+12V Current				2.5	10	mA
Input Logic HIGH		•	2.0			V
Input Logic LOW		•			0.8	V
Softstart Current				6		µA
Control Line Input Current	$\overline{SLP\_S5}$, $\overline{SLP\_S3}$, PWROK	•			100	µA
Over Temperature Shutdown				150		°C

Note:
1. Voltage Regulation includes Initial Voltage Setpoint and Output Temperature Drift.

Table 1. Power Descriptors

PWROK	$\overline{SLP\_S3}$	$\overline{SLP\_S5}$	Main	3.3V Dual	VADJ	State	Usage
1	1	1	ON	ON, Powered from MAIN	ON, Powered from MAIN	S0	S0
1	0	1	OFF	ON, Powered from STANDBY	ON, Powered from STANDBY	S3	S0 → S3
0	0	1	OFF	ON, Powered from STANDBY	ON, Powered from STANDBY	S3	S3
0	1	1	OFF	ON, Powered from STANDBY	ON, Powered from STANDBY	S3	S3 → S0
1	0	0	OFF	ON, Powered from STANDBY	OFF	S5	S0 → S5
0	0	0	OFF	ON, Powered from STANDBY	OFF	S5	S5
0	1	0	OFF	ON, Powered from STANDBY	OFF	S5	S5 → S0
1	1	0	ON	ON, Powered from MAIN	OFF	S5	Not Used
0	0	0 → 1	OFF	ON, Powered from STANDBY	OFF	S5*	*

*When PWROK = $\overline{SLP\_S3}$ = 0 and $\overline{SLP\_S5}$ transitions from 0 to 1, the FAN5063 remains in the S5 state. See Table 2.

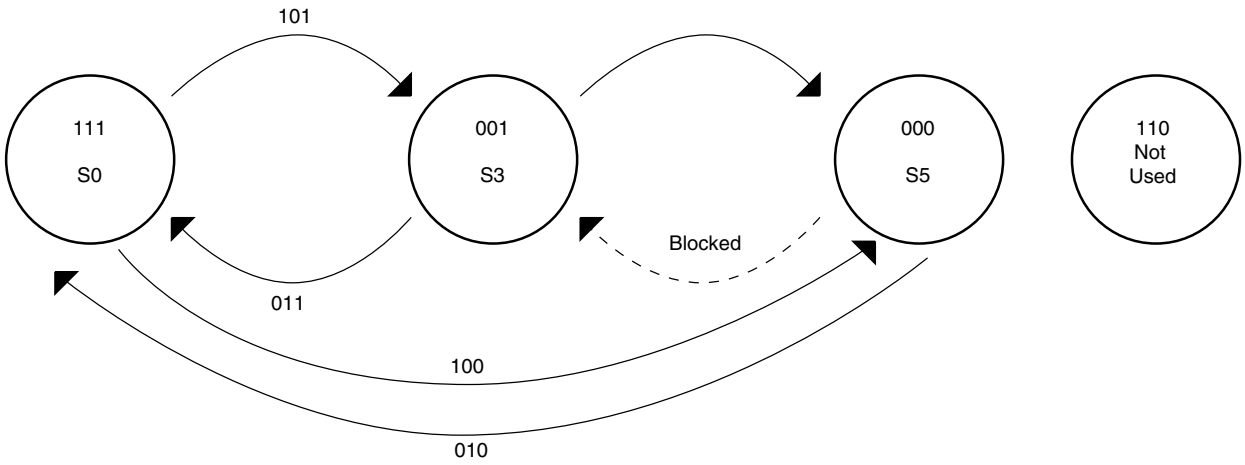


Figure 1. Power State Usage Diagram

Table 2. State Transition Table

Initial Control Signal	Initial Control Signal: 000	001	010	011	100	101	110	111
000	—	x	-	x	—	x	—	S0
001	S5	—	S5	-	S5	—	S5	S0
010	—	x	-	x	—	x	—	S0
011	S5	—	S5	—	S5	—	S5	S0
100	—	x	—	x	—	x	—	S0
101	S5	—	S5	—	S5	—	S5	S0
110	—	x	—	x	—	x	—	S0
111	S5	S3	S5	S3	S5	S3	S5	—

Notes:
1. Control Signal order: PWROK, $\overline{\text{SLP\_S3}}$, $\overline{\text{SLP\_S5}}$.
2. Dash (—) signifies that no state change takes place.
3. X signifies that the state transition is blocked, and the FAN5063 remains in the S5 state.

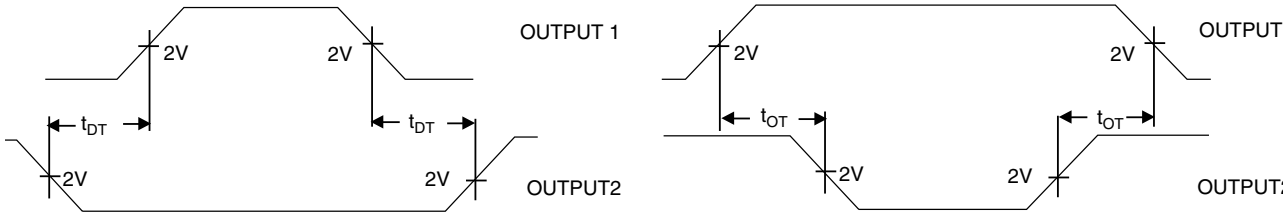


Figure 2. Deadtime and Overlap Time Measurements

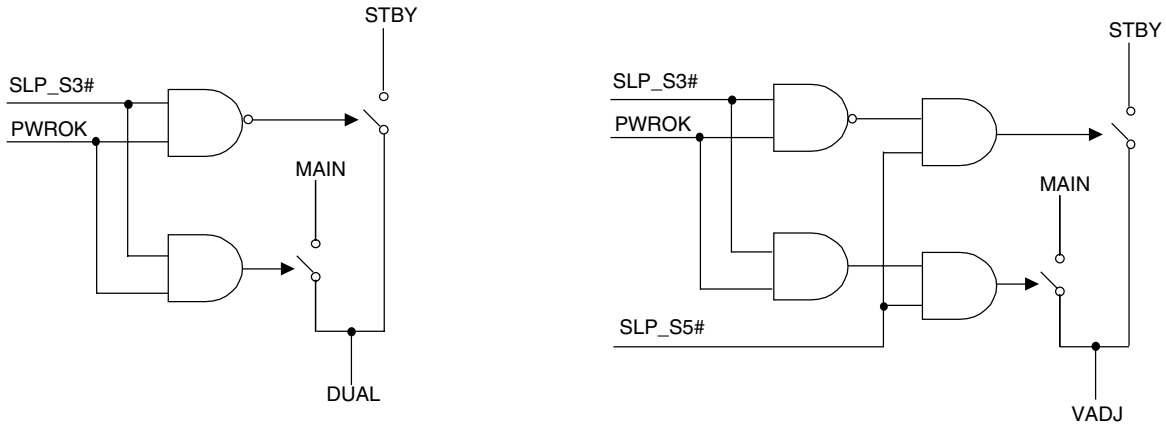


Figure 3. Control Logic for Dual Voltages and Memory Voltages

Application Circuits

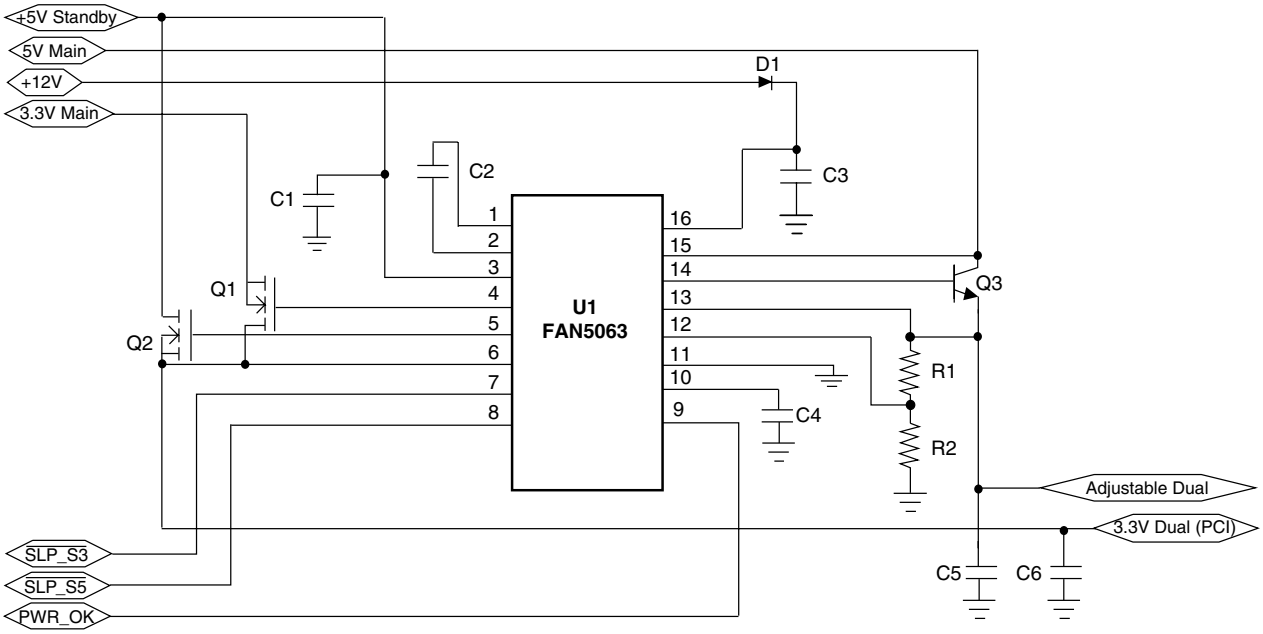


Figure 4. ACPI Selector

Table 3. FAN5063 Application Bill of Materials

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1-4	Various	4	100nF, 25V	Ceramic
C5–6	Various	2	220µF, 6V	Tantalum, ESR ~ 0.1Ω
R1	Various	1	*	*10KΩ for 2.5V, 16.5KΩ for 3.3V
R2	Various	1	10KΩ Resistor	
D1	Fairchild MBR0520L	1	20V, 1/2A Schottky	
Q1	Fairchild FDS4410DY	1	N-channel MOSFET	$R_{ds,on}$ = 20mΩ @ V_{gs} = 4.5V
Q2	Fairchild NDS9956A	1	N-channel MOSFET	$R_{ds,on}$ = 110mΩ @ V_{gs} = 4.5V
Q3	Fairchild TIP41A	1	NPN	V_{CE} ~0.4V @ I_C = 2A, I_B = 100mA
U1	Fairchild FAN5063	1	ACPI Dual Switch Controller	

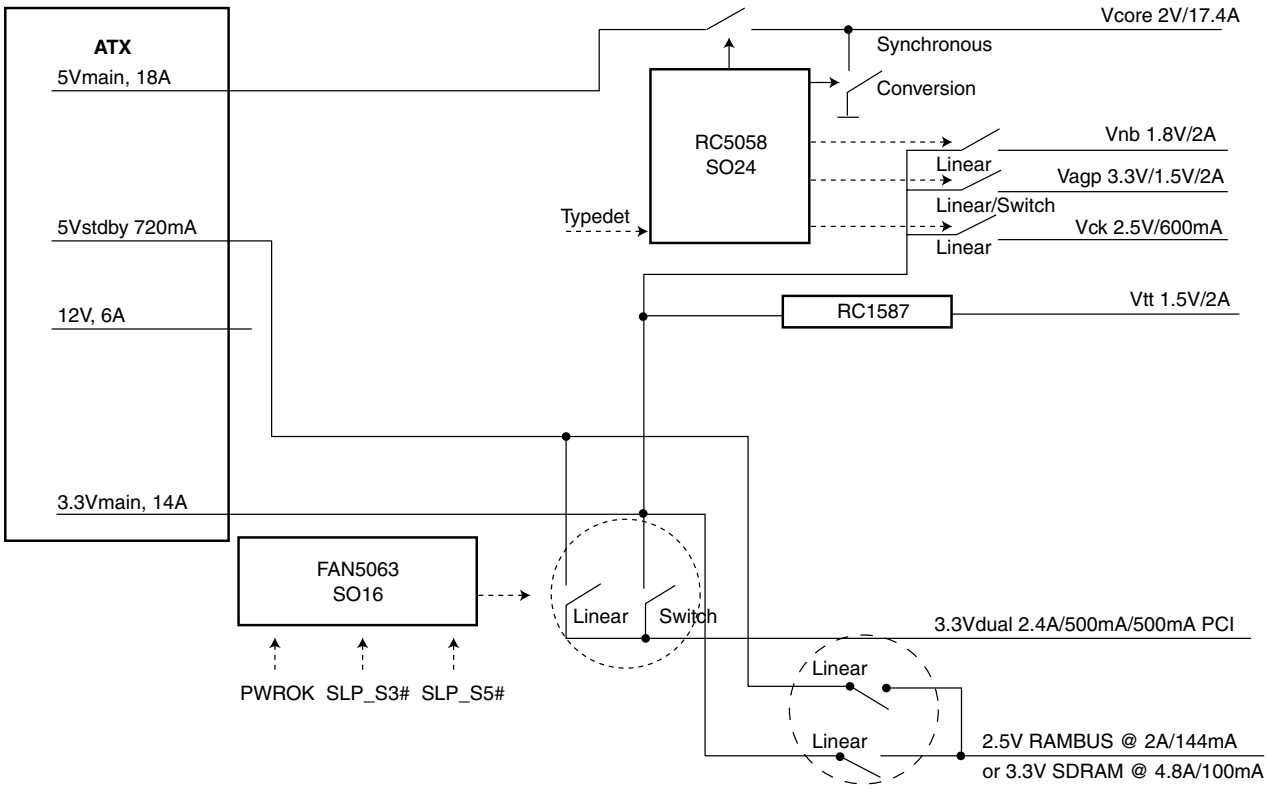


Figure 5. Camino System Architectural Block Diagram (Power Paths Only)

Application Information

The FAN5063 Controller

The FAN5063 is a fully compliant ACPI controller IC. Used with an ATX power supply, it generates a 3.3V Dual for PCI, and power for either SDRAM and RAMBUS, and has a large array of additional protection functions integrated in. Used in conjunction with Fairchild's RC5058, it provides control and power functions necessary to implement a Camino or Whitney motherboard. It can also be used to generate the dual voltages necessary for a Tehama motherboard.

Overview of ACPI

The Advanced Configuration and Power Interface, or ACPI, is a system for controlling the use of power in a computer. It enables the computer manufacturer and the computer user to determine the computer's power usage dynamically. For example, when the computer has been unused for a certain time, the monitor and peripherals could be turned off, and their states saved to memory. After a longer period, the processor could be turned off, and the memory saved to disk. A peripheral could then re-awaken the entire system on the occurrence of an event, such as the arrival of a FAX on a modem.

As shown in Figure 5, the available power inputs to the computer system from the ATX power supply are +5V main, +12V main, +3.3V main, and +5V standby. "Main" means that these power outputs are available under full-power operation of the system, but can be turned off in some of the power-saving modes. "Standby" means that this power output is always present.

The most general ACPI system requires four dual outputs: 5V dual, 3.3V dual, 3.3V SDRAM, and 2.5V RAMBUS (or 2.5V dual). "Dual" means that the power can be (but is not necessarily) present whether the main power supplies are present or not. To ensure the presence of these outputs, while not overloading the standby power, they have dual inputs, from both main power and standby. The presence or absence of the dual outputs is determined by the control signals to the FAN5063.

ACPI States

As shown in Table 1, there are three ACPI states that are of primary concern to the system designer, designated S0, S3 and S5. S0 is the full-power state, the state of the computer when it is being actively used. The other two states are sleep states, reflecting differing levels of power-down.

S3 is a state in which the processor is powered down, but its last state is being preserved in IC memory, which is kept on. Since memory is fast, the computer can quickly come back up to full operation. However, this state continues to draw moderate power, due to the memory being kept alive.

S5 is a state in which memory is off, and the last state of the processor has been written to the hard disk. Since the disk is slow, the computer takes longer to come back to full operation. However, since memory is off, this state draws minimal power.

It is anticipated that only the following state transitions will occur: S0 → S3, S0 → S5, S3 → S5, S5 → S0, and S3 → S0; the transition S5 → S3 will occur only as an intermediate state during the transition from S5 → S0. To prevent overcurrent limit from activating, the FAN5063 blocks this transition. For example, when PWROK = $\overline{SLP\_S3}$ = 0, and $\overline{SLP\_S5}$ transitions from 0 to 1, the FAN5063 remains in the S5 state. See Table 2.

3.3V Dual Output

The 3.3V dual output is intended to power subsystems such as the computer's PCI slots. A typical application that would require the use of 3.3V dual rather than +3.3V main for a PCI slot would be the use of a modem: if the system needs to be able to awaken from sleep when the modem receives incoming data, then that slot must be powered from dual, because main power is off. Other slots not requiring dual power can be configured using the control signals.

3.3V dual is generated by two MOSFETs, one from +3.3V main, the other from +5V standby, as shown in Figure 4. When main power is present, the MOSFET Q1 is turned on as a switch, so that input and output are connected together. When main power is absent, the MOSFET Q2 is controlled by the FAN5063 as a linear regulator, generating a regulated 3.3V from +5V standby. The MOSFET Q1 must be connected as shown in the figures, to avoid back-feed.

The state of the MOSFETs is controlled by the $\overline{SLP\_S3}$ and PWROK lines, as shown in Figure 3. When both $\overline{SLP\_S3}$ and PWROK are asserted, the main switch is on, and the linear regulator is off. If either line is de-asserted, the main switch is off and the linear regulator is on.

Q1 and Q2 as shown in Table 3 have different $R_{DS,on}$ ratings. In a typical system, it is anticipated that full-power current will be about 2.4A maximum, and standby current will be about 500mA maximum. The difference in maximum currents means that Q2 can be a less expensive device than Q1.

The design of the linear regulator for the 3.3V Dual necessitates a minimum load current of 50mA. Furthermore, in order to guarantee stable operation, the output capacitor on the 3.3V Dual must have a minimum ESR as shown in Figure 6. The hatched region shows acceptable values of ESR vs. output capacitance. Values of the output capacitor less than 47μF or greater than 300μF are not recommended.

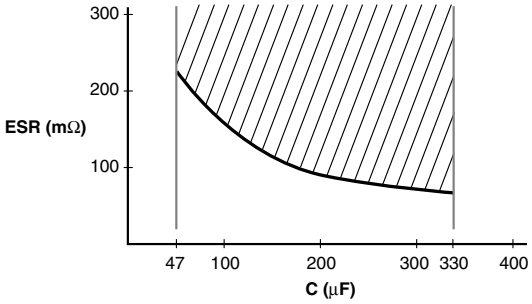


Figure 6. Recommended C vs. ESR for Stable Operation of the 3.3V Dual

Adjustable Dual Output

The adjustable dual output is intended to provide power to RAMBUS or SDRAM memory.

Adjustable dual is generated by one external NPN bipolar acting as a linear regulator from +5V main, and one linear regulator internal to the FAN5063 from +5V standby, as shown in Figure 4, and in the block diagram on the front page. When main power is present, the NPN Q3 linear regulates, and when main power is absent, the internal linear regulator is on. Q3 cannot be substituted with a MOSFET. If used in one direction, the MOSFET's body diode would permit back-feed; if used in the other direction, it would short-circuit the linear regulator action.

The state of the external MOSFET and the internal linear regulator is controlled by the $\overline{\text{SLP\_S3}}$ and PWROK lines, and additionally the $\overline{\text{SLP\_S5}}$ line, as shown in Figure 3. When $\overline{\text{SLP\_S5}}$ is de-asserted, both the external MOSFET and the internal linear regulator are off, and there is no output voltage on the 3.3V SDRAM line.

If the $\overline{\text{SLP\_S5}}$ line is asserted, the adjustable dual output is on. In this condition, if either the $\overline{\text{SLP\_S3}}$ or the PWROK line, or both, are de-asserted, the linear regulator is on and the MOSFET is off. Only in the case if both the $\overline{\text{SLP\_S3}}$ and the PWROK lines are asserted, the MOSFET is on and the linear regulator is off.

In a typical system, it is anticipated that standby current will be a maximum of 144mA, and full-power current may be as high as 2A. This places some significant constraints on the selection of Q3. Since its input may be as low as (5V – 5%) = 4.75V, there is only 4.75V – 3.3V = 1.45mV of V_{CE} headroom for its operation as a linear regulator. For this reason the FAN5063 can provide up to 200mA of steady-state base current. The TIP41A device shown has a sufficiently low $V_{CE,sat}$ to guarantee worst-case regulation even at 2A I_E with this base current.

The output voltage of the Adjustable Dual is set with two resistors as shown in Figure 4, according to the equation.

$$Vadj = 1.25V \bullet \frac{R_1 + R_2}{R_2}$$

FAN5063 ACPI Control Lines

As already discussed, the FAN5063 outputs are controlled by the three ACPI control lines, $\overline{\text{SLP\_S3}}$, $\overline{\text{SLP\_S5}}$ and PWROK, as summarized in Tables 1 and 2. System designers must in particular be careful to ensure that their system is designed with $\overline{\text{SLP\_S5}}$, not $\overline{\text{SLP\_S5}}$; if $\overline{\text{SLP\_S5}}$ is used, it must be inverted before being used with the FAN5063.

The control lines have internal pull-ups of approximately 40μA, and so can be controlled by open collector drivers if desired. In a noisy system, it may be desirable to filter these lines, which can be done with a 1KΩ resistor and a small capacitor.

FAN5063 Dynamic Operation

The FAN5063 is designed to minimize the output capacitance required to hold up the various output lines during transitions between different states. Thus in particular, the adjustable dual output has guaranteed minimum overlap time, the time (as shown in Figure 2) during a state transition during which both main and standby are connected to the output. This overlap time guarantees that a power source is always connected to the output, so that there will be no dip in the output voltage during state transitions. There is also a maximum overlap time, to ensure that the standby power doesn't have to source main power very long, thus minimizing thermal stress on the standby device.

The 3.3V dual is different because it is powered by both a linear regulator and a switch. If the linear regulator were to turn on while the switch is on (or vice versa) the linear regulator would supply power to the main line through the switch. For this reason, the linear regulator must be off before the switch is on, and vice versa. Thus, this output has guaranteed minimum deadtime when both linear regulator and switch are off. During this time, the output capacitor must hold up the load, and so there is also a specified maximum deadtime, allowing a maximum necessary capacitance to be selected, see below.

Stability

As with all linear regulators, the FAN5063's linear regulators require a minimum load. With the exception of the 3.3V dual output, however, all of these minimum loads are internal to the FAN5063. The 3.3V dual output requires a minimum load of 50mA; if a situation may occur in which the load is less than 50mA, additional steps may be necessary to ensure stability.

Furthermore, depending on location, it may be necessary to bypass the drain (or collector) of the linear regulator with a low ESR capacitor for stability. As a rule of thumb, if the pass element is more than 1" from its power source, it should have a bypass.

Softstart

Pin 10 of the FAN5063 functions as a softstart. When power is first applied to the chip, a constant current is applied from the pin into an external capacitor, linearly ramping up the voltage. This ramp in turn controls the internal reference of the FAN5063. providing a softstart for the linear regulators. The actual state of the FAN5063 on power up will be determined by the state of its control lines.

The switches in the system must be either on or off, and so softstart has no effect on their characteristics: if the appropriate control signals are asserted, they will turn on at once.

The softstart is effective only during power on. During a transition between states, such as from S5 → S0, the linear regulators are not softstarted.

It is important to note that the softstart pin is not an enable; pulling it low will not necessarily turn off all outputs.

Charge Pump

In main power operation, the FAN5063 is run from the +12V main supply. This supply also provides voltage to the various MOSFET gates. However, during standby, this supply is off. To provide power to the chip and the appropriate gates, the FAN5063 incorporates a free-running charge pump. As shown in Figure 4, and in the block diagram on the front page, a capacitor attached between pins 1 and 2 of the FAN5063 acts as a charge pump with internal diodes. The charge pump output is internally diode or'red with the 12V input. The 12V input must have a series diode to prevent back-feeding the charge pump to the + 12V main when in standby. The 12V input line needs a bypass capacitor for high-frequency noise rejection.

Overcurrent

The FAN5063 does not directly detect current through the devices that power its outputs. Instead, it monitors the output voltages. In the event of a hard short, the voltage drops below 80% of nominal, and all outputs are latched off, and remain off until 5V standby power is recycled. The overcurrent latch off is delayed by 150μsec to prevent nuisance trips.

During softstart, the overcurrent voltage monitors are kept proportional to the reference, to avoid tripping overcurrent during startup.

In the S5 state, when the memory outputs are off, the voltage monitors on the memory lines are disabled, to prevent tripping the overcurrent. When turning these lines back on from the S5 state, overcurrent is prevented from tripping because the S3 state is blocked. See Table 2.

If the adjustable dual is not used, its feedback line, pin 12, must be connected to 5V STBY, to prevent an overcurrent trip.

UVLO

If the +5V standby is below approximately 4.5V, the FAN5063 will leave off or turn off all outputs. Similar comments apply to the +12V main at 7.5V. The +5V standby UVLO has approximately 0.5V hysteresis, the +12V main UVLO 1V.

Over Temperature

The FAN5063 is capable of sourcing substantial current, 200mA minimum to the adjustable voltage transistor's base during S0 and 144mA to the line during S3. As a result, there can be heavy power dissipation in the IC. While the FAN5063 is designed to accept this power dissipation, any overloading of outputs can cause excessive heating. If the FAN5063 die temperature exceeds about 150°, all outputs are shut off. Outputs remain off until the die temperature returns to its safe area.

Transistor Selection

External transistor selection depends on usage, differing for the linear regulators and the switches.

The MOSFET switches, should be sized based on regulation requirements and power dissipation. Since the ATX outputs are ±5%, the outputs driven from them must be wider. As an example, if we want to hold 3.3V PCI to -10%, we can drop only 5% = 165mV across Q1. At 2.4A, this means Ql must have a maximum $R_{DS,on}$ of 165mV/2.7A = 68mΩ, including tolerance and self-heating effects. We thus choose a Fairchild FDC633N, which has 72mΩ maximum $R_{DS,\,on}$ at 4.5V V_{GS} at 25°C. We can estimate power dissipation as $(2.4A)^2$ * 42mΩ = 270mW, which should be acceptable for this package.

Q2 is a MOSFET functioning as a linear regulator. Since it delivers only 500mA, it is easy to select a MOSFET, it need only be able to handle 500mA * (5V + 5% – 3.3V) = 1W. We select the Fairchild FDS6630A in an SO-8 package.

Q3 is an NPN bipolar functioning as a linear regulator. As already discussed, it must have a $V_{CE,sat}$ lower than 1.45V at I_E = 2A and I_B = 200mA. Its power dissipation can be as high as (5V + 5%–3.3V) * 2A = 3.9W.

Alternate for Adjustable Dual

Instead of the bipolar transistor shown in Figure 4 for Q3, the linear pass element for the adjustable dual, a MOSFET and schottky diode can be used as shown in Figure 7.

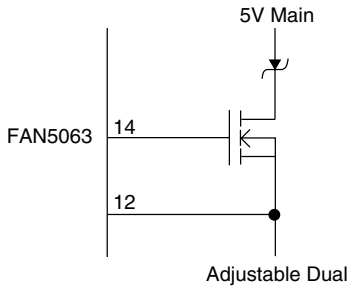


Figure 7. Adjustable Dual with MOSFET

The schottky should be chosen to have a low V_f at the specified adjustable voltage and current. The MOSFET's $R_{DS,on}$ must then be lower than (5V -5% -VADJ -V_f)/I_{Dual} including temperature. An additional constraint is that the MOSFET must have a gate threshold voltage lower than 1.5V. For example, for 2.8A @3.3V, choose the diode to be an MBR835, and the MOSFET a Fairchild FDC653M. This same technique can then also be used for adjustable currents higher than can be achieved with the bipolar transistor.

Output Capacitor Selection

Output capacitor selection depends on whether the line has overlap time or not.

For both the adjustable dual, there is guaranteed overlap time between when one source is turned on and the other source turned off. For this output, the output capacitor is not needed to hold up the supply, but only for noise filtering and to respond to transient loading.

The 3.3V dual output has deadtime between when one source is turned off and the other source turned on. During the time when both are off, the output current must be supplied by the output capacitor. Mitigating this, it must be realized that the system will be designed in such a way that the current has gone to its sleep value before the transition occurs. For example, the 3.3V dual has a sleep current of 500mA maximum. Maximum deadtime is 6μsec, and so charge depletion is 500mA * 6μsec = 3μC. Suppose that we have a total of 8% drop due to the source tolerance and the MOSFET drop, and we are trying to hold 10% regulation. The remaining 2% = 66mV implies a minimum capacitance of 3μC/66mV = 45μF.

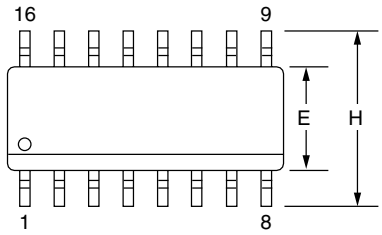
Mechanical Dimensions

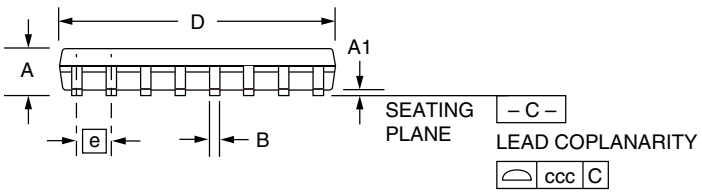
16 Lead SOIC

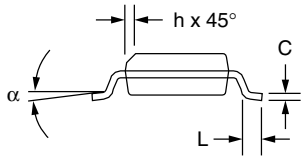
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
FAN5063M	16 pin SOIC

FAN5063
ACPI Dual Switch Controller

Contents

Datasheet

Download this datasheet

PDF

e-mail this datasheet

[E-

This pagePrint version

Related Links

Request samples
How to order products
Product Change Notices (PCNs)
Support
Distributor and field sales representatives
Quality and reliability
Design tools

General description

The FAN5063 is an ACPI Switch Controller for the Camino, Whitney and Tehama Platforms.It is controlled by PWROK, /SLP_S3 and /SLP_S5,and provides 3.3V Dual for PCI and VADJ Dual output for SDRAM or RAMBUS with 200mA minimum base current for an external NPN transistor.An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components.The FAN5063 also offers integrated Current Limiting that protects each output,and softstart for the linear regulators.The FAN5063 is available in a 16 pin SOIC.

back to top

Features

- Implements ACPI control with PWROK, /SLP_S3 and /SLP_S5
- Switch and linear regulator controller for 3.3V Dual (PCI)
- Linear regulator controller and linear regulator for VADJ Dual output adjustable from 2.5V to 3.5V
- Break-before-Make
- Drives all N-Channel MOSFETs plus NPN
- Latched overcurrent protection for outputs
- Power-up softstarts for the linear regulators

- UVLO guarantees correct operation for all conditions
- 16 pin SOIC package

back to top

Applications

- Camino Platform ACPI Controller
- Whitney Platform ACPI Controller
- Tehama Platform ACPI Controller

back to top

Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Package marking	Packing method
FAN5063M	Full Production	$1.23	SOIC	16	$Y&Z&2&T FAN5063M A	RAIL
FAN5063MX	Full Production	$1.23	SOIC	16	$Y&Z&2&T FAN5063M A	TAPE REEL

* 1,000 piece Budgetary Pricing

back to top

Application notes

AB-26: AB-26 Using Other Voltages with the FAN5063 (38 K) Jul 19, 2002

back to top