Automotive Grade Non-Synchronous Buck Controller

NCV8852

SOIC−8
SUFFIX D
CASE 751

The NCV8852 is an adjustable−output non−synchronous buck controller which drives an external P−channel MOSFET. The device uses peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the gate driver.

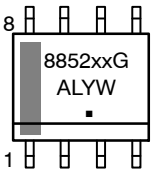
Protection features include internal soft−start, undervoltage lockout, cycle−by−cycle current limit, hiccup−mode overcurrent protection, hiccup−mode short−circuit protection.

Additional features include: programmable switching frequency, low quiescent current sleep mode and externally synchronizable switching frequency.

Features

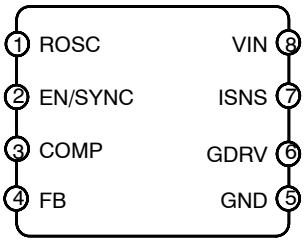
- Ultra Low Iq Sleep Mode
- Adjustable Output with 800 mV ±2.0% Reference Voltage
- Wide Input of 3.1 to 44 V with Undervoltage Lockout (UVLO)
- Programmable Switching Frequency
- Internal Soft−Start (SS)
- Fixed−Frequency Peak Current Mode Control
- Internal Slope Compensating Artificial Ramp
- Internal High−Side PMOS Gate Driver
- Regulated Gate Driver Current Source
- External Frequency Synchronization (SYNC)
- Programmable Cycle−by−Cycle Current Limit (CL)
- Hiccup Overcurrent Protection (OCP)
- Output Short Circuit Hiccup Protection (SCP)
- Space−Saving 8−PIN SOIC Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAM



8852xxG = Specific Device Code
xx = 01
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCV885201D1R2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

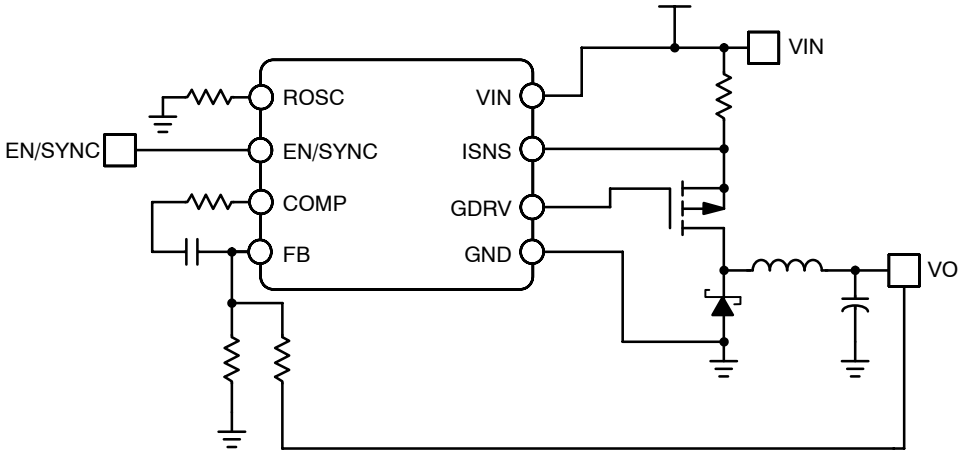


Figure 1. NCV8852 Application Diagram

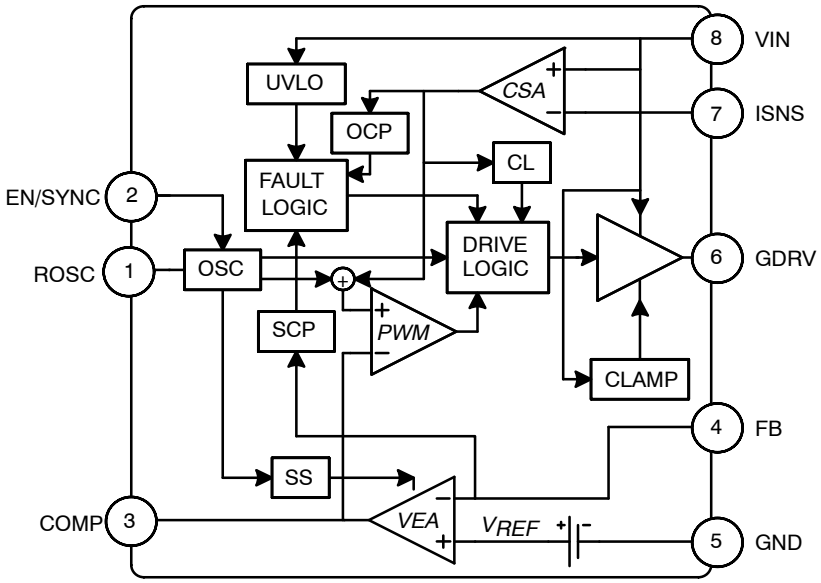


Figure 2. NCV8852 Simple Block Diagram

PIN DESCRIPTIONS

No	Pin Symbol	Function
1	ROSC	Use a resistor from ground to set the frequency.
2	EN/SYNC	Enable and synchronization input. The falling edge synchronizes the internal oscillator. The part is disabled into sleep mode when this pin is brought low for longer than the enable time−out period.
3	COMP	Output of the voltage error amplifier. An external compensator network from COMP to GND is used to stabilize the converter and tailor transient performance.
4	FB	Output voltage feedback. A resistor from the output voltage to FB with another resistor from FB to GND creates a voltage divider for regulation and programming of the output voltage.
5	GND	Ground reference.
6	GDRV	Gate driver output. Connect to gate of the external P−channel MOSFET. A series resistance can be added from GDRV to the gate to tailor EMC performance.
7	ISNS	Current sense input. Connect this pin to the source of the external P−channel MOSFET, through a current−sense resistor to VIN to sense the switching current for regulation and current limiting.
8	VIN	Main power input for the IC.

MAXIMUM RATINGS (Voltages are with respect to GND unless otherwise indicated.)

Rating	Value	Unit
DC Voltage (VIN, ISNS, GDRV)	−0.3 to 44	V
Peak Transient Voltage (Load Dump on VIN)	44	V
DC Voltage (EN/SYNC)	−0.3 to 6.0	V
DC Voltage (COMP, FB, ROSC)	−0.3 to 3.6	V
DC Voltage Stress (VIN − GDRV)	−0.7 to 12	V
Operating Junction Temperature Range	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free 60 to 150 seconds at 217°C	265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PACKAGE ATTRIBUTES

Characteristic	Value
ESD Capability Human Body Model Machine Model Charge Device Model	 2.0 kV 200 V >1.0 kV
Moisture Sensitivity Level	MSL 1 260°C
Package Thermal Resistance Junction−to−Ambient, $R_{\theta JA}$	 100°C/W

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.4 V to 36 V, EN = 5 V. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0 V, Sleep Mode		2.5	6.0	μA
	$I_{q,off}$	V_{IN} = 13.2 V, EN = 5 V or toggled, V_{FB} = 1 V, No Switching		2.0	3.0	mA
	$I_{q,on}$	V_{IN} = 13.2 V, EN = 5 V or toggled, V_{FB} = 0 V, Switching		3.0	5.0	mA
Undervoltage Lockout	V_{uvlo}	V_{IN} decreasing	2.9	3.1	3.3	V
Undervoltage Lockout Hysteresis	$V_{uvlo,hys}$		50	150	300	mV
Overvoltage Lockout	V_{ovlo}		36.9	38	39.3	V
OSCILLATOR						
Switching Frequency	f_{SW}		100		500	kHz
R_{OSC} Voltage	V_{ROSC}			1.0		V
Default Switching	f_{SW}	R_{OSC} = Open R_{OSC} = 100 kΩ R_{OSC} = 20 kΩ R_{OSC} = 10 kΩ	153 180 283 409	170 200 315 455	187 220 347 501	kHz
Slope Compensation	m_a			25.5		mV/μs
Minimum On Time	t_{onmin}		90	110	140	ns
Max Duty Cycle − Switching	$D_{max,sw}$	Maximum duty cycle when switching		93		%
Max Duty Cycle	D_{max}			100		%
Soft−Start Time	t_{ss}		1.0	1.5	2.0	ms
Soft−Start Delay	$t_{ss,dlly}$		200	300	400	μs
EN/SYNC						
Low Threshold	$V_{s,il}$				0.8	V
High Threshold	$V_{s,ih}$		2.0			V
Input Current	I_{sync}			5.0	10	μA
SYNC Frequency Range	f_{sync}	Relative to Nominal Switching Frequency	80		600	%
SYNC Delay	$t_{s,dly}$	From SYNC falling edge to GDRV falling edge		50	100	ns
SYNC Duty Cycle	D_{sync}		25		75	%
Disable Delay Time	t_{en}	% of f_{SW}		300		%
VOLTAGE ERROR AMP						
DC Gain	A_v		55	80	91	dB
Gain−Bandwidth Product	G_{BW}		1.7	2.4	3.1	MHz
FB Bias Current	$I_{vfb,bias}$			0.1	1.0	μA
Charge Currents	$I_{src,vea}$	Source, V_{FB} = 0.9 V, V_{COMP} = 1.2 V	1.2	1.8	2.5	mA
	$I_{snk,vea}$	Sink, V_{FB} = 0.7 V, V_{COMP} = 1.2 V	0.5	0.8	1.0	
Reference Voltage	V_{ref}		784	800	816	mV
High Saturation Voltage	$V_{c,max}$		2.2	2.3		V
Low Saturation Voltage	$V_{c,min}$			0.001	0.3	V
CURRENT SENSE AMP						
Common−Mode Range	CMR		3.1		40	V
Differential Mode Range	DMR		300			mV
Amplifier Gain	A_{csa}			2.0		V/V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.4 V to 36 V, EN = 5 V. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT SENSE AMP						
Input Bias Current	$I_{sns,bias}$	NCV885201		70	120	μA
CURRENT LIMIT / OVER CURRENT PROTECTION						
Cycle−by−Cycle Current Limit Threshold	V_{cl}		85	100	115	mV
Cycle−by−Cycle Current Limit Response Time	t_{cl}				200	nsec
Over Current Protection Threshold	V_{ocp}	% of V_{cl}	125	150	175	%
Over Current Protection Response Time	t_{ocp}				200	ns
GATE DRIVERS						
Leading Edge Blanking Time	$t_{on,min}$				100	ns
Gate Driver Pull Up Current	I_{sink}	V_{IN} − V_{GDRV} = 4 V	160	230	300	mA
Gate Driver Pull Down Current	I_{src}	V_{IN} − V_{GDRV} = 4 V	160	230	300	mA
Gate Driver Clamp Voltage (V_{IN} − V_{GDRV})	V_{drv}		6.0	8.0	10	V
Power Switch Gate to Source Voltage	V_{gs}	V_{IN} = 4 V	3.8			V
SHORT CIRCUIT PROTECTION						
Startup Blanking Time	$t_{scp,dly}$	From start of soft−start, % of soft−start time	105		300	%
Short−Circuit Threshold Voltage	V_{scp}	% of Feedback Voltage (V_{ref})	65	70	75	%
Hiccup Time	$t_{hcp,dly}$	% of Soft−Start Time		135		%
SC Response Time	t_{scp}	Switcher Running		60	200	ns
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{sd}	T_J rising	160	170	180	°C
Thermal Shutdown Hysteresis	$T_{sd,hys}$	T_J Shutdown − T_J Startup	10	15	20	°C
Thermal Shutdown Delay	t_{tsd}	T_J > Thermal Shutdown Threshold to stop switching			200	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS CURVES

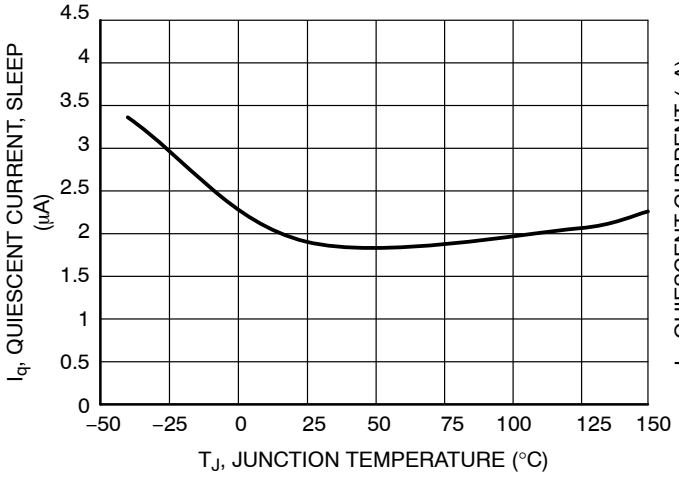


Figure 3. Quiescent Current (Sleep) vs. Junction Temperature

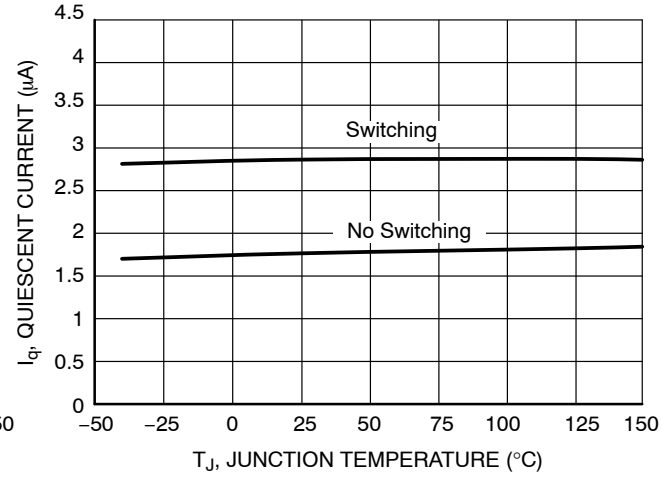


Figure 4. Quiescent Current vs. Junction Temperature

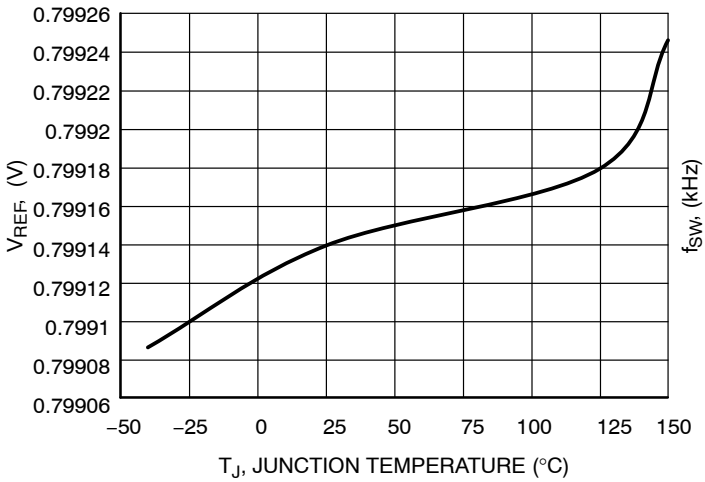


Figure 5. Reference Voltage vs. Junction Temperature

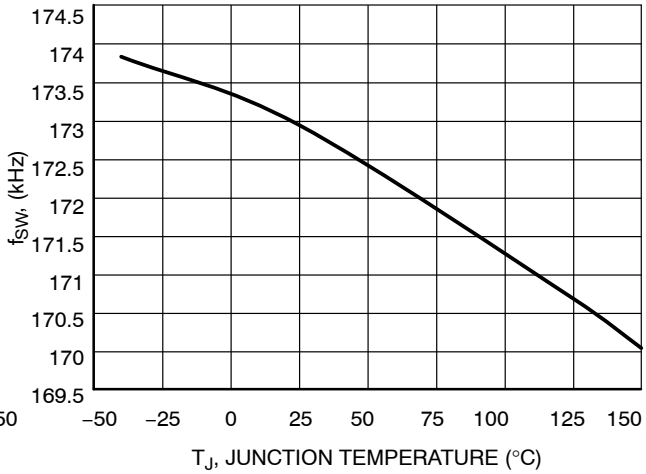


Figure 6. Switching Frequency (R_{OSC} = open) vs. Junction Temperature

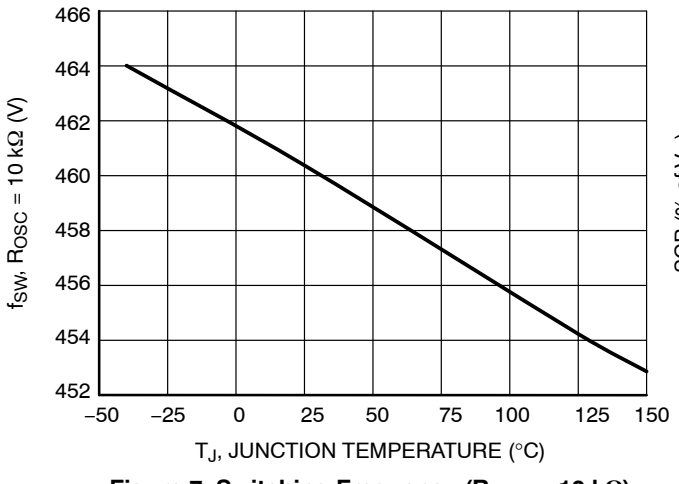


Figure 7. Switching Frequency (R_{OSC} = 10 kΩ) vs. Junction Temperature

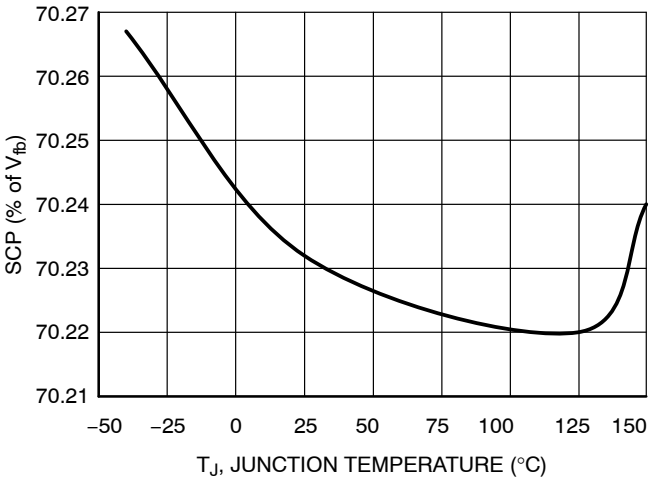


Figure 8. Short−Circuit Protection Threshold vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES

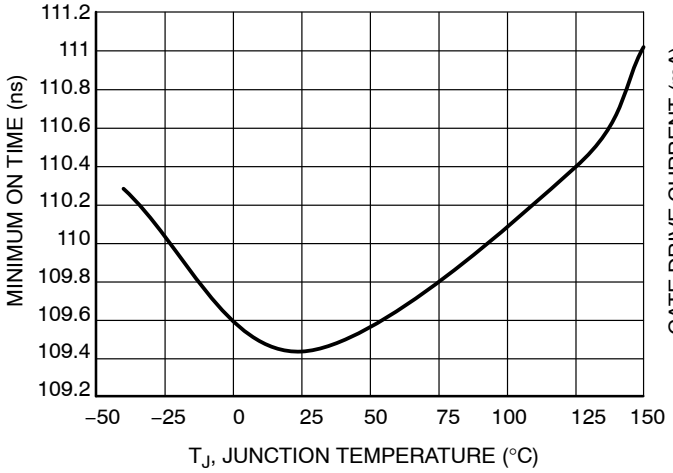


Figure 9. Minimum On Time vs. Junction Temperature

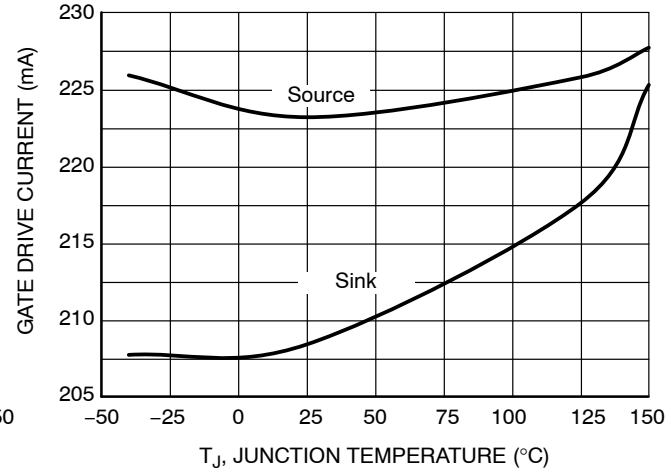


Figure 10. Gate Drive Current vs. Junction Temperature

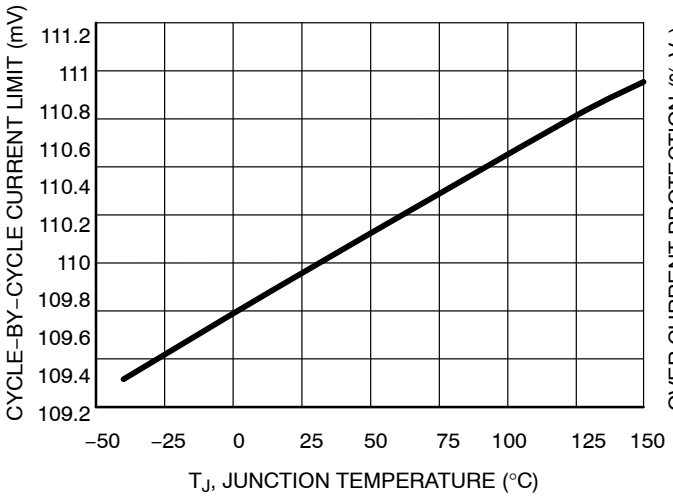


Figure 11. Cycle−by−Cycle Limit vs. Junction Temperature

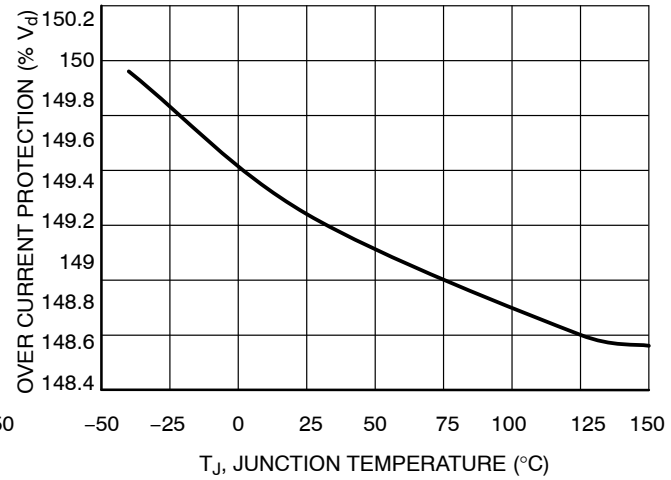


Figure 12. Over Current Protection vs. Junction Temperature

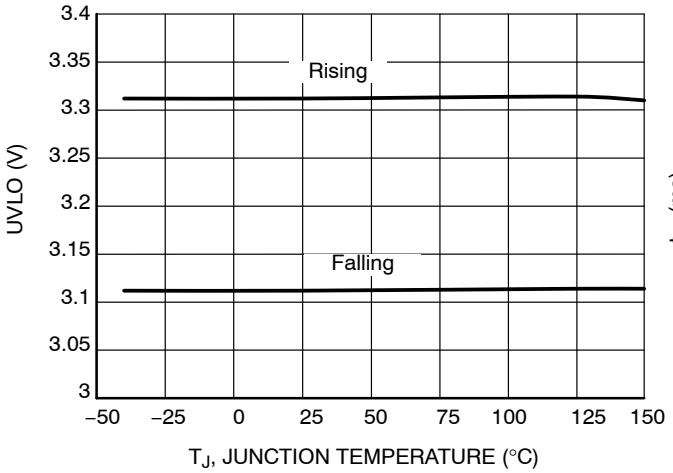


Figure 13. UVLO Threshold vs. Junction Temperature

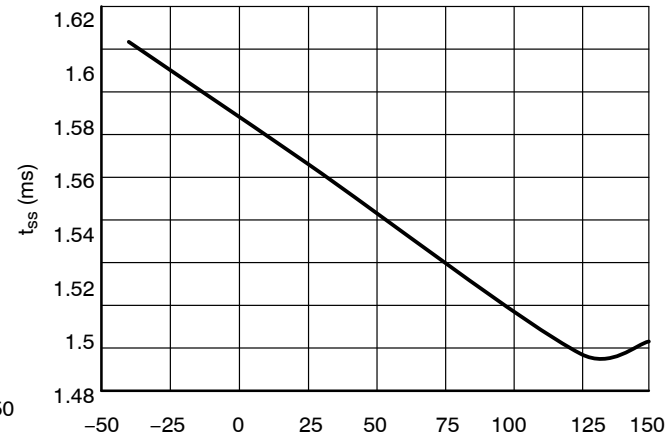


Figure 14. Soft−Start Time vs. Junction Temperature

THEORY OF OPERATION

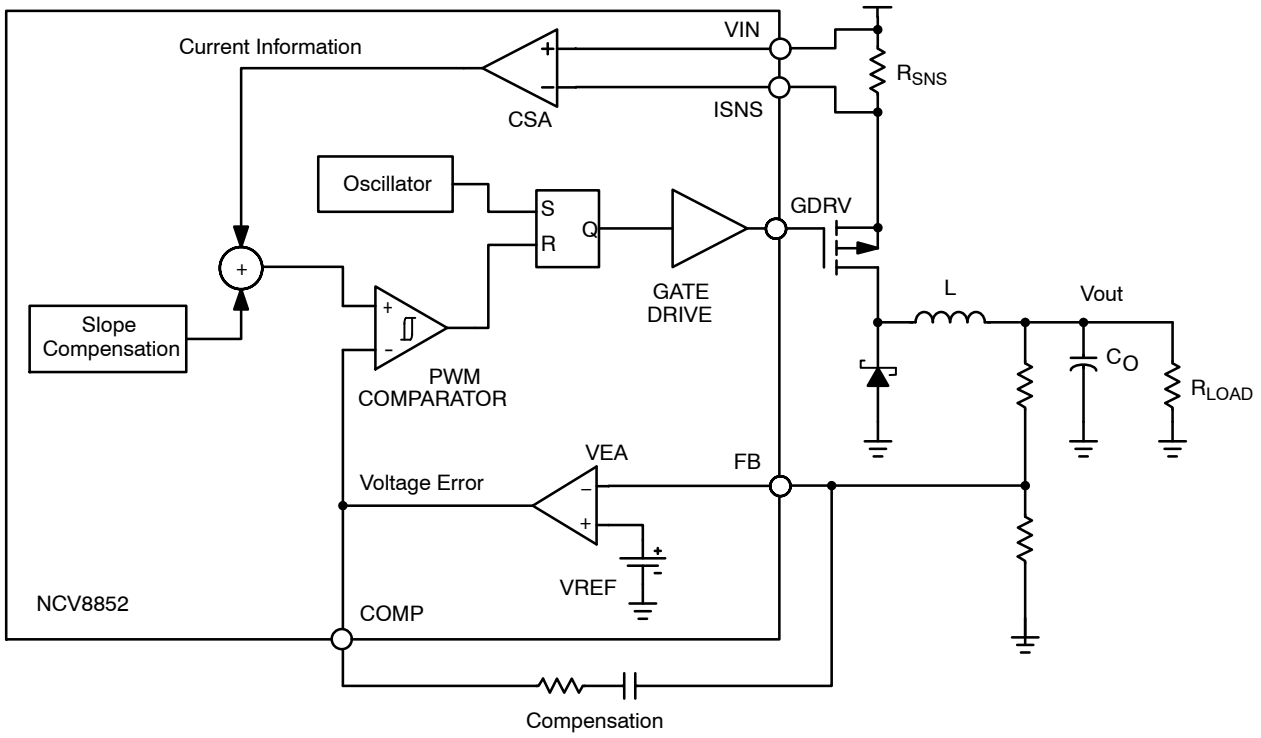


Figure 15. Current Mode Control Schematic

Current Mode Control

The NCV8852 SMPS incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived from the resistor in the power path, the signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

The NCV8852 also includes a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Overcurrent Protection

The NCV8852 features two current limit protections: peak current mode and overcurrent hiccup mode. When the current sense amplifier detects a voltage above the peak current limit between V_{IN} and ISNS after the current limit leading edge blanking time, the peak current limit causes the power switch to turn off for the remainder of the cycle. Set the current limit with a resistor from V_{IN} to ISNS, with $R = 0.100 / I_{limit}$.

If the voltage across the current sense resistor exceeds the overcurrent threshold voltage the part enters overcurrent hiccup mode. The part will remain off for the hiccup time and then go through the power on reset procedure.

Short Circuit Hiccup Protection

When the output voltage falls below the short circuit trip voltage the part enters short circuit latch off. When a short is detected the NCV8852 disables the outputs and attempts to re−enable the outputs after the short circuit hiccup time. The part remains off for the hiccup time and then goes through the power on reset procedure. If the short has been removed then the output stage re−enables and operates normally; however, if the short is still present the cycle begins again. Internal heat dissipation is kept to a minimum as current will only flow during the reset time of the protection circuitry. The hiccup mode is continuous until the short is removed.

Gate Drive

To turn on the P−Channel MOSFET, the gate driver turns on a current source to ground. A clamp ensures that the gate drive voltage does not exceed 10 V. When the clamp starts conducting the current source starts to turn off. To turn off the external MOSFET, the gate driver turns on a current source to V_{IN}.

100% Duty Cycle Operation

Each cycle, the oscillator allows either a maximum duty cycle up to 93% or 100% duty cycle operation. The oscillator does not allow duty cycles between 93% and 100%.

Every cycle, the oscillator determines whether an off−time is necessary. If so, the oscillator creates a duty cycle up to 93%. If an off−time is not required, it can be skipped and 100% duty cycle is allowed for the cycle.

Below are a few examples of what this could look like on the switching node:

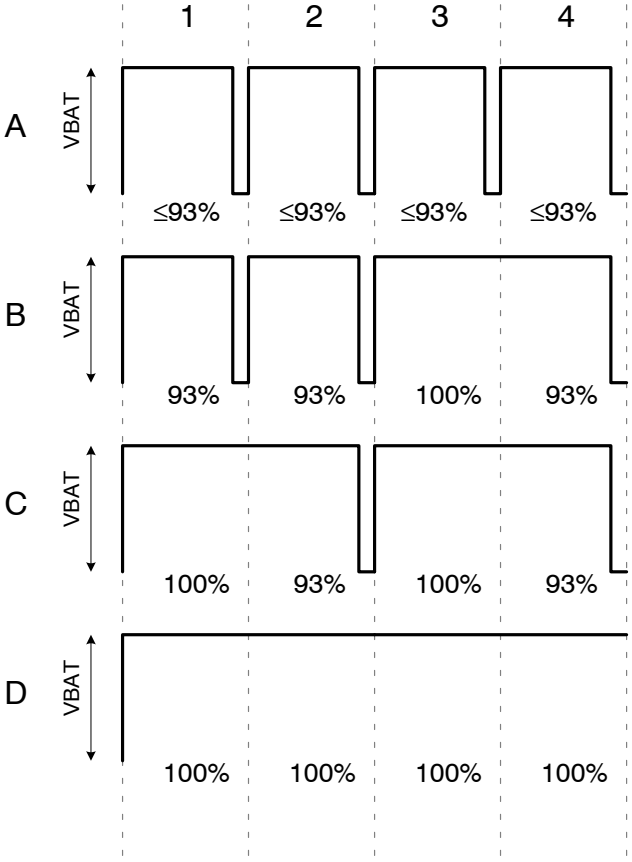


Figure 16. Duty Cycle Timing

A: Continuous operation. Each period has a duty cycle that is less than or equal to 93%.

B: One off−time is skipped in period 3, while the minimum off−time is maintained in periods 1, 2, and 4.

C: An off−time is skipped in period 1 and in period 3, while the minimum off−time is maintained in periods 2 and 4.

D: Low input voltage causes the IC to regulate at continuous 100% duty cycle (dropout).

EN/SYNC

This pin has three modes. When a dc logic high (CMOS/TTL compatible) voltage is applied to this pin the NCV8852 operates at the R_{OSC} programmed frequency. When a dc logic low voltage is applied to this pin the NCV8852 enters a low quiescent current sleep mode. When a square wave of at least 80% of the switching frequency is applied to this pin the switcher operates at the same frequency as the square wave. If the signal is slower than 80% of the switching frequency, it will be interpreted as enabling and disabling the part. The falling edge of the square wave corresponds to the start of the switching cycle.

R_{OSC}

The default setting is an open ROSC pin, allowing the oscillator to run at 170 kHz. Adding a resistor to GND increases the switching frequency. A resistor in series with a voltage source greater than 1.0 V will decrease the switching frequency.

Overvoltage Lockout

To protect the IC, if the voltage on the VIN pin the exceeds V_{ovlo} the NCV8852 will shutdown. When the voltage drops below this voltage the part will go through the normal soft start procedure.

Undervoltage Lockout

Undervoltage lockout protection is engaged when the input voltage drops below the V_{uvlo} signal. The part will remain off until the input voltage rises above the V_{uvlo} value plus hysteresis. Depending on the desired output voltage, it is possible to engage the short-circuit hiccup mode before undervoltage lockout occurs.

Soft−Start

To ensure moderate inrush current and reduce output overshoot, the NCV8852 features a soft start which periodically adds charge to a capacitor until the final reference voltage is achieved. Charging does not depend on the switching frequency when using the ROSC pin. When using an external SYNC signal, however, charging is based on the switching frequency. If, for example, the NCV8852 is synchronized to twice the free running (not synced) frequency, the soft start will be half as long.

DESIGN METHODOLOGY

Choosing external components for the NCV8852 encompasses the following design process:

1. Define operational parameters
2. Select switching frequency
3. Select current sensor
4. Select a MOSFET
5. Select a diode
6. Select output inductor
7. Select output capacitors
8. Select compensator components

(1) Operating Parameter Definition

First, select feedback resistors to choose the output voltage as follows:

$$V_{OUT} = V_{REF} \cdot \frac{R_1 + R_2}{R_2}$$

where:

V_{OUT}: desired output voltage
R_1: upper feedback resistor (between VOUT and FB) [Ω]
R_2: lower feedback resistor (between FB and GND) [Ω]

For a 5.0 V output, set R_1 to 42.2 kΩ and R_2 to 8.06 kΩ.

Certain operating parameters must be defined before proceeding with the rest of the design. These are application dependent and include the following:

V_{IN}: input voltage, range from minimum to maximum with a typical value [V]
I_{OUT}: output current, range from minimum to maximum with an initial startup value
I_{CL}: desired typical current limit

A number of basic calculations must be performed up front to use in the design process, as follows:

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(max)}}$$

$$D = \frac{V_{OUT}}{V_{IN(typ)}}$$

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(min)}}$$

where:

D_{MIN}: minimum duty cycle (ideal) [%]
$V_{IN(max)}$: maximum input voltage [V]
D: typical duty cycle (ideal) [%]
$V_{IN(typ)}$: typical input voltage [V]
D_{MAX}: maximum duty cycle (ideal) [%]
$V_{IN(min)}$: minimum input voltage [V]

(2) Switching Frequency Selection

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values to achieve the same inductor current ripple and output voltage ripple. However, increasing the frequency increases the switching losses of the MOSFETs, leading to decreased efficiency, especially noticeable at light loads.

Typically, the switching frequency is selected to avoid interfering with signals of known frequencies. The graph in Figure 17, below, shows the required resistance to program the frequency. From 200 kHz to 500 kHz, the following formula is accurate to within 3% of the expected value:

$$R_{OSC} = \frac{2859}{F_{SW} - 170}$$

where:

F_{SW}: desired switching frequency [kHz]
R_{OSC}: resistor from ROSC pin to GND [kΩ]

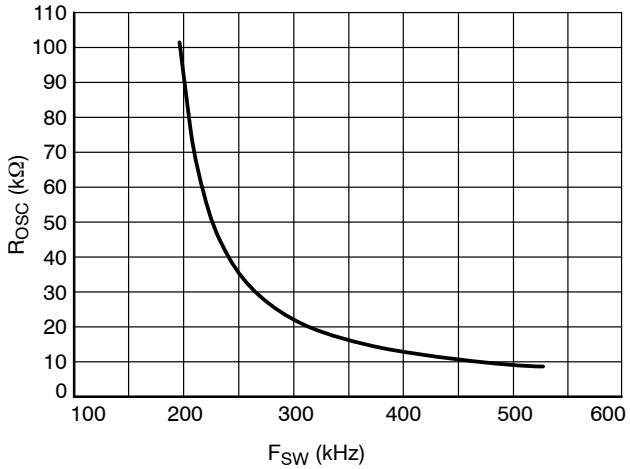


Figure 17. Frequency vs. ROSC

(3) Current Sensor Selection

Current sensing for peak current mode control relies on the inductor current signal. This is translated into a voltage via a current sense resistor, which is then measured differentially by the current sense amplifier, generating a single−ended output to use as a signal. The easiest means of implementing this transresistance is through the use of a sense resistor in series with the source of the MOSFET and VIN. A sense resistor should be calculated as follows:

$$R_{SNS} = \frac{V_{CL}}{I_{CL}}$$

where:

R_{SNS}: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desired cycle−by−cycle current limit [A]

(4) MOSFET Selection

The NCV8852 has been designed to work with a P−channel MOSFET in a non−synchronous buck configuration. The MOSFET needs to be capable of handling the maximum allowable current in the system, I_{CL}. Keep in mind that, depending on your minimum V_{IN} signal, it is possible to achieve 100% duty cycle. The power dissipated through the MOSFET during conduction is as follows:

$$P_{MOS,on} = I_{CL}^{2} \cdot D_{MAX} \cdot r_{DS,on}$$

where:

$P_{MOS,on}$: power through MOSFET [W]
I_{CL}: cycle−by−cycle current limit [A]
$r_{DS,on}$: on−resistance of the MOSFET [Ω]

To calculate the switching losses through the MOSFET, use the following equation:

$$P_{MOS,sw} = \frac{1}{2} V_{IN} \cdot I_{OUT} \cdot \left(t_{on} + t_{off}\right) \cdot F_{SW}$$

$$t_{on} = t_{off} = \frac{Q_{Gate}}{I_{drv}}$$

where:

$P_{MOS,\,sw}$: MOSFET switching losses [W]
t_{on}: time to turn on the MOSFET [s]
t_{off}: time to turn off the MOSFET [s]
Q_{Gate}: gate charge [C]
I_{drv}: gate drive current [A]

(5) Diode Selection

The diode must be chosen according to its maximum current and voltage ratings, and to thermal considerations.

The maximum reverse voltage the diode sees is the maximum input voltage (with some margin in case of ringing on the switch node). The maximum forward current is the peak current limit of the NCV8852, or 150% of I_{CL}.

(6) Output Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the power supply, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, an inductor is chosen for a set amount of current ripple and to assure adequate transient response.

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in the event of a load transient. A good starting point for peak−to−peak ripple is around 10% of the inductor current.To choose the inductor value based on the peak−to−peak ripple current, use the following equation:

$$i_L = \frac{V_{OUT} \cdot (1 - D_{MIN})}{L \cdot F_{SW}}$$

where:

i_L: peak−to−peak output current ripple [Ap−p]

From this equation it is clear that the ripple current increases as L decreases, emphasizing the trade−off between dynamic response and ripple current. The peak and valley values of the triangular current waveform are as follows:

$$I_{L(pk)} = I_{OUT} + \frac{i_L}{2}$$

$$I_{L(vly)} = I_{OUT} - \frac{i_L}{2}$$

where:

$I_{L(pk)}$: peak (maximum) value of ripple current [A]
$I_{L(vly)}$: valley (minimum) value of ripple current [A]

Saturation current is specified by inductor manufacturers as the current at which the inductance value has dropped from the nominal value, typically 10%. For stable operation, the output inductor must be chosen so that the inductance is close to the nominal value even at the peak output current, $I_{L(pk)}$, it is recommended to choose an inductor with saturation current sufficiently higher than the peak output current, such that the inductance is very close to the nominal value at the peak output current. This allows for a safety factor and allows for more optimized compensation.

Inductor efficiency is another consideration when selecting an output inductor. Inductor losses include dc and ac winding losses, which are very low due to high core resistance, and magnetic hysteresis losses, which increase with peak−to−peak ripple current. Core losses also increase as switching frequency increases.

Ac winding losses are based on the ac resistance of the winding and the RMS ripple current through the inductor, which is much lower than the dc current. The ac winding losses are due to skin and proximity effects and are typically much less than dc losses, but increase with frequency. Dc winding losses account for a large percentage of output inductor losses and are the dominant factor at switching frequencies at or below 500 kHz. The dc winding losses in the inductor can be calculated with the following equation:

$$P_{L(dc)} = I_{OUT}^{2} \cdot R_{dc}$$

where:

$P_{L(dc)}$: dc winding losses in the output inductor
R_{dc}: dc resistance of the output inductor (DCR)

(7) Output Capacitor Selection

The output capacitor is a basic component for the fast response of a power supply. In fact, for the first few microseconds of a load transient, they supply the current to the load. The controller recognizes the load transient and proceeds to increase the duty cycle to its maximum. Neglecting the effect of the ESL, the output voltage has a first drop due to ESR of the bulk capacitor(s).

$$\Delta V_{OUT(ESR)} = \Delta I_{OUT} \cdot ESR$$

A lower ESR produces a lower ΔV during load transient. In addition, a lower ESR produces a lower output voltage ripple.

In the case of stepping into a short, the inductor current approaches zero with the worst case initial current at the current limit and the initial voltage at the output voltage set point, calculating the voltage overshoot as follows:

$$\Delta V_{OS} = \sqrt{\frac{L \cdot I_{CL}^{2}}{C} + V_{OUT}^{2}} - V_{OUT}$$

Accordingly, a minimum amount of capacitance can be chosen for maximum allowed output voltage overshoot:

$$C_{MIN} = \frac{L \cdot I_{CL}^{2}}{\left(V_{OUT} + \Delta V_{OS(max)}\right)^{2} - V_{OUT}^{2}}$$

where:

C_{MIN}: minimum amount of capacitance to minimize voltage overshoot to $\Delta V_{OS(max)}$ [F]

$\Delta V_{OS(max)}$: maximum allowed voltage overshoot during a short [V]

(8) Select Compensator Components

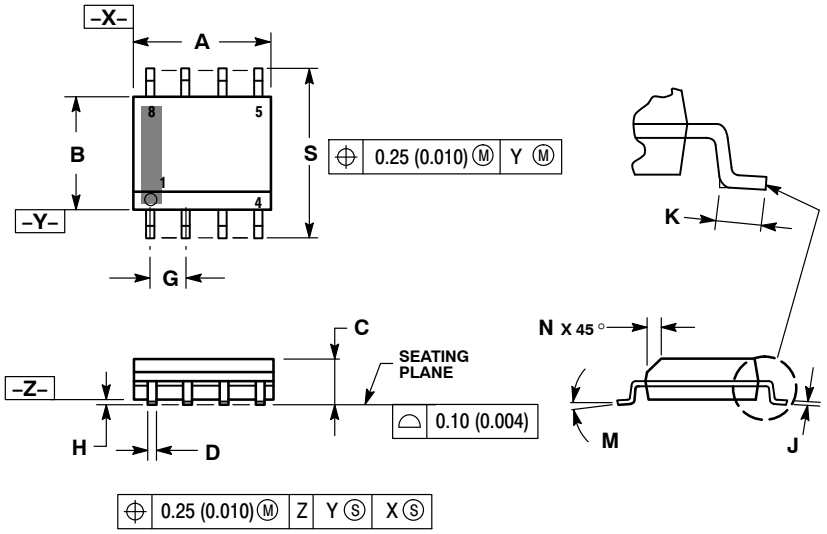
The Current Mode control method employed by the NCV8852 allows the use of a simple, Type II compensation to optimize the dynamic response according to system requirements. Using a simulation tool such as CompCalc can assist in the selection of these components.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

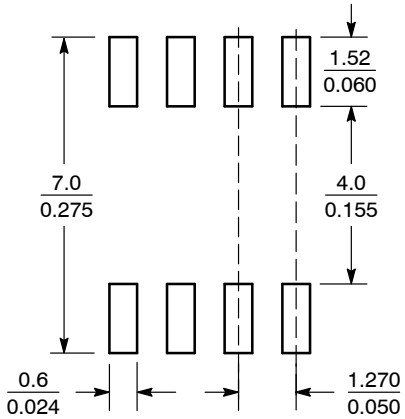
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

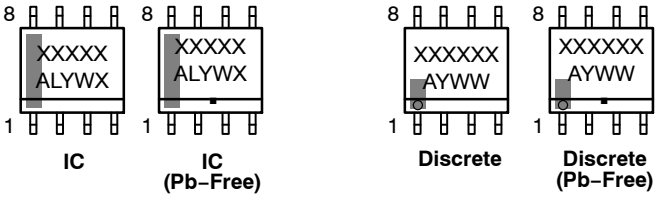
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales