FAIRCHILD SEMICONDUCTOR®

HUFA75852G3_F085

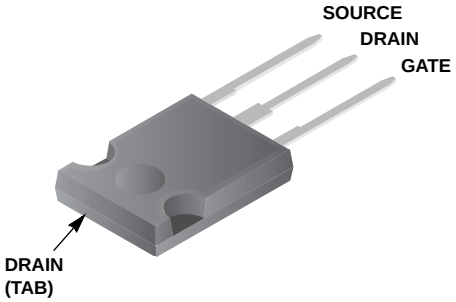
Data Sheet **December 2011**

75A, 150V, 0.016 Ohm, N-Channel, UltraFET® Power MOSFET

UltraFET™

Packaging

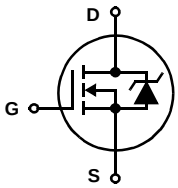
JEDEC TO-247



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)}$ = 0.016Ω, V_{GS} = 10V
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Qualified to AEC Q101
- RoHS Compliant

Symbol



Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA75852G3_F085	TO-247	75852G

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HUFA75852G3_F085	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	150	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	150	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous ($T_C = 25^oC$, V_{GS} = 10V) (Figure 2)	I_D	75	A
Continuous ($T_C = 100^oC$, V_{GS} = 10V) (Figure 2)	I_D	75	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 14, 15	
Power Dissipation	P_D	500	W
Derate Above 25^oC		3.33	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief TB334	T_{pkg}	260	^oC

NOTE:

1. $T_J = 25^oC$ to 150^oC.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 140V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 135V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 10)	2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V (Figure 9)	-	0.013	0.016	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-247	-	-	0.30	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	30	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 10V)						
Turn-On Time	t_{ON}	V_{DD} = 75V, I_D = 75A V_{GS} = 10V, R_{GS} = 2.0Ω (Figures 18, 19)	-	-	260	ns
Turn-On Delay Time	$t_{d(ON)}$		-	22	-	ns
Rise Time	t_r		-	151	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	82	-	ns
Fall Time	t_f		-	107	-	ns
Turn-Off Time	t_{OFF}		-	-	285	ns
GATE CHARGE SPECIFICATIONS						
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V; V_{DD} = 75V, I_D = 75A, $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	400	480	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V	-	215	260	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V	-	15	17.5	nC
Gate to Source Gate Charge	Q_{gs}		-	25	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	66	-	nC
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	7690	-	pF
Output Capacitance	C_{OSS}		-	1650	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	535	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.25	V
		I_{SD} = 35A	-	-	1.00	V
Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	260	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	1830	nC

Typical Performance Curves

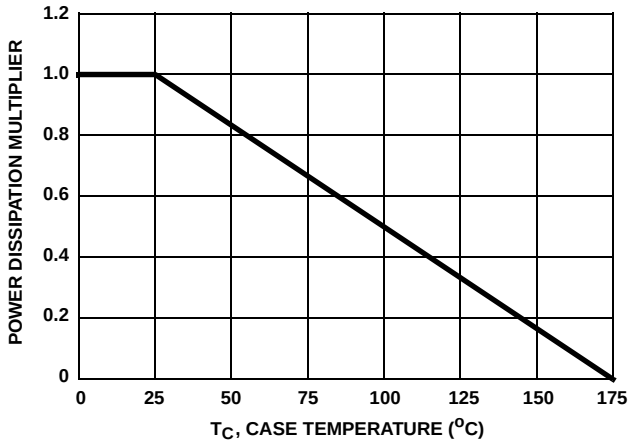


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

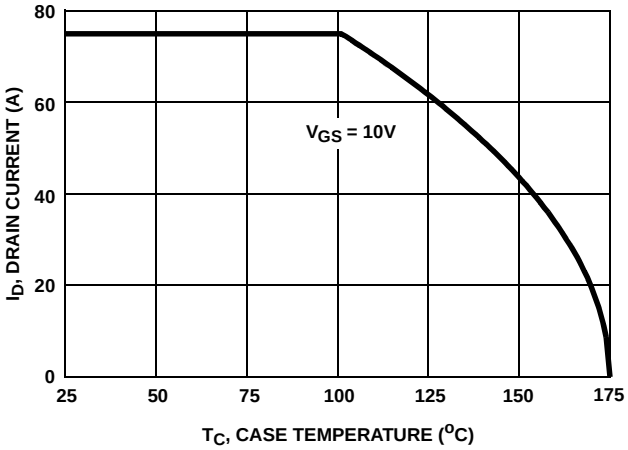


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

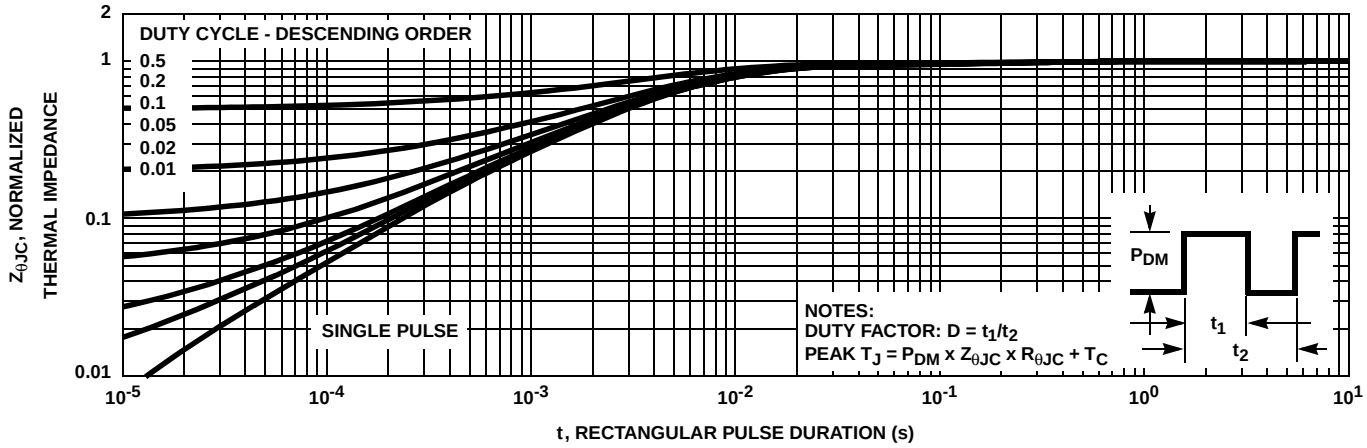


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

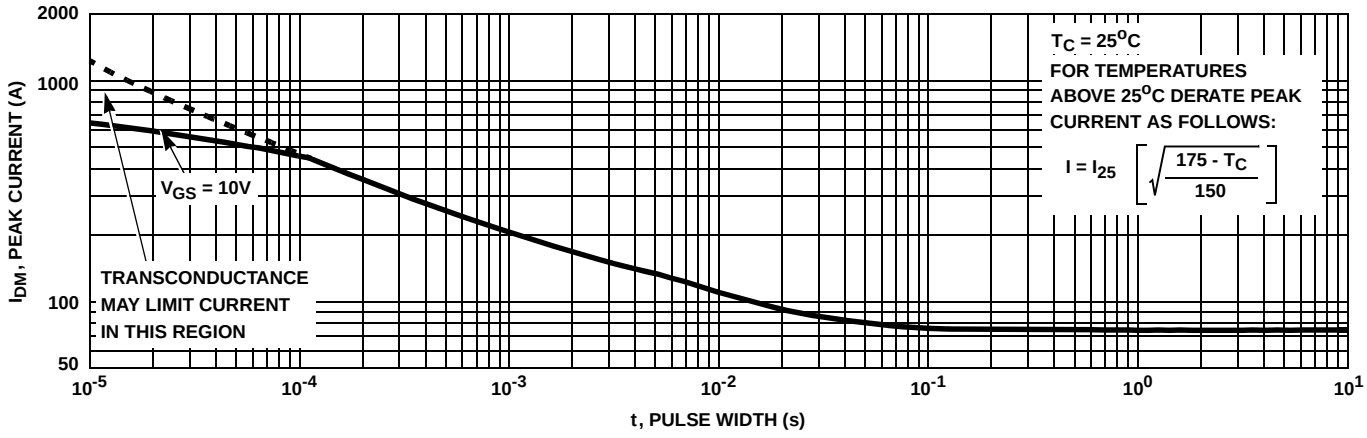


FIGURE 4. PEAK CURRENT CAPABILIT Y

Typical Performance Curves (Continued)

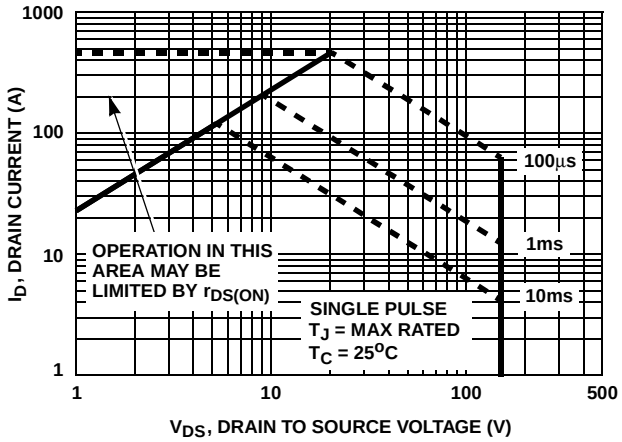
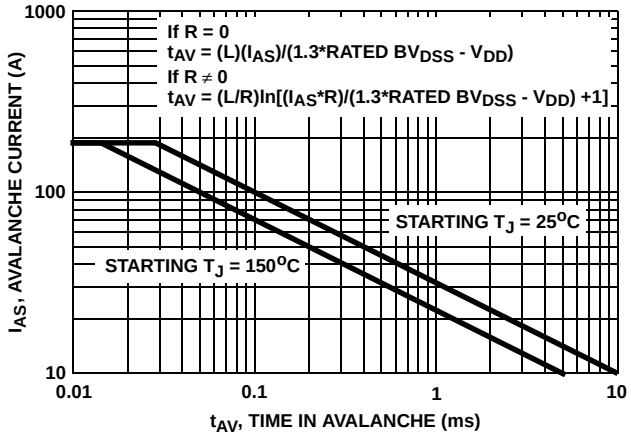


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

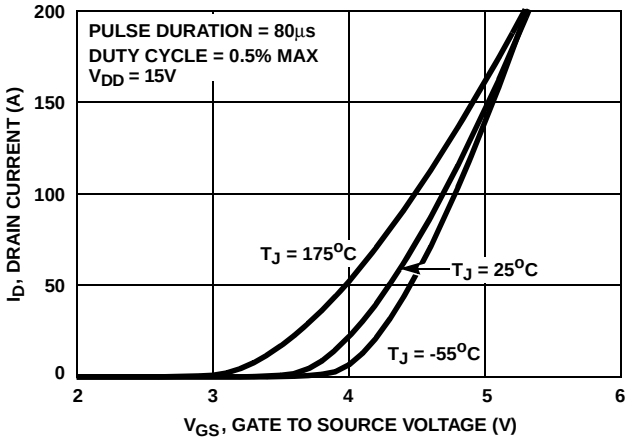


FIGURE 7. TRANSFER CHARACTERISTICS

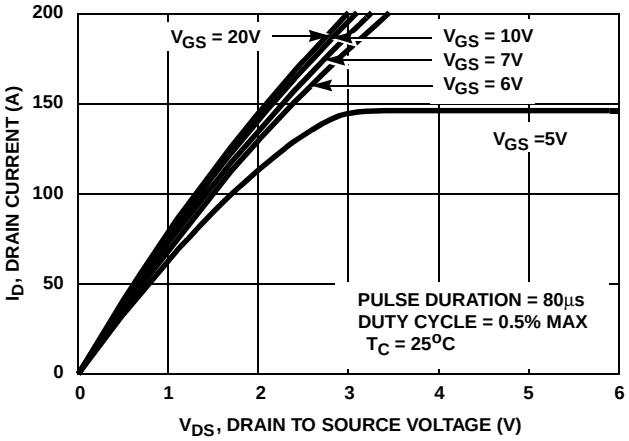


FIGURE 8. SATURATION CHARACTERISTICS

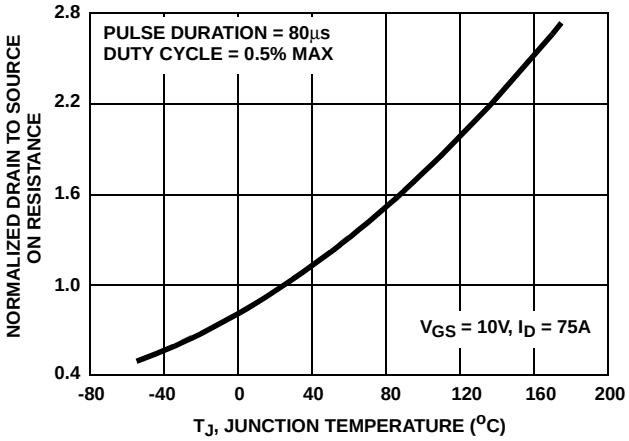


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

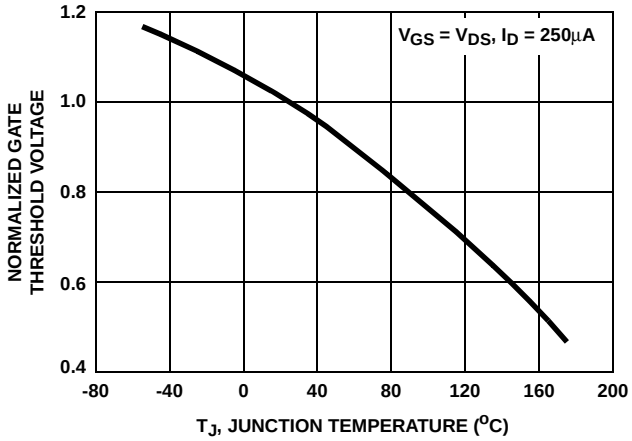


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

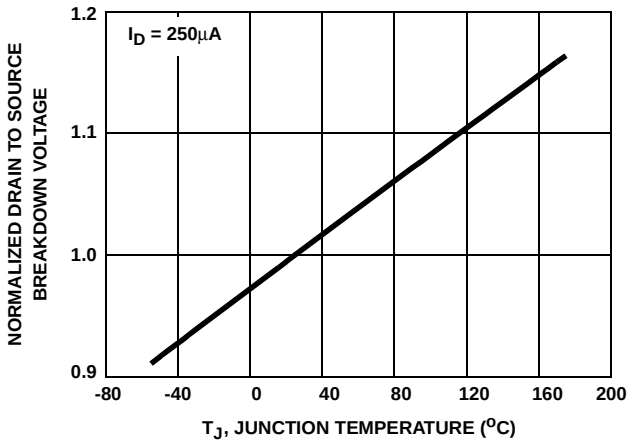


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

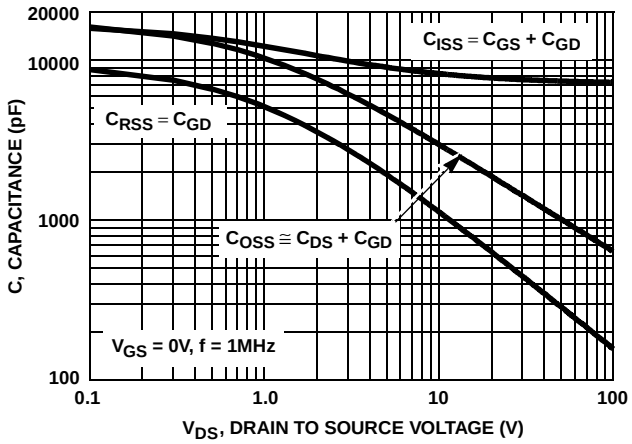
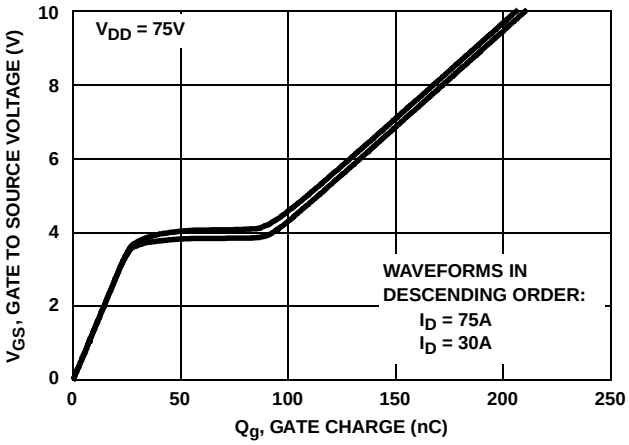


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

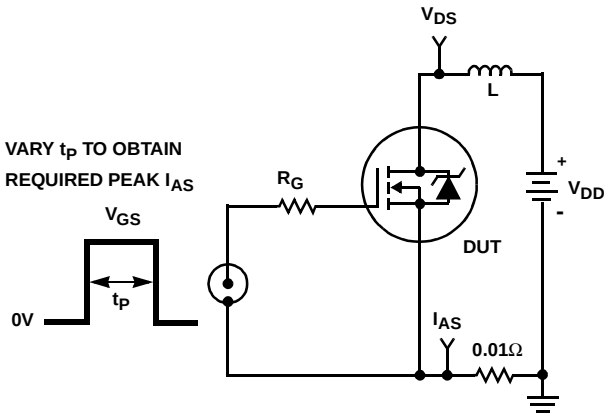


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

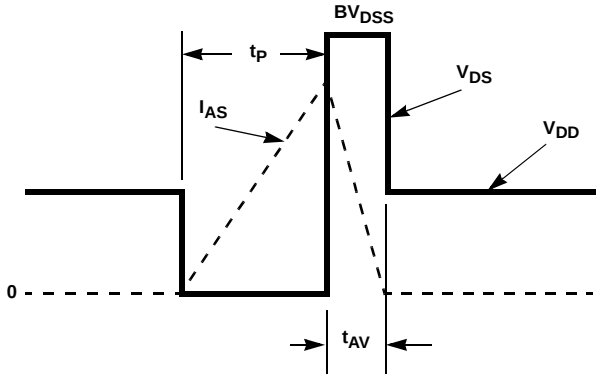


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

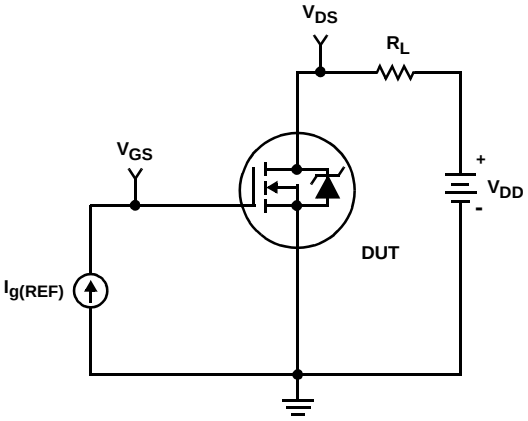


FIGURE 16. GATE CHARGE TEST CIRCUIT

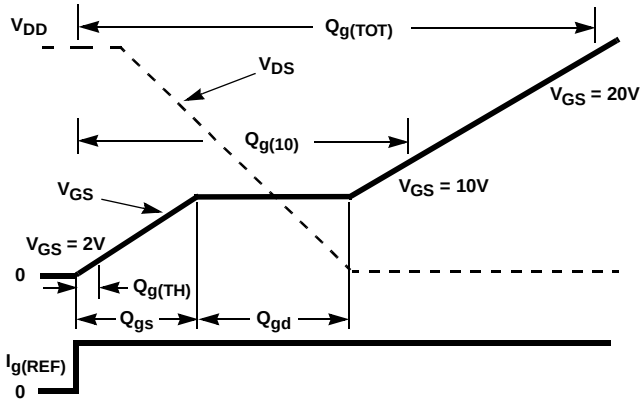


FIGURE 17. GATE CHARGE WAVEFORMS

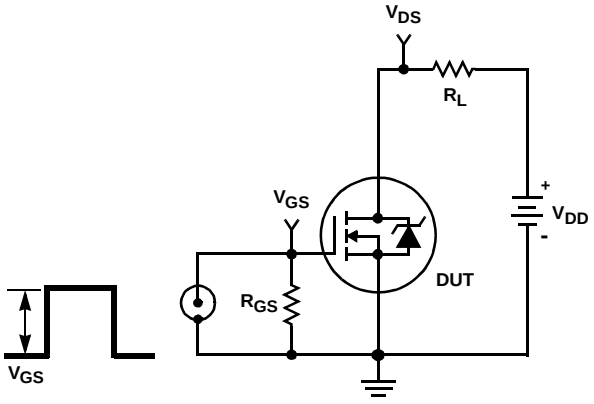


FIGURE 18. SWITCHING TIME TEST CIRCUIT

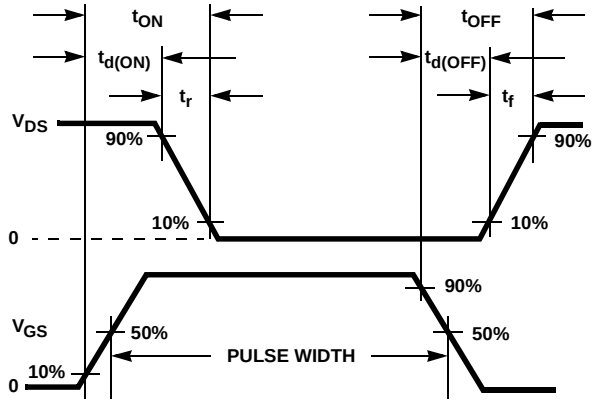


FIGURE 19. SWITCHING TIME WAVEFORM

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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