

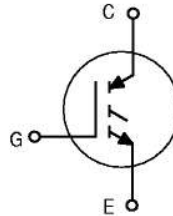
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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 by MGW20N120/D

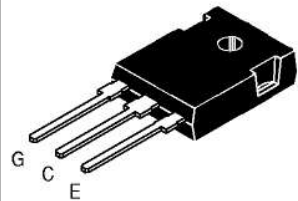
Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N-Channel Enhancement-Mode Silicon Gate

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO-247 Package with Isolated Mounting Hole
- High Speed E_{off} : 160 μ J/A typical at 125°C
- High Short Circuit Capability – 10 μ s minimum
- Robust High Voltage Termination


MGW20N120

Motorola Preferred Device

IGBT IN TO-247
20 A @ 90°C
28 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

CASE 340K-01
STYLE 4
TO-247AE
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	1200	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V_{CGR}	1200	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$	I_{C25}	28	Adc
— Continuous @ $T_C = 90^\circ\text{C}$	I_{C90}	20	
— Repetitive Pulsed Current (1)	I_{CM}	56	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	174	Watts
Derate above 25°C		1.39	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Short Circuit Withstand Time ($V_{CC} = 720 \text{ Vdc}$, $V_{GE} = 15 \text{ Vdc}$, $T_J = 125^\circ\text{C}$, $R_G = 20 \Omega$)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	35	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	$^\circ\text{C}$
Mounting Torque, 6-32 or M3 screw		10 lbf•in (1.13 N•m)	

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

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MGW20N120**ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage ($V_{GE} = 0\text{ Vdc}$, $I_C = 25\ \mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(BR)CES}$	1200 —	— 870	— —	Vdc mV/°C
Emitter-to-Collector Breakdown Voltage ($V_{GE} = 0\text{ Vdc}$, $I_{EC} = 100\text{ mAdc}$)	$V_{(BR)ECS}$	25	—	—	Vdc
Zero Gate Voltage Collector Current ($V_{CE} = 1200\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$) ($V_{CE} = 1200\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{CES}	— —	— —	100 2500	μAdc
Gate-Body Leakage Current ($V_{GE} = \pm 20\text{ Vdc}$, $V_{CE} = 0\text{ Vdc}$)	I_{GES}	—	—	250	nAdc

ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage ($V_{GE} = 15\text{ Vdc}$, $I_C = 10\text{ Adc}$) ($V_{GE} = 15\text{ Vdc}$, $I_C = 10\text{ Adc}$, $T_J = 125^\circ\text{C}$) ($V_{GE} = 15\text{ Vdc}$, $I_C = 20\text{ Adc}$)	$V_{CE(on)}$	— — —	2.42 2.36 2.90	3.54 — 4.99	Vdc
Gate Threshold Voltage ($V_{CE} = V_{GE}$, $I_C = 1.0\text{ mAdc}$) Threshold Temperature Coefficient (Negative)	$V_{GE(th)}$	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance ($V_{CE} = 10\text{ Vdc}$, $I_C = 20\text{ Adc}$)	g_{fe}	—	12	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{CE} = 25\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ies}	—	1860	—	pF
Output Capacitance		C_{oes}	—	122	—	
Transfer Capacitance		C_{res}	—	29	—	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	$(V_{CC} = 720\text{ Vdc}$, $I_C = 20\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$, $L = 300\ \mu\text{H}$, $R_G = 20\ \Omega$) Energy losses include "tail"	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	103	—	
Turn-Off Delay Time		$t_{d(off)}$	—	190	—	
Fall Time		t_f	—	284	—	
Turn-Off Switching Loss		E_{off}	—	1.65	2.75	
Turn-On Delay Time	$(V_{CC} = 720\text{ Vdc}$, $I_C = 20\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$, $L = 300\ \mu\text{H}$, $R_G = 20\ \Omega$, $T_J = 125^\circ\text{C}$) Energy losses include "tail"	$t_{d(on)}$	—	83	—	ns
Rise Time		t_r	—	107	—	
Turn-Off Delay Time		$t_{d(off)}$	—	216	—	
Fall Time		t_f	—	494	—	
Turn-Off Switching Loss		E_{off}	—	3.19	—	
Gate Charge	$(V_{CC} = 720\text{ Vdc}$, $I_C = 20\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$)	Q_T	—	62	—	nC
		Q_1	—	21	—	
		Q_2	—	25	—	

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L_E	—	13	—	nH
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(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

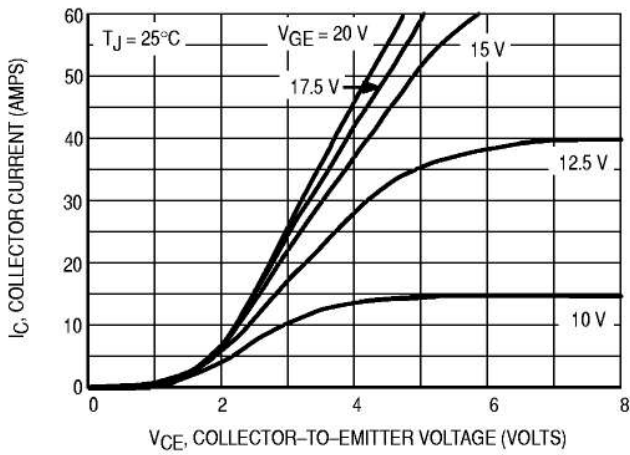


Figure 1. Output Characteristics

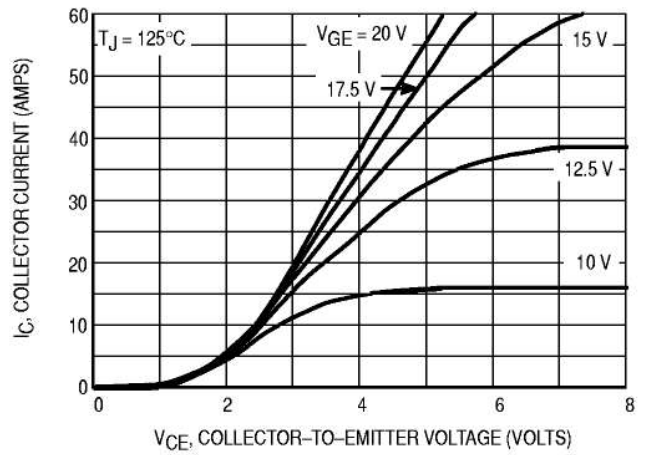


Figure 2. Output Characteristics

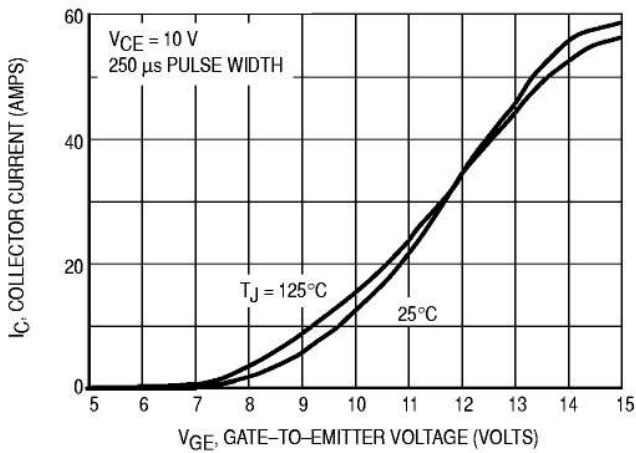


Figure 3. Transfer Characteristics

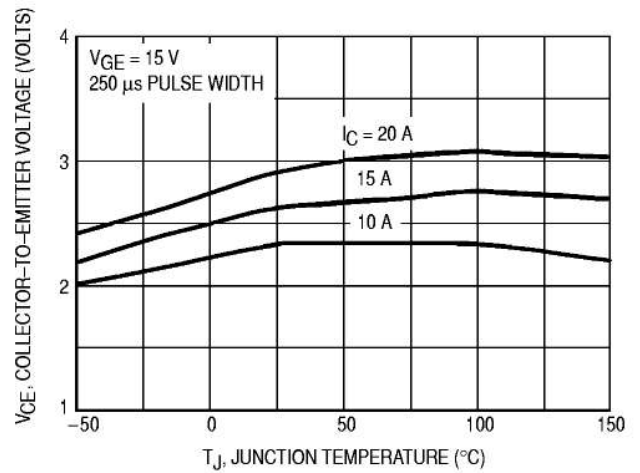


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

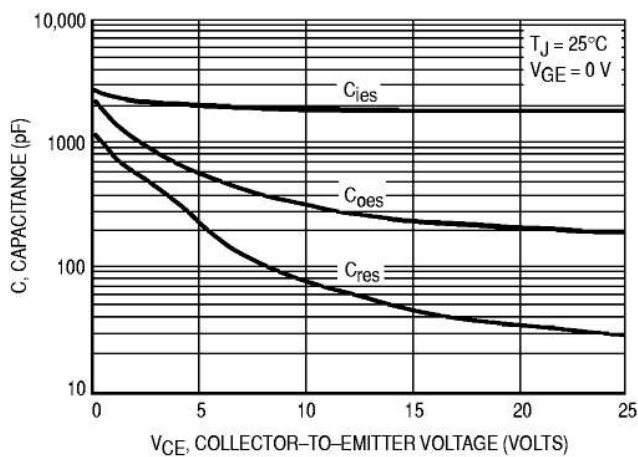


Figure 5. Capacitance Variation

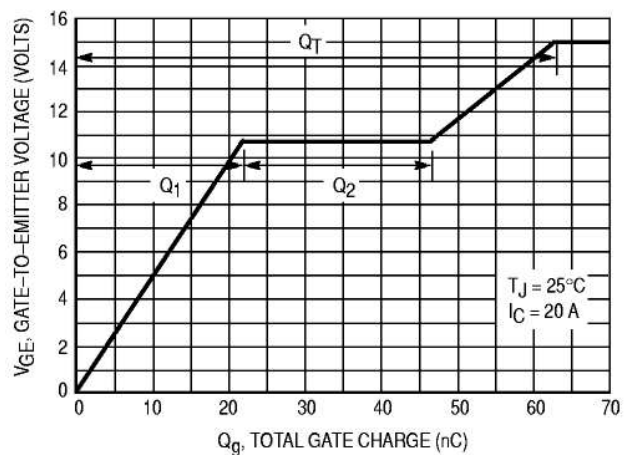


Figure 6. Gate-to-Emitter Voltage versus Total Charge

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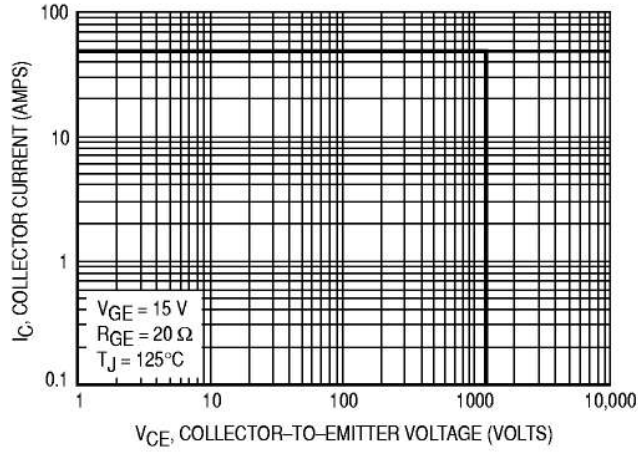


Figure 7. Reverse Biased Safe Operating Area

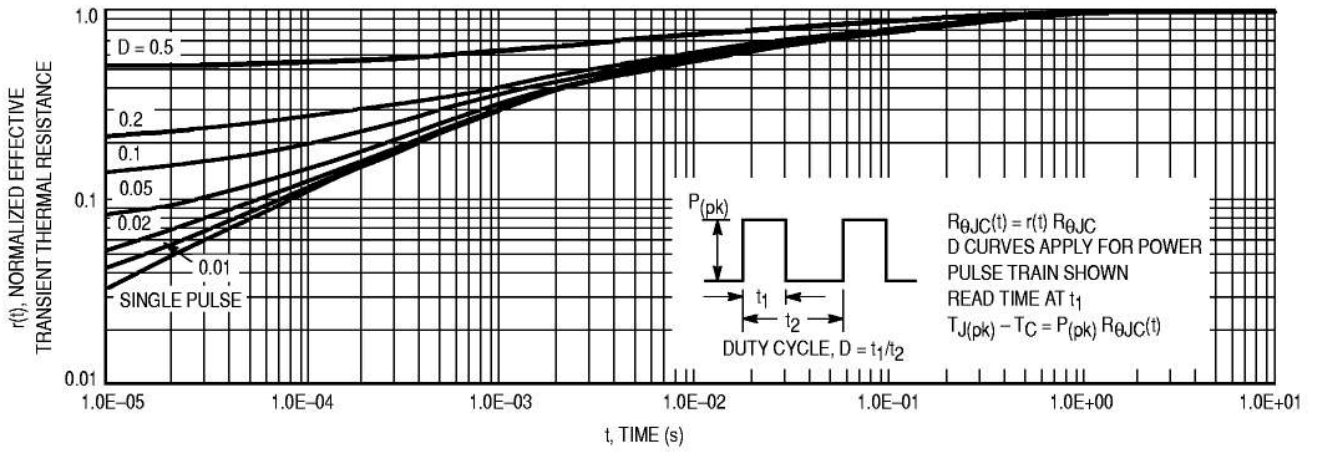
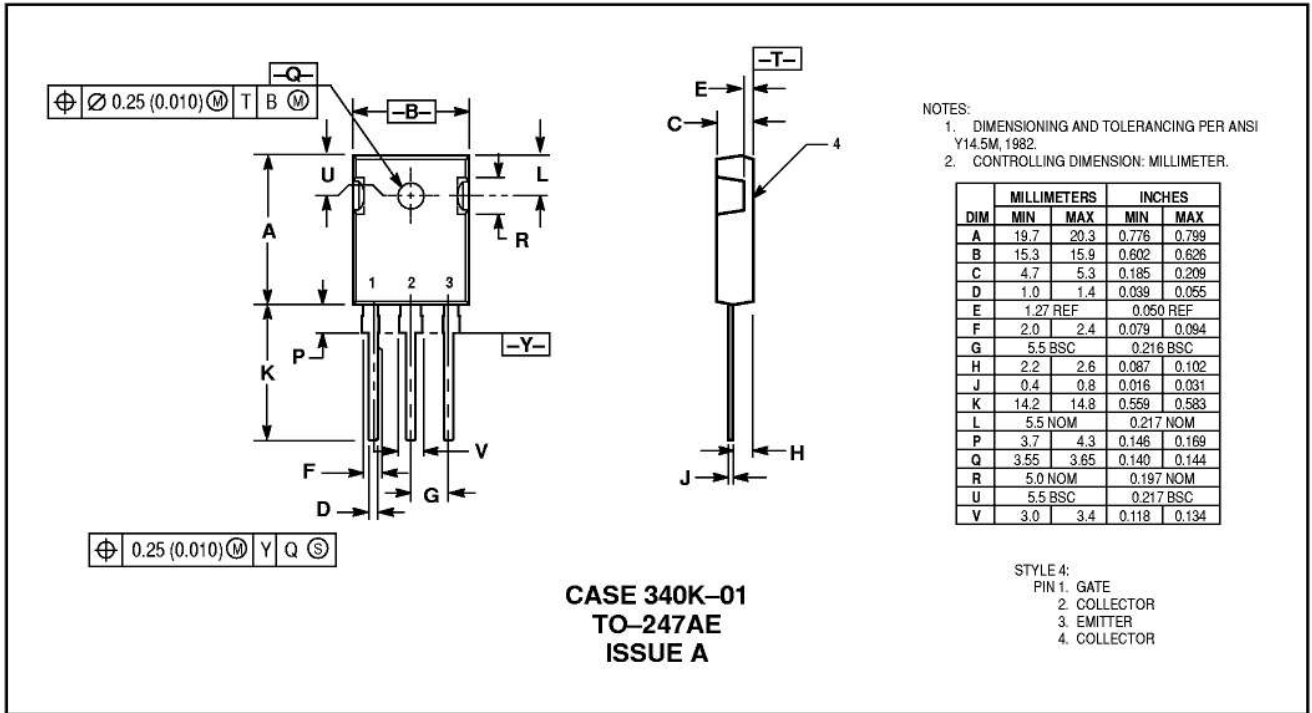


Figure 8. Thermal Response

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PACKAGE DIMENSIONS



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JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141,
 4-32-1 Nishi-Gotanda, Shagawa-ku, Tokyo, Japan. 03-5487-8488

Customer Focus Center: 1-800-521-6274

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 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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