PL460

PL460 Data Sheet

Description

The PL460 is a programmable modem for narrow-band Power Line Communication (PLC), able to run any PLC protocol in the frequency band below 500 kHz. PL460 embeds the PLC line driver, providing a highly integrated solution that reduces the total bill of materials, simplifies the layout and eases the modem design.

This device has been designed to comply with FCC, ARIB, KN60 and CENELEC EN50065 regulations matching requirements of the Internet of Things and Smart Energy applications. It supports state-of-the-art narrow-band PLC standards such as ITU G.9903 (G3-PLC®), ITU G.9904 (PRIME) as well as any other narrowband PLC protocols, at the same time being a future-proof platform able to support the evolution of these standards.

The PL460 is designed to be driven by external Microchip host devices, thus providing an additional level of flexibility on the host side. The Microchip host device loads the proper PLC-protocol firmware in the PL460 before modem operation and controls the PL460 modem.

Features

- Programmable Narrow-Band Power Line Communication (PLC) Modem
- Embedded PLC Class-D Amplifier
- Integrated PLC Front End:
  – PGA with automatic gain control and ADC
  – Digital transmission level control
  – Supports two independent transmission branches for the PLC signal
  – Up to 500 kHz PLC signal bandwidth
- Architecture:
  – High-performance architecture combining CPU, specific co-processors for digital signal processing and dedicated hardware accelerators for common narrow-band PLC tasks
- Cryptographic Engine and Secure Boot:
  – Secure boot: supports AES-128 CMAC for authentication, AES-128 CBC for decryption
  – Fuse programming control for decryption and authentication 128-bit keys
- Clock Management:
  – 24 MHz external crystal for system clock
- Power Management:
  – 3.3V external supply voltage for I/O, digital and analog
  – 1.25V internal voltage regulator for the core
  – 12V external supply for the PLC amplifier
  – Optimized power modes for specific operation profiles, including Low Power mode
- Package: Available in TFBGA-81, 10 mm*10 mm, 1.0 mm pitch
- Temperature Range: Industrial (-40ºC to +85ºC)

Table of Contents

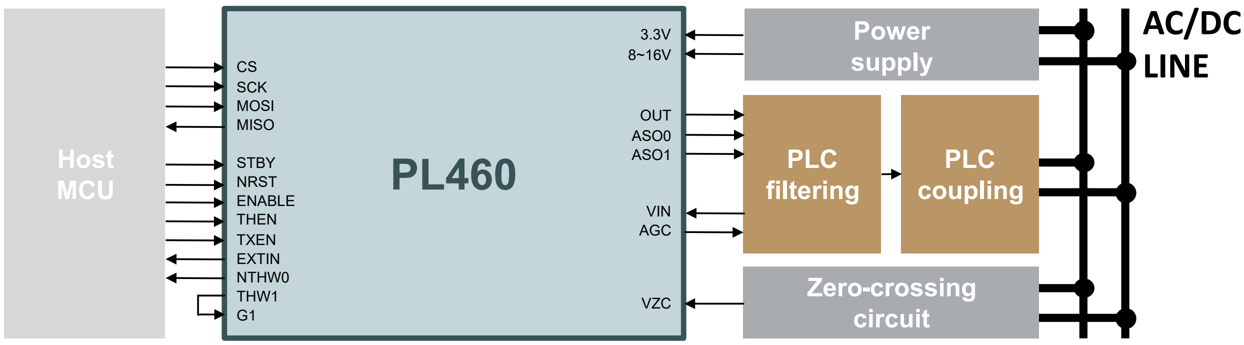
1. Typical Application of PL460

PL460 modem is designed to be managed by an external host microcontroller through a 4-line standard Serial Peripheral Interface (SPI).

Four additional signals allow the host to control the PL460: STBY, ENABLE, TXEN and NRST. Another signal EXTIN from the PL460 is used to signal events from the PL460 to the host controller.

The thermal monitoring functionality checks the internal temperature of the device and allows the PL460 to adapt its operation in case of overheating. The functionality is enabled using THEN input. Two output signals are used to generate different temperature warnings, NTHW0 and THW1. The first one, NTHW0, can be managed by the host controller. The second warning, THW1, is managed directly by the PL460 using the G1 input.

Figure 1-1. PL460 Application Example



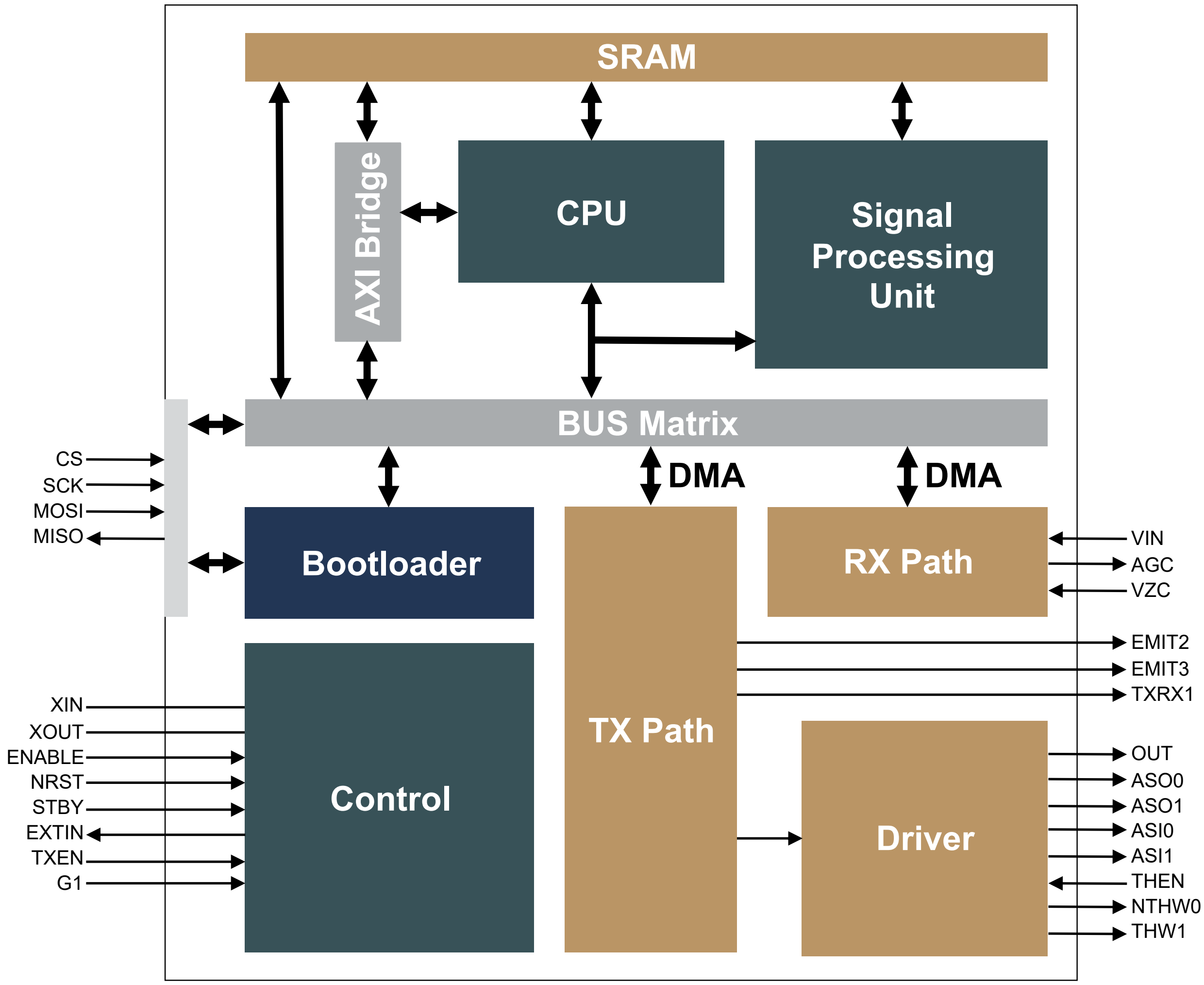
The zero-crossing detection (VZC) is an optional feature and its usage depends on the PLC protocol specification.

Check Microchip reference designs for a detailed description of the usage of the aforementioned control signals and features.

2. Block Diagram

The PL460 is a programmable PLC modem. It is composed of a high-performance core and a class-D amplifier line driver for the main transmission branch. The main functions of the high-performance core are to manage communication with the host controller and to run the lower layers of the PLC protocols.

Figure 2-1. PL460 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	3.3V Digital supply	Power	—	—	3.0V to 3.6V (1)
VDDIN	3.3V Voltage input for core voltage regulator	Power	—	—	3.0V to 3.6V (1)
VDDIN_AN	3.3V Analog supply (ADC + PGA)	Power	—	—	3.0V to 3.6V (2)
VDDCORE	1.25V Voltage Regulator Output with internal connection to Core power supply	Power	—	—	1.25V (3)
VDDPLL	1.25V PLL power supply input. Must be connected to VDDCORE through a LP filter	Power	—	—	1.25V (4)
VREGP	PLC Driver voltage regulator output for external decoupling capacitor	Power	—	—	(5)
VREGN	PLC Driver voltage regulator output for external decoupling capacitor	Power	—	—	(6)
PVDDAMP	Power supply of PLC driver amplifier and regulators	Power	—	—	8V to 16V (7)(8)
VDDAMP	3.3V Digital and analog power supply of PLC driver	Power	—	—	3.0 to 3.6V (9)
GND	Digital ground	Power	—	—	(10)
AGND	Analog ground	Power	—	—	(10)
PGND	Power ground of PLC driver	Power	—	—	(10)
GNDAMP	Analog ground of PLC driver	Power	—	—	(10)
Clocks, Oscillators and PLLs					
XIN	Crystal Oscillator Input	Input	—	VDDIO	—
XOUT	Crystal Oscillator Output	Output	—	VDDIO	—
Reset/Enable					
NRST	System Reset	Input	Low	VDDIO	(11)
ENABLE	Enable Internal core voltage regulator	Input	High	VDDIO	—
Power Line Communications					
OUT	Switching amplifier output	Output	—	PVDDAMP	—
ASO[0:1]	Analog Switch Outputs to disable the bandpass filtering when there is no PLC transmission activity	Output	—	PVDDAMP	High-voltage, high-current and low resistance analog switches.
ASI[0:1]	Analog Switch status	Output	—	VDDIO	—
VIN	PLC signal reception input	Input	—	VDDIN_AN	—

...........continued					
Signal Name	**Function**	**Type**	**Active Level**	**Voltage reference**	**Comments**
AGC	Automatic Gain Control. This digital tri-state output is managed by AGC hardware logic to drive external circuitry when input signal attenuation is needed	Output	—	VDDIO	(12)
VZC	Mains Zero-Cross Detection Signal. This input detects the zero-crossing of the mains voltage	Input	—	VDDIO	External Protection Resistor (12), (13)
VREFP	Internal Reference “Plus” Voltage	Analog	—	VDDIN_AN	(14)
VREFN	Internal Reference “Minus” Voltage	Analog	—	VDDIN_AN	(14)
VREFC	Internal Reference Common-mode Voltage	Analog	—	VDDIN_AN	(15)
EMIT[2:3]	PLC Tri-state Transmission ports	Output	—	VDDIO	—
TXRX1	Analog Front-End Transmission/Reception for the auxiliary transmission branch. This digital output is used to modify external coupling behavior in Transmission/Reception	Output	—	VDDIO	—
Input/Output					
STBY	Enable Sleep mode of the modem	Input	High	VDDIO	(16)
EXTIN	Indication of pending events	Output	Low	VDDIO	—
TXEN	Transmission enabled	Input	High	VDDIO	—
Thermal Monitor					
THEN	Enable Thermal Monitor functionality	Input	High	VDDIO	—
NTHW0	Indication of the first thermal warning	Output	—	VDDIO	—
THW1	Indication of the second thermal warning	Output	—	VDDIO	—
G1	General Purpose Input	Input	High	VDDIO	—
Serial Peripheral Interface - SPI					
CS	SPI Chip Select	Input	Low	VDDIO	Internal pull up (17)
SCK	SPI Clock signal	Input	—	VDDIO	Internal pull up (17)
MOSI	SPI Host Out Client In	Input	—	VDDIO	Internal pull up (17)
MISO	SPI Host In Client Out	Output	—	VDDIO	—

Notes:

1. Connecting two 100 nF decoupling multilayer ceramic capacitors (MLCC) to the VDDIO and VDDIN pins is recommended. In addition, for correct PLC transmission using the auxiliary branch, placing one 4.7 µF decoupling multilayer ceramic capacitor (MLCC) as close as possible to VDDIO pins D1 and D3 is strongly recommended.
2. Placing a 100 nF decoupling multilayer ceramic capacitor (MLCC) in the VDDIN_AN pins is recommended.
3. Placing 100 nF plus 2.2 µF decoupling multilayer ceramic capacitors (MLCC) in each pair of VDDCORE pins (H5-J5 and C1-C2) is recommended.
4. Placing 100 nF plus 4.7 µF decoupling multilayer ceramic capacitors (MLCC) in the VDDPLL pin is recommended.

5. A 100 nF multilayer ceramic capacitor (MLCC) is required between the ‘VREGP’ and ‘PVDDAMP’ pads for decoupling and stabilization purposes.
6. A 100 nF multilayer ceramic capacitor (MLCC) is required between the ‘VREGN’ and ‘GNDAMP’ pads for decoupling and stabilization purposes.
7. Placing one 100 uF aluminum Low-ESR 25V capacitor and three 100 nF 25V multilayer ceramic capacitors (MLCC) in the PVDDAMP pins is recommended.
8. The PLC-protocol firmwares provided by Microchip are configured by default for a power supply of the PLC driver amplifier of 12V.
9. Placing a 100 nF decoupling multilayer ceramic capacitor (MLCC) in the VDDAMP pins is recommended.
10. Separate pins are provided for GND, AGND, PGND and GNDAMP grounds. Taking these layout considerations into account to reduce interference is recommended. It is recommended to connect ground pins as short as possible to the system ground plane. For more details about EMC Considerations, refer to AVR040 Application Note.
11. It is recommended to connect the NRST signal to a GPIO in the host controller with an internal pull-down default reset configuration to help keep PL460 in reset until the host boots. For more details, refer to 6.1. Reset (NRST) Pin
12. See Table 11-4.
13. VZC is not isolated; some isolation circuitry is required in case of using a non-isolated design. Refer to the Reference Design for further information.
14. Bypass to analog ground with an external 22 nF decoupling capacitor and connect an external 10 nF decoupling capacitor between VREFP and VREFN.
15. Bypass to analog ground with an external 10 nF decoupling capacitor.
16. The STBY signal must be connected to GND if the Sleep mode functionality is not used. If using the Sleep mode functionality, the STBY signal must be connected to a GPIO in the host controller with an internal pull-down default reset configuration to avoid enabling Sleep mode until the host boots. For more details, refer to 6.3. Standby (STBY) Pin
17. See Table 11-5.

4. Package and Ballout

4.1 Packages

The PL460 is available in a TFBGA81 package. Refer to 12. Mechanical Characteristics for the TFBGA81 package mechanical drawing.

Table 4-1. PL460 Packages

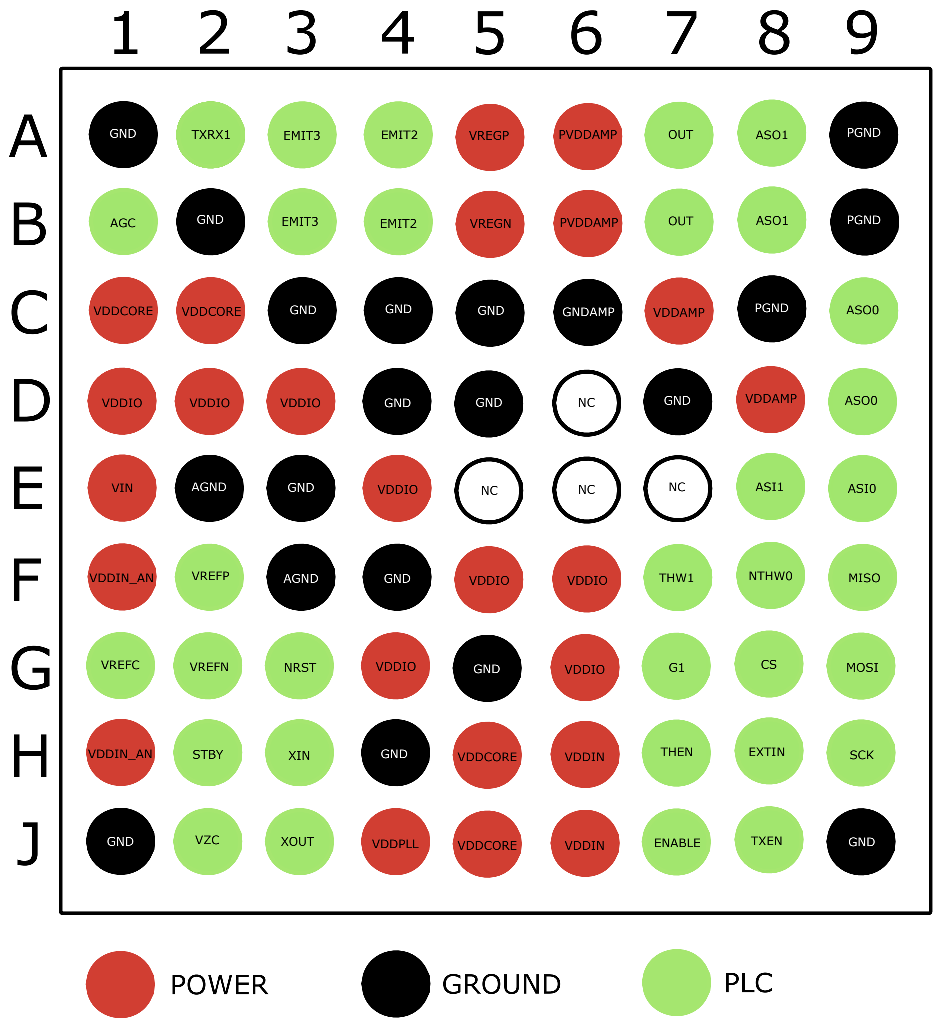
Package Name	Ball Count	Ball Pitch	Package Size
TFBGA81	81	1.00 mm	10 x 10 mm^2

4.2 Ballout

Table 4-2. PL460 Ballout

A1	GND	C1	VDDCORE	E1	VIN	G1	VREFC	J1	GND
A2	TXRX1	C2	VDDCORE	E2	AGND	G2	VREFN	J2	VZC
A3	EMIT3	C3	GND	E3	GND	G3	NRST	J3	XOUT
A4	EMIT2	C4	GND	E4	VDDIO	G4	VDDIO	J4	VDDPLL
A5	VREGP	C5	GND	E5	NC	G5	GND	J5	VDDCORE
A6	PVDDAMP	C6	GNDAMP	E6	NC	G6	VDDIO	J6	VDDIN
A7	OUT	C7	VDDAMP	E7	NC	G7	G1	J7	ENABLE
A8	ASO1	C8	PGND	E8	ASI1	G8	CS	J8	TXEN
A9	PGND	C9	ASO0	E9	ASI0	G9	MOSI	J9	GND
B1	AGC	D1	VDDIO	F1	VDDIN_AN	H1	VDDIN_AN		
B2	GND	D2	VDDIO	F2	VREFP	H2	STBY		
B3	EMIT3	D3	VDDIO	F3	AGND	H3	XIN		
B4	EMIT2	D4	GND	F4	GND	H4	GND		
B5	VREGN	D5	GND	F5	VDDIO	H5	VDDCORE		
B6	PVDDAMP	D6	NC	F6	VDDIO	H6	VDDIN		
B7	OUT	D7	GND	F7	THW1	H7	THEN		
B8	ASO1	D8	VDDAMP	F8	NTHW0	H8	EXTIN		
B9	PGND	D9	ASO0	F9	MISO	H9	SCK		

Figure 4-1. PL460 Ballout



4.3 Pinout Specification

Table 4-3. Pinout Specification

Ballout	Power Rail	I/O Type	Primary		Reset State
			Signal	Dir	Signal, Dir, Hiz, ST
A1	GND	Power	GND	—	—
A2	VDDIO	GPIO	TXRX1	I/O	PIO, I, Hiz
A3	VDDIO	PLC	EMIT3	O	O, Hiz
A4	VDDIO	PLC	EMIT2	O	O, Hiz
A5	PVDDAMP	Power	VREGP	—	—
A6	PVDDAMP	Power	PVDDAMP	—	—
A7	PVDDAMP	PLC	OUT	O	—
A8	PVDDAMP	PLC	ASO1	O	—

...........continued					
Ballout	Power Rail	I/O Type	Primary		Reset State
			Signal	Dir	Signal, Dir, Hiz, ST
A9	PGND	Power	PGND	—	—
B1	VDDIO	AGC	AGC	O	O, ST0
B2	GND	Power	GND	—	—
B3	VDDIO	PLC	EMIT3	O	O, Hiz
B4	VDDIO	PLC	EMIT2	O	O, Hiz
B5	PVDDAMP	Power	VREGN	—	—
B6	PVDDAMP	Power	PVDDAMP	—	—
B7	PVDDAMP	PLC	OUT	O	—
B8	PVDDAMP	PLC	ASO1	O	—
B9	PGND	Power	PGND	—	—
C1	VDDCORE	Power	VDDCORE	—	—
C2	VDDCORE	Power	VDDCORE	—	—
C3	GND	Power	GND	—	—
C4	GND	Power	GND	—	—
C5	GND	Power	GND	—	—
C6	GNDAMP	Power	GNDAMP	—	—
C7	PVDDAMP	Power	VDDAMP	—	—
C8	PGND	Power	PGND	—	—
C9	PVDDAMP	PLC	ASO0	O	—
D1	VDDIO	Power	VDDIO	—	—
D2	VDDIO	Power	VDDIO	—	—
D3	VDDIO	Power	VDDIO	—	—
D4	GND	Power	GND	—	—
D5	GND	Power	GND	—	—
D6			NC		Do not connect, reserved for test
D7	GND	Power	GND	—	—
D8	PVDDAMP	Power	VDDAMP	—	—
D9	PVDDAMP	PLC	ASO0	O	—
E1	VDDIN_AN	PLC	VIN	I	I, Hiz
E2	AGND	Ground	AGND	—	—
E3	GND	Power	GND	—	—
E4	VDDIO	Power	VDDIO	—	—
E5			NC		Do not connect, reserved for test
E6			NC		Do not connect, reserved for test

...........continued					
Ballout	Power Rail	I/O Type	Primary		Reset State
			Signal	Dir	Signal, Dir, Hiz, ST
E7			NC		Do not connect, reserved for test
E8	VDDIO	GPIO	ASI1	O	—
E9	VDDIO	GPIO	ASI0	O	—
F1	VDDIN_AN	Power	VDDIN_AN	—	—
F2	VDDIN_AN	Analog	VREFP	—	—
F3	AGND	Power	AGND	—	—
F4	GND	Power	GND	—	—
F5	VDDIO	Power	VDDIO	—	—
F6	VDDIO	Power	VDDIO	—	—
F7	VDDIO	GPIO	THW1	O	—
F8	VDDIO	GPIO	NTHW0	O	—
F9	VDDIO	GPIO	MISO	I/O	MISO, I, Hiz
G1	VDDIN_AN	Analog	VREFC	—	—
G2	VDDIN_AN	Analog	VREFN	—	—
G3	VDDIO	RST	NRST	I	I, Hiz
G4	VDDIO	Power	VDDIO	—	—
G5	GND	Power	GND	—	—
G6	VDDIO	Power	VDDIO	—	—
G7	VDDIO	GPIO	G1	I	PIO, I, Hiz
G8	VDDIO	GPIO	CS	I/O	CS, I, Hiz
G9	VDDIO	GPIO	MOSI	I/O	MOSI, I, Hiz
H1	VDDIN_AN	Power	VDDIN_AN	—	—
H2	VDDIO	GPIO	STBY	I	—
H3	VDDIO	CLOCK	XIN	I	I, Hiz
H4	GND	Power	GND	—	—
H5	VDDCORE	Power	VDDCORE	—	—
H6	VDDIN	Power	VDDIN	—	—
H7	VDDIO	GPIO	THEN	I	PIO, I, Hiz
H8	VDDIO	GPIO	EXTIN	O	PIO, I, Hiz
H9	VDDIO	GPIO	SCK	I/O	SCK, I, Hiz
J1	GND	Power	GND	—	—
J2	VDDIO	GPIO	VZC	I	VZC/PIO, I, Hiz
J3	VDDIO	CLOCK	XOUT	O	O
J4	VDDPLL	Power	VDDPLL	—	—

...........continued					
Ballout	Power Rail	I/O Type	Primary		Reset State
			Signal	Dir	Signal, Dir, Hiz, ST
J5	VDDCORE	Power	VDDCORE	—	—
J6	VDDIN	Power	VDDIN	—	—
J7	VDDIO	LDO	ENABLE	I	I, Hiz
J8	VDDIO	GPIO	TXEN	I	PIO, I, Hiz
J9	GND	Power	GND	—	—

Note:

HiZ = High Impedance, ST = Set To

5. Power Considerations

5.1 Power Supplies

The following table defines the power supply requirements of the PL460.

Table 5-1. Power Supplies

Name	Associated Ground	Description
VDDCORE	GND	Core power supply with internal connection to 1.25V voltage regulator output.
VDDIO	GND	3.3V Digital supply.
VDDIN	GND	3.3V Input for core voltage regulator.
VDDIN_AN	AGND	3.3V Analog supply (ADC + PGA).
VDDPLL	GND	1.25V Voltage Regulator Output. To be connected to VDDCORE through a low-pass filter.
PVDDAMP	PGND	8-16V Power supply of the embedded PLC driver
VDDAMP	GNDAMP	3.3V Digital and analog supply of PLC driver

The PL460 embeds a voltage regulator to supply the core. The Voltage Regulator state is controlled by the ENABLE pin. The VDDCORE pins in the package must be populated with external decoupling capacitors; connecting one 100 nF and one 2.2 μF capacitor to each pair of VDDCORE pins, C1-C2 and H5-J5, is recommended.

All ground pads GND, AGND and PGND must be connected at the PCB level. Furthermore, it is recommended to keep PGND and AGND nets in the PCB layout in separate power planes with a single point connection to GND. Refer to reference designs provided by Microchip for a reference layout.

Assuming previous described connections are done, the following decoupling capacitors are mandatory at the PCB level:

- MLCC 100 nF 10% 25V X7R 0603 between VREGN and GNDAMP
- MLCC 100 nF 10% 25V X7R 0603 between VREGP and VDD
- MLCC 100 nF 10% 25V X7R 0603 between VDDAMP and GND

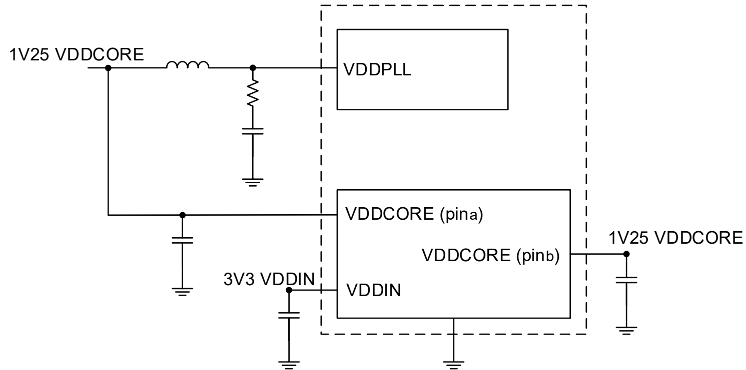
PVDDAMP decoupling capacitive network is highly dependent on final application. Refer to 3. Signal Description for the recommended decoupling network for NB-PLC cases.

5.2 Power Constraints

The following power constraints apply to the PL460 device. Deviating from these constraints may lead to unwanted device behavior.

- PVDDAMP must be stable when transmitting. A variation of 1V above or 2V below the configured PVDDAMP voltage can damage internal regulators and must be avoided. Microchip recommends to monitor PVDDAMP and, if the conditions described occurs, disable transmissions using pin TXEN.
- VDDIN and VDDIO must have the same level, 3.3V.
- VDDPLL voltage must be derived from VDDCORE through a low-pass filter. Using a second order LC with a cutoff frequency equal to 25 KHz is recommended. The inductor can be replaced by a ferrite bead, then a cutoff frequency equal to 75 KHz could be acceptable. In those cases, it is mandatory to check the communication performances of the system to detect problems originating from poor PLL supply filtering.

Figure 5-1. Core Voltage Regulator Connectivity[(1)]



Note:

1. Refer to 3. Signal Description and reference designs provided by Microchip for further information about recommended values of decoupling capacitors and low-pass filter components.

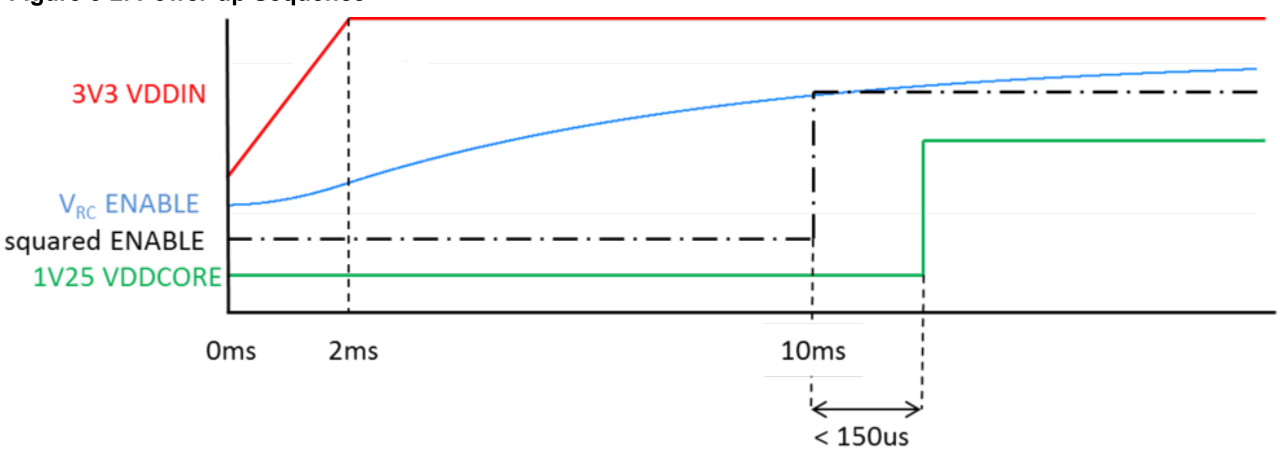
For more information on power considerations, refer to 11.8. Power On Considerations.

5.2.1 Power-up

VDDIO, VDDIN and VDDAMP must rise simultaneously, prior to VDDCORE and VDDPLL rising. This is respected if VDDCORE and VDDPLL are supplied by the embedded voltage regulator and the voltage regulator is turned on after VDDIN reaches 3.3V.

The figure below shows system response when an RC delay line (R = 6K8Ω, C = 1 μF) is used to derive ENABLE control from VDDIN.

Figure 5-2. Power-up Sequence



Although no special power-up sequence is required between high-voltage PVDDAMP power domain and low-voltage domain (VDDIO, VDDIN and VDDAMP), it is recommended to satisfy the ramp-up slopes defined in Table 5-2. The PL460 is designed to operate properly either with PVDDAMP pins powered-up while the low-voltage domain is not available as well as the other way around.

Table 5-2. Ramp-up Slopes of PLC Amplifier Power Supplies

Parameter	Min	Typ	Max	Unit
3.3V power supply ramp-up slope [(1)], [(2)]	0.6	—	24	V/ms
PVDDAMP power supply ramp-up slope [(1)], [(3)]	1.5	—	16	V/ms

Notes:

1. Power supply ramp-up slope recommended values take into account the recommended decoupling networks to be used on each supply rail, as well as output current capability of power supplies typically used in smart metering applications.
2. VDDAMP pins connected at the PCB level.
3. PVDDAMP pins connected at the PCB level.

5.2.2 Power-down

VDDIO, VDDIN and VDDAMP should fall simultaneously; VDDCORE and VDDPLL will fall later as the regulator VDDIN decreases.

6. Input/Output Lines

The PL460 has several kinds of input/output (I/O) lines to manage the device and different features related to the firmware running in the PL460.

6.1 Reset (NRST) Pin

The NRST pin is unidirectional. It is managed by the external host controller and can be driven low to provide a Reset signal to reset the PL460. It resets the core and the peripherals. There is no constraint on the length of the Reset pulse.

It is recommended to connect the NRST pin to a GPIO of the host controller whose reset state is configured as pull-down. If the GPIO reset configuration is high-impedance, a pull-down resistor connected to GND must be used to ensure the timing of the power-on sequence. If using a GPIO with pull-up as reset configuration, then a 100 nF capacitor connected to GND must be used to ensure the timing of the power-on sequence.

When using the Sleep mode functionality, the NRST and STBY signals must be connected to a GPIO in the host controller with an internal pull-down default reset configuration to avoid enabling Sleep mode until the host boots.

To enter Sleep mode, it is required to reset the device (driving the NRST pin low) before enabling the STBY input. To exit Sleep mode, the STBY pin must be disabled before releasing NRST.

Refer to 11.8. Power On Considerations to view the timing constraints using this pin.

6.2 Enable (ENABLE) Pin

The ENABLE pin is unidirectional. It is managed by the external host controller and has to be driven high to provide power to the core voltage regulator embedded in the PL460.

Refer to 11.8. Power On Considerations to view the timing constraints using this pin.

6.3 Standby (STBY) Pin

The STBY pin is unidirectional. It is managed by the external host controller to enable Sleep mode (driven high) while keeping the Reset (NRST) pin enabled (driven low). In Sleep mode, the core of the device and the peripherals are reset, reducing power consumption. The content of the RAM memory is maintained; therefore, the program reloading is not required when the PL460 returns to normal operating mode.

To avoid device malfunction due to an undefined status of the PLC line driver pins, the STBY pin only must be enabled (driven high) after the NRST is enabled (driven low). To exit Sleep mode, it is required to disable the STBY pin (driven low) first and, then, disable NRST (driven high).

When using the Sleep mode functionality, the NRST and STBY signals must be connected to a GPIO in the host controller with an internal pull-down default reset configuration to avoid enabling Sleep mode until the host boots.

If the Sleep mode is not required, the STBY pin must be connected to GND to avoid device malfunction due to undefined status of the PLC line driver pins.

6.4 External Interrupt (EXTIN) Pin

The EXTIN signal automatically indicates to the external host controller that the firmware running in the PL460 has one or more pending events to be consulted by the host controller.

6.5 Transmission Enabled (TXEN) Pin

The TXEN pin is unidirectional. It is managed by the external host controller and has to be driven high to enable the PLC transmission. If the transmissions are disabled, ongoing/programmed transmission (if any) will be aborted and subsequent requests will be denied.

6.6 Zero-Cross Detection (VZC) Pin

The VZC pin is unidirectional. The input signal must be a digital pulse train directly related to the mains voltage. For more information about how the PL460 detects the zero-cross, refer to 10.1.2. Zero-Crossing Detection.

Additionally, the VZC pin is used during fuse programming to enter in the programming mode. For more information about fuse programming, refer to 7.4.5. Fuse Programming.

6.7 Thermal Monitor (THEN, NTHW0, THW1, G1) Pins

An on-die temperature monitor with two warning thresholds and hysteresis is included in the PL460 to improve product reliability by avoiding high power dissipation situations. This risky condition might occur during PLC transmission in case of very low impedance load and high-level output signal conditions.

The input pin THEN is used to enable the thermal monitor functionality. Connecting it directly to the ENABLE pin is recommended to control both of them at the same time.

The open-drain outputs 'NTHW0' and 'THW1' are used to notify high temperature conditions as it is indicated in Table 6-1:

Table 6-1. Thermal Warning Temperature Threshold and Output Status

Output	Thermal Threshold (℃)		Output Status	
	Rise	Fall	$T_{die} \geq T_{th}$	$T_{die} < T_{th}$
NTHW0	110	100	Low	Hi-Z
THW1	120	110	Hi-Z	Low

The first output, NTHW0, can be connected to the host controller to manage the temperature warning, but the second output, THW1, must be connected directly to the PL460 in order to manage the temperature warning itself. The pin G1 is configured in the PLC-protocol firmware to be used as an input interrupt for the thermal warning THW1, so it is recommended to connect pins THW1 and G1 directly.

7. Bootloader

7.1 Description

The bootloader loads the program from an external host to the internal memory of the PL460. It allows loading of plain programs or secured programs. When a secured program is loaded, the original program length must be padded to become a multiple of 16 bytes, and the length (number of blocks, where a block is a 16 byte set) must be specified for correct signature validation and decryption.

Signature uses AES128 CMAC. Signature can be calculated over the {Encrypted Software} or over {Encrypted Software + Initialization Vector + Number of Blocks-1}. The number of blocks for signature calculation will be specified as a 16 byte integer number in the {image}, although the number is programmed as a 16-bit integer in the corresponding register of the bootloader.

Decryption of the secured program uses AES128 CBC.

When secured software transfer has been selected, system operation will not start unless signature validation and decryption pass correctly.

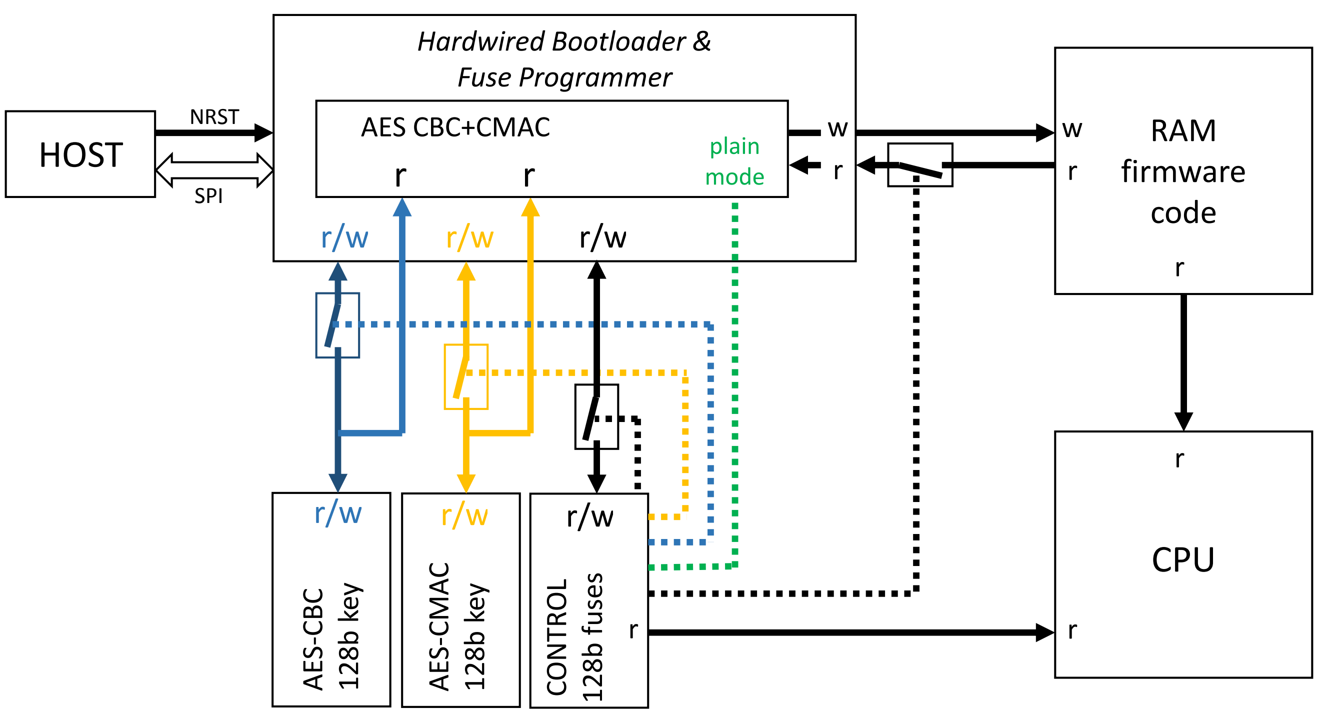
The bootloader also allows programming of security keys and security control fuses.

7.2 Embedded Characteristics

- Bootloader operates on SCK (typ. freq. 12 Mhz, max. freq ≤16 Mhz) synchronously with core and bus clocks
- Fixed phase and polarity SPI control protocol
- Password to unlock bootloader
- Fuse programming control

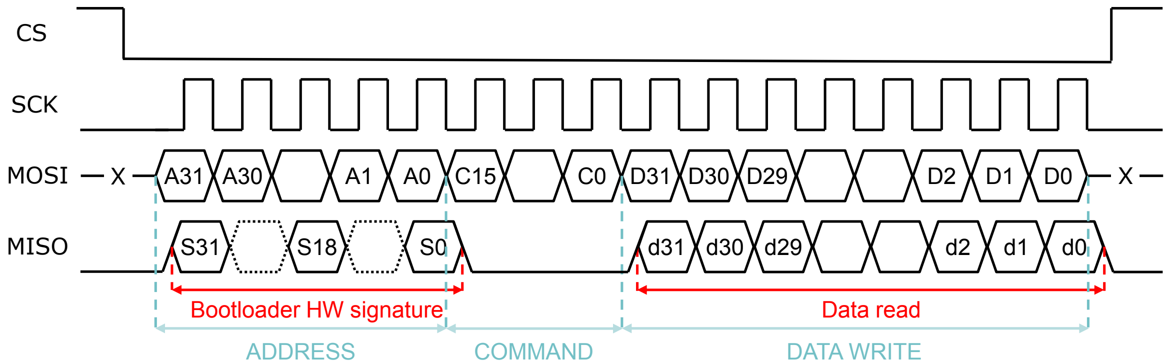
7.3 Block Diagram

Figure 7-1. Block Diagram



7.4 Functional Description

The bootloader loads the program from an external host to the internal memory of the PL460. The external host can access the instruction memory, data memory and registers through SPI. The bootloader only works in SPI Mode 0 (CPHA=1 and CPOL=0). The basic data transfer is:



The basic frame sent from the host through the MOSI signal is composed as shown in the following table:

Address	Command	Data
32-bit block	16-bit block	n blocks of 32 bits

All the blocks in the basic frame sent by MOSI use little-endian format.

Each frame received from the host will be acknowledged with a 32-bit signature through the MISO signal.

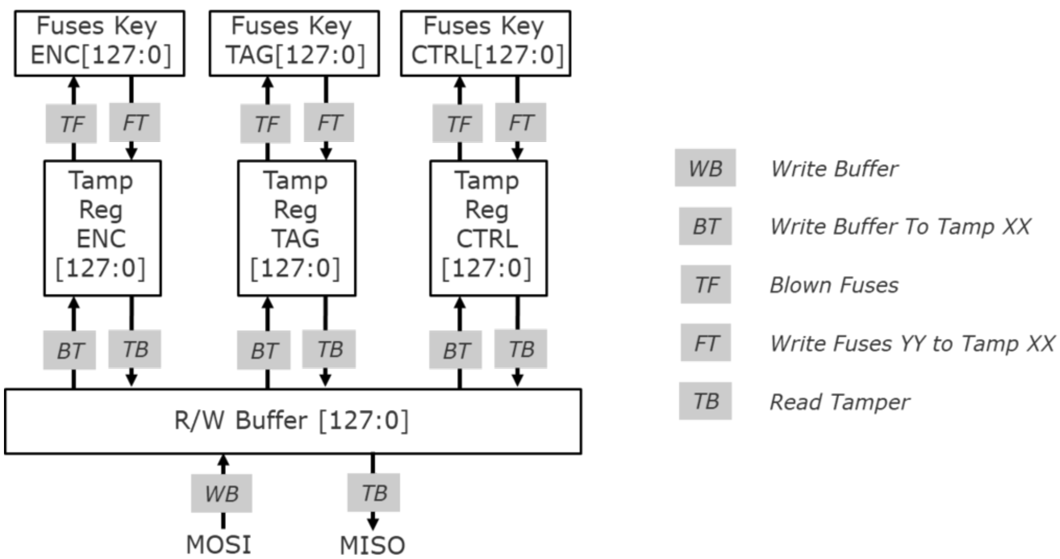
There is a series of SPI commands supported by the bootloader. The commands are:

Command	Description	addr(31:0)	data(n*32-1:0)
0x0000	Write word on one address	0xAAAAAAAA(1)	0xDDDDDDDD(2)
0x0001	Write words on consecutive addresses	0xAAAAAAAA(1)	0xDDD…DDD(2) (3)
0x0002	Read words on consecutive addresses	0xAAAAAAAA(1)	0x000…000(4)
0x0003	Read word on one address	0xAAAAAAAA(1)	0x00000000
0x0004	Write number of decryption packets	0x00000000	0x0000DDDD(2)
0x0005	Write decryption initial vector	0x00000000	0xDDD…DDD(2) (3)
0x0006	Write decryption signature	0x00000000	0xDDD…DDD(2) (3)
0x0007	Write 128 bit fuses value to Buffer register	0x00000000	0xDDD…DDD(2) (3)
0x0008	Write Buffer register to Tamper register for KEY_ENC_FUSES	0x00000000	0x00000000
0x0009	Write Buffer register to Tamper register for KEY_TAG_FUSES	0x00000000	0x00000000
0x000B	Write Buffer register to Tamper register for CONTROL_FUSES	0x00000000	0x00000000
0x000C	Blow desired fuses	0x00000000	0x00000000
0x000D	Write KEY_ENC_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x000E	Write KEY_TAG_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x0010	Write CONTROL_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x0011	Read Tamper register	0x00000000	0x000…000(4)
0x0012	Read bootloader status	0x00000000	0x00000000
0x0013	Start Decryption	0x00000000	0x00000000

...........continued			
Command	**Description**	**addr(31:0)**	**data(n*32-1:0)**
0x0014	Start/Stop BOOTLOADER access window in Host mode	0x00000000	0x00000000
0x0015	Start Decryption Plus	0x00000000	0x00000000
0xA55A	Control of MISO signal transferred to M7-SPI	0x00000000	0x00000000
0xA66A	Control of MISO signal transferred to M7-SPI and Bootloader clock disabled	0x00000000	0x00000000
0xDE05	Unblock bootloader	0x00000000	0xDDDDDDDD(2)

Notes:
1. ‘AA’ is an address byte.
2. ‘DD’ is a data byte.
3. Command contains as many bytes as needed to send.
4. Command contains as many ‘00’s as bytes wanted to be read.

The figure below shows the structure of the registers and data transfers for fuses and their control logic.



7.4.1 Unlock, Load Program and Start Loaded Program

After Reset, the bootloader is locked and the host must send two frames as a password to unlock the bootloader. These frames are:

Order	Address	Command	Data
1	0x00000000	0xDE05	0x5345ACBA
2	0x00000000	0xDE05	0xACBA5345

At this point, the host sends commands to the bootloader and it can start loading the program to the PL460. The program must be loaded starting with address 0x00000000.

After loading the program, it must be started. Starting the loaded program requires clearing the CPUWAIT bit of the MSSC Miscellaneous register (Address 0x400E1800) and transferring control of the MISO signal to the M7-SPI peripheral:

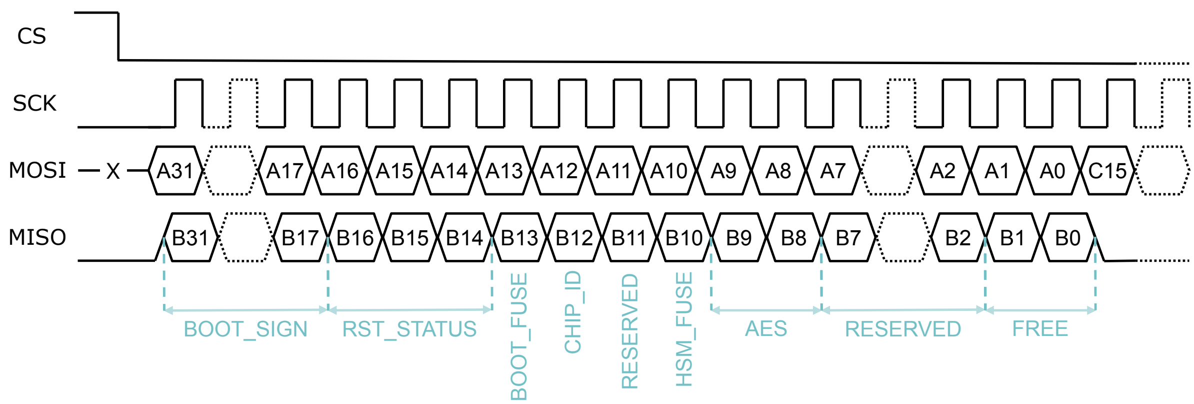
Order	Address	Command	Data
1	0x400E1800	0x0000	0x00000000
2	0x00000000	0xA66A	0x00000000

If this action is not done, the MISO signal will remain controlled by the BOOTLOADER.

7.4.2 Bootloader Hardware Signature

Each frame received from the host (write or read frame) will be acknowledged with a 32-bit signature through the MISO signal. This is used to give the bootloader's signature and the state of the system to the host.

This frame is composed of:



Bit	Name	Value
31..17	BOOT_SIGN	010101100011010
16	RST_STATUS	USER_RST
15		CM7_RESET
14		WDT_RESET
13	BOOT_FUSE	—
12	CHIP_ID	—
11	RESERVED	—
10	HSM_FUSE	—
9	AES_FUSES	AES_DIS
8		AES_128
7..2	RESERVED	—
1..0	FREE_FUSES	—

7.4.3 Write Process

The command used to write on a unique address is CMD=0x0000.

The command used to write on several consecutive addresses is CMD=0x0001. In this case, it will be sent the 32 bits of the initial address, 16 bits of the command (0x0001) and as many consecutive words (32 bits) as are wanted to write.

Regarding the decryption packets, the commands to write the number of decryption packets (CMD=0x0004), the initial vector of decryption (CMD=0x0005) or the decryption signature to test if decryption is correct (CMD=0x0006), the address of the frame is not taken into account and it can be composed of any address value. To write the decryption packet, only the last 15 bits are taken into account. In the case of decryption initial vector and decryption signature where it is necessary to send the 128-bit value as data, it is made in the same way as the write process at consecutive addresses, sending 4 consecutive words (32 bits).

To write a fuse box, the Buffer register must be written in advance (CMD=0x0007) and then the Tamper registers of KEY_ENC_BOX, KEY_TAG_BOX or CONTROL_BOX must be written with the content of the buffer (CMD=0x0008, CMD=0x0009 and CMD=0x000B respectively). Finally, to blow the desired fuses with the values in the corresponding Tamper register, the command (CMD=0x000C) must be sent with any address and any data value.

The end of this writing process is indicated in the answer of the bootloader status command (CMD=0x0012). If the writing process is active, bit 0 of the answer is ‘1’. In other cases, all data of the answer is ‘0’.

In the case of CONTROL_BOX, to activate the new values, it is also necessary to write the CONTROL_FUSES values to the corresponding Tamper register (CMD=0x0010).

7.4.4 Read Process

The CMD=0x0003 command reads a unique address.

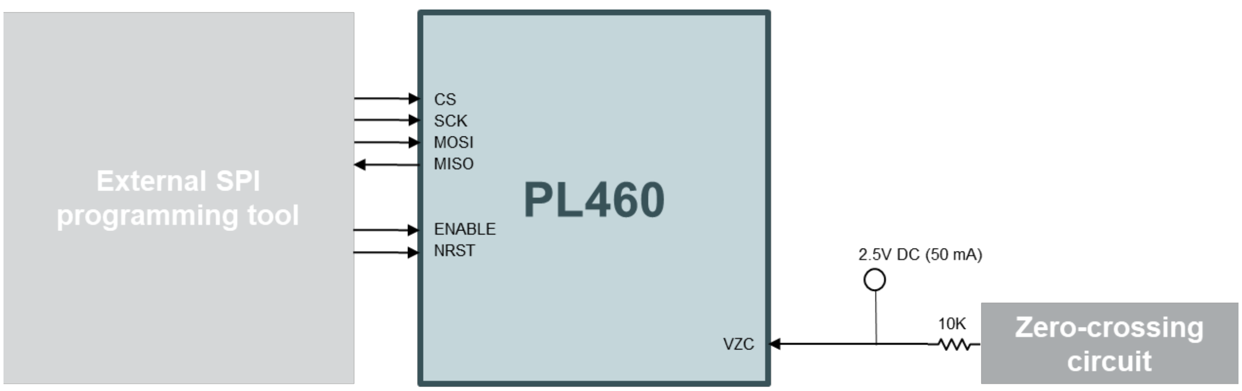
The CMD=0x0002 command reads several consecutive addresses. In this case the frame will be composed of 32 bits for the address, 16 bits for the command and as many SCK pulses (always multiple of 32) as needed to read data.

To read a fuse box, it must have been written previously in the corresponding Tamper register. The content of Tamper registers KEY_ENC_BOX, KEY_TAG_BOX or CONTROL_BOX are written to the buffer with the commands CMD=0x000D, CMD=0x000E and CMD=0x0010, respectively. Once the Tamper register is written, it can be read with the command CMD=0x0011.

7.4.5 Fuse Programming

To write control or key fuses, an external supply of 2.5V ±10% DC 50 mA supply must be connected to VZC pin. The voltage in VZC must be applied only after the PL460 is already powered (11.8. Power On Considerations) and maintained during the entire fuse programming process. If fuses are programmed in the system, the appropriate protection of VZC circuitry by means of a 10K resistor must be implemented, as it is shown in the figure below.

Figure 7-2. Externally Fuse Programming Setup



The fuse programming commands are sent through SPI. In case of using an external fuses programming controller, the host MCU SPI ports must be left in High-Impedance mode to allow the connection between the PL460 and the external fuses programming controller.

7.4.6 Control Fuses

The control fuse box includes 128 OTP (One-time programming) fuse bits. Only some of them are used to configure software security features (see table below). Reserved bits in the range 0 to 17 must not be modified. Bits from 18 to 128 are not used. The default status of all fuses is not set.

Fuse Bit	Name	Description
0	ENCRNOTPLAIN	If it is set, Secure mode is active
1	READ_AES_KEY	If it is set, KEY_ENC and KEY_TAG cannot be read

...........continued		
Fuse Bit	**Name**	**Description**
2	WRITE_AES_KEY	If it is set, KEY_ENC and KEY_TAG can't be written
5	READ_CONTROL	If it is set, CONTROL_FUSES can't be read
6	WRITE_CONTROL	If it is set, CONTROL_FUSES can't be written
7	READ_RAM	If it is set, memory ram can't be read
8	RESERVED	Reserved
9	RESERVED	Reserved
10	FORCE_IVNBINC	If it is set, initialization vector and number of blocks must be used in the calculation of the signature
11	RESERVED	Reserved
12	RESERVED	Reserved
13	RESERVED	Reserved
14	RESERVED	Reserved
15	RESERVED	Reserved
16	DBG_DISABLE	If it is set, JTAG debug is disabled
17	DBG_DISABLE_SE	Reserved

7.4.7 Decryption

After writing the full encrypted binary in the program RAM, decryption of the program is launched. There are two options depending on the content of the encrypted program, which has been loaded.

If the KEY_TAG includes only the program, basic decryption is required (CMD=0x0013).

If the KEY_TAG includes the program plus initial vector and total number of packets, decryption plus is required (CMD=0x0015).

In both cases, neither address nor data are considered.

If FORCE_IVNBINC fuse is set to '1', both decryption commands (CMD=0x0013 and CMD=0x0015) will calculate the signature over SOFT+IV+NB.

7.4.8 Examples

7.4.8.1 Write a Non-encrypted Program

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_0001_DDDDDDDD…	Write the program at consecutive addresses from 0x00000000
0x00000000_0002_XXXXXXXX…	(Optional) Read the program to validate it (READ_RAM fuse must be not set)
0x400E1800_0000_00000000	Clear CPUWAIT to start program operation
0x00000000_A66A_00000000	Give control of the MISO signal to M7-SPI and disable bootloader clock

7.4.8.2 Write an Encrypted Program when Keys are already Written

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_0004_0000XXXX	Set the number of blocks of the encrypted program
0x00000000_0005_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Set the initialization vector of the encrypted program
0x00000000_0006_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Set signature of the encrypted program
0x00000000_0001_EEEEEEEE…	Write the program at consecutive addresses from 0x00000000
0x00000000_0013_00000000	Launch code decryption
0x00000000_0012_00000000	Check bootloader status to know if decrypt process has finished. Answers: • 0x"Bootloader Hardware signature"_0000_ 00000002 (aes_active) • 0x"Bootloader Hardware signature"_0000_ 00000000 (bootloader ready)
0x00000000_0002_XXXXXXXX…	(Optional) Read the decrypted program to validate it (READ_RAM fuse must not be set)
0x400E1800_0000_00000000	Clear CPUWAIT to start program operation
0x00000000_A66A_00000000	Give control of the MISO signal to M7-SPI and disable bootloader clock

7.4.8.3 Write Decryption Keys, or Control Bits, in the Fuse Boxes

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_0007_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Write the decryption key KEY_ENC in the Buffer register
0x00000000_0008_00000000	Write the Buffer register to the Tamper register for KEY_ENC_FUSES
0x00000000_000C_00000000	Blow fuses at corresponding fuse box
0x00000000_0012_00000000	Check bootloader status to see if the process of blowing fuses has finished. Answers: • 0x"Bootloader Hardware signature"_0000_ 00000001 (fuse blowing active) • 0x"Bootloader Hardware signature"_0000_ 00000000 (bootloader ready)
0x00000000_0007_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Write the signature/authentication key KEY_TAG in the Buffer register
0x00000000_0009_00000000	Write the Buffer register to the Tamper register for KEY_TAG_FUSES
0x00000000_000C_00000000	Blow fuses at corresponding fuse box

...........continued

Command	Description
0x00000000_0012_00000000	Check bootloader status to see if the process of blowing fuses has finished. Answers: • 0x"Bootloader Hardware signature"_0000_ 00000001 (fuse blowing active) • 0x"Bootloader Hardware signature"_0000_ 00000000 (bootloader ready)
0x00000000_0007_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Write the signature/authentication key KEY_TAG in the Buffer register
0x00000000_000B_00000000	Write the Buffer register to the Tamper register for CONTROL_FUSES
0x00000000_000C_00000000	Blow fuses at corresponding fuse box
0x00000000_0012_00000000	Check bootloader status to see if the process of blowing fuses has finished. Answers: • 0x"Bootloader Hardware signature"_0000_ 00000001 (fuse blowing active) • 0x"Bootloader Hardware signature"_0000_ 00000000 (bootloader ready)
0x00000000_0010_00000000	Read CONTROL_FUSES fuse value to its Tamper register to load the new value in the system

7.4.8.4 Read Decryption Keys, or Control Bits, from the Fuse Boxes

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_000D_00000000	Read fuse box values for KEY_ENC and write them to the corresponding Tamper register
0x00000000_0011_00000000 00000000 00000000 00000000	Read the Tamper register through the SPI
0x00000000_000E_00000000	Read fuse box values for KEY_TAG and write them to the corresponding Tamper register
0x00000000_0011_00000000 00000000 00000000 00000000	Read the Tamper register through the SPI
0x00000000_0010_00000000	Read fuse box values for CONTROL_FUSES and write them to the corresponding Tamper register
0x00000000_0011_00000000 00000000 00000000 00000000	Read the Tamper register through the SPI

8. Serial Peripheral Interface (SPI)

8.1 Description

The SPI circuit is a synchronous serial data link that provides communication with external devices in client mode. The Serial Peripheral Interface is essentially a Shift register that serially transmits data bits to a host SPI device. During a data transfer, SPI host controls the data flow, while the client device has data shifted in and out by the host.

The SPI system consists of two data lines and two control lines:

- MOSI (host out client in): This data line supplies the output data from the host shifted into the input(s) of the client(s)
- MISO (host in client out): This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer
- SCK (Serial Clock): This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SCK pulse for each bit that is transmitted
- CS (Peripheral Chip Select): This control line allows clients to be turned on and off by hardware

8.2 Embedded Characteristics

- Client Serial Peripheral Bus Interface
  - 8-bit to 16-bit data length
- Client Mode Operates on SCK, Asynchronously with Core and Bus Clock

8.3 Signal Description

The pins used for interfacing the compliant external devices are multiplexed with PIO lines.

Table 8-1. I/O Lines

Signal	Pin Description	Client	I/O Line
MISO	Host In Client Out	Output	F9
MOSI	Host Out Client In	Input	G9
CS	Peripheral Chip Select/Client Select	Input	G8
SCK	Serial Clock	Input	H9

8.4 Functional Description

8.4.1 Data Transfer

Four combinations of polarity and phase are available for data transfers. Consequently, a host/client pair must use the same parameter pair values to communicate.

The table below shows the four modes and corresponding parameter settings.

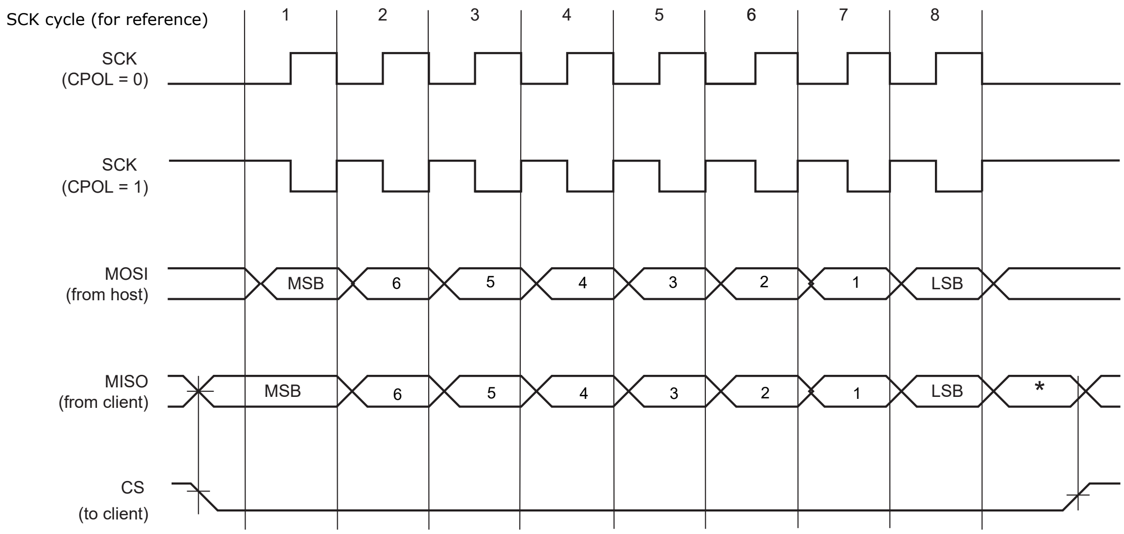
Table 8-2. SPI Bus Protocol Modes

SPI Mode	Shift SCK Edge	Capture SCK Edge	SCK Inactive Level
0	Falling	Rising	Low
1	Rising	Falling	Low

...........continued			
SPI Mode	**Shift SCK Edge**	**Capture SCK Edge**	**SCK Inactive Level**
2	Rising	Falling	High
3	Falling	Rising	High

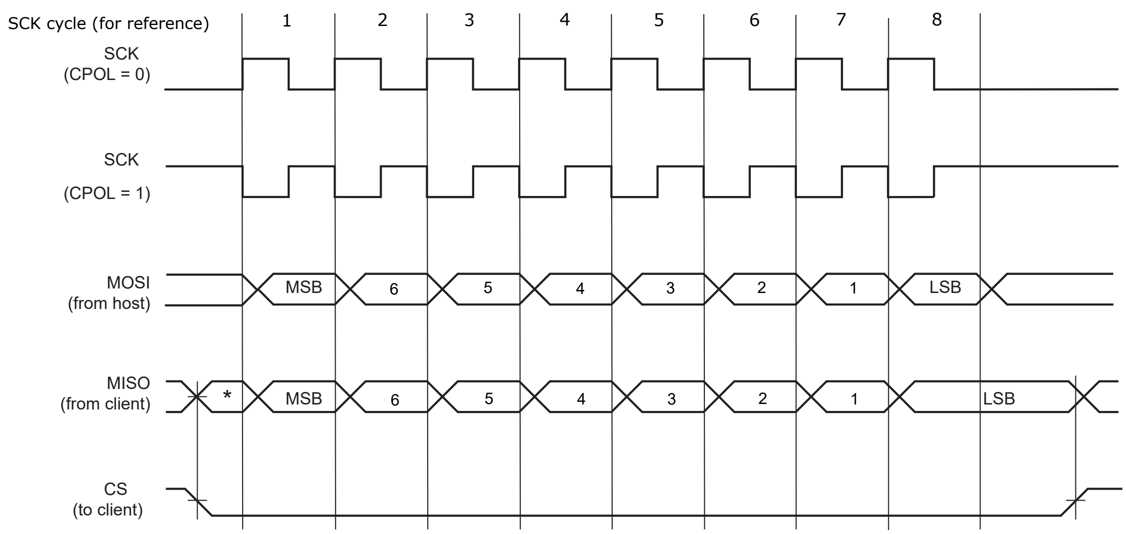
The figures below show examples of data transfers.

Figure 8-1. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)



* Not defined.

Figure 8-2. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



* Not defined.

8.4.2 SPI Client Mode

When operating in client mode, the SPI processes data bits on the clock provided on the SPI clock pin (SCK). The SPI waits until CS goes active before receiving the serial clock from an external host. When CS falls, the clock is validated and the data is loaded.

The bits are shifted out on the MISO line and sampled on the MOSI line.

When a transfer starts, the data shifted out is the data present in the internal Shift register. If no data has been written, the last data received is transferred. If no data has been received since the last reset, all bits are transmitted low, as the internal Shift register resets to 0.

When the first data is written, it is transferred immediately to the internal Shift register. If new data is written, it remains until a transfer occurs, i.e., CS falls and there is a valid clock on the SCK pin. When the transfer occurs, the last data written is transferred to the internal Shift register. This enables frequent updates of critical variables with single transfers.

If no character is ready to be transmitted, i.e., no character has been written since the last load to the internal Shift register, the last character is retransmitted.

8.4.3 SPI Typical Frequencies

Table 8-3. Typical Operating Frequency

Application case	Typical frequency
CENELEC A / CENELEC B	8 MHz
FCC (transmission band above 150 kHz)	12 MHz
Bootloader	12 MHz

9. Transmission Path

The transmission path adapts the digital data to generate a class-D amplified Pulse-Density Modulated (PDM) signal with high-current capability to drive low-impedance loads which are inherent to PLC systems. This output signal is externally band-pass filtered and coupled to the mains network.

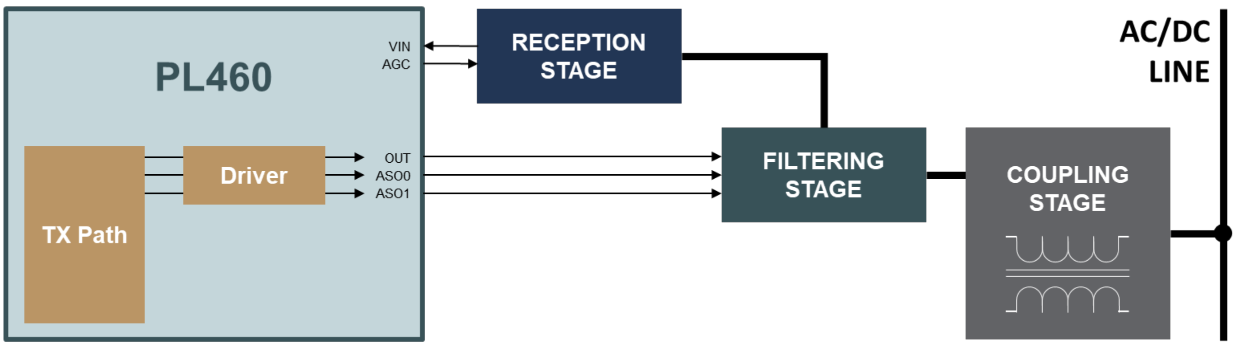
The PL460 supports up to two independent transmission branches described in the following sections.

9.1 Main Transmission Branch

The main transmission branch uses the embedded class-D PLC line driver to optimize performance in terms of efficiency and EMC compliance while reducing BOM cost and PCB complexity.

This is the default branch for single-band applications either in CEN-A, CEN-B or FCC bands.

Figure 9-1. Main Transmission Block Diagram



ASO0 and ASO1 pins manage the filtering stage associated with the Main Transmission Branch. The PL460 is capable of automatically managing up to two external filters in the filtering stage, each filter associated to an ASOx line. In case of requiring only one filter in the coupling, both ASO lines must be connected together externally.

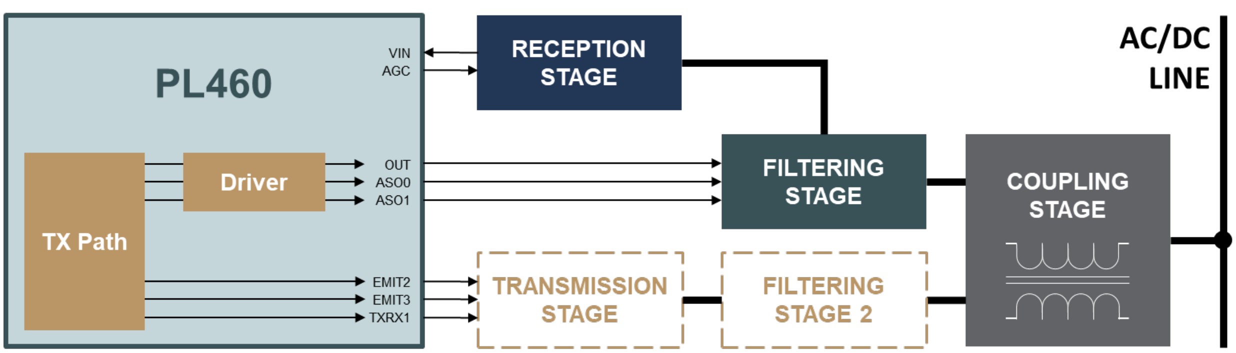
The ASIx pins indicate the status of the ASOx outputs, indicating whether the main branch is transmitting or not.

9.2 Auxiliary Transmission Branch

The Auxiliary Transmission Branch can provide an additional output bit-stream, if required. This PLC signal is driven by means of the EMIT outputs, and controlled by the TXRX1 signal, as described by Figure 9-2. Note that the auxiliary transmission path cannot use the embedded PLC driver in the PL460 and requires an external circuit for signal amplification, in addition to the standard filtering and coupling stages.

The auxiliary PLC transmission branch may be required in case of multi-band applications (for example, FCC+CEN-A).

Figure 9-2. Transmission Path Block Diagram using Auxiliary Branch

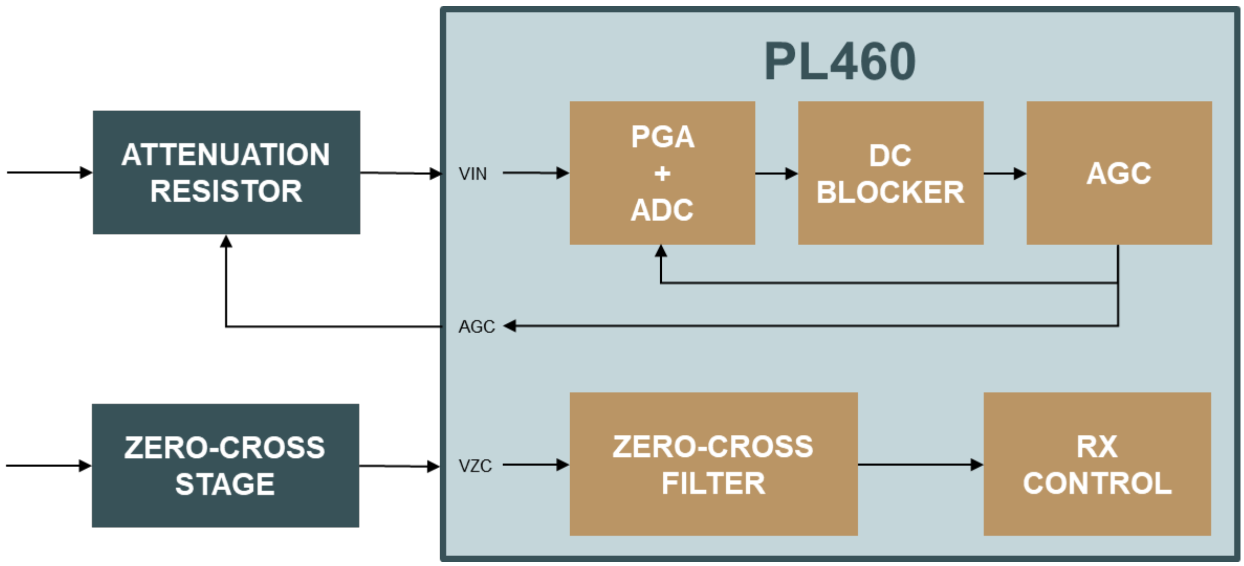


EMIT2 and EMIT3 provide a 3.3V PLC signal (not amplified) to the external transmission stage. TXRX1 is used to control the behavior of the external discrete filter in transmission and reception. Refer to Microchip reference designs for detailed descriptions about how to implement the external circuitry required by the auxiliary transmission branch.

10. Reception Path

The PL460 modem has a single-ended reception stage as it is shown in the figure below. It supports a maximum input of $24V_{pp}$ without saturation. The signal is adapted to the requirements of the Rx path by means of an Automatic Gain Control (AGC) and a Programmable Gain Amplifier (PGA) as it is described in 10.1.1. PLC Signal Adaptation. Additionally, the reception stage is also capable to detect zero-crosses (in case of being connected to an AC line) if an adapted signal is provided, as it is explained in 10.1.2. Zero-Crossing Detection.

Figure 10-1. PL460 Reception Path Block Diagram



10.1 Functional Description

10.1.1 PLC Signal Adaptation

The reception path implements several stages to adapt the received signal to avoid saturation of the Analog-to-Digital Converter (ADC) and maximize the dynamic range. The AGC stage uses an external resistor to attenuate the input signal if needed. The PL460 provides a control signal to configure the resistor dynamically in function of the level of signal measured.

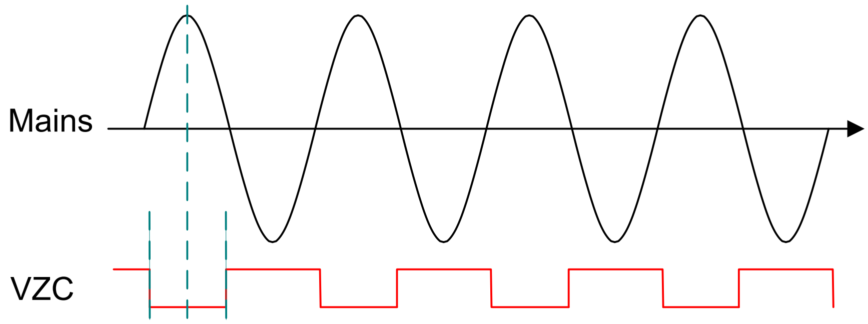
The PL460 also implements a PGA that adds five levels of gain to adjust the input signal to the ADC.

Finally, the DC blocker module is capable to detect and subtract any DC offset to prevent it from affecting the signal processing of the obtained samples.

10.1.2 Zero-Crossing Detection

The PL460 implements a zero-crossing detection stage. An external circuit is required to adapt the AC signal to VZC input requirements of the PL460. Once adapted, the zero-crossing detection stage measures rising and falling edges by hardware and then a PLL software algorithm is applied. The center of the low-level pulse input must be aligned with the peak of the mains wave, although some adjustment can be made on the application to correct the delay between pulse and wave.

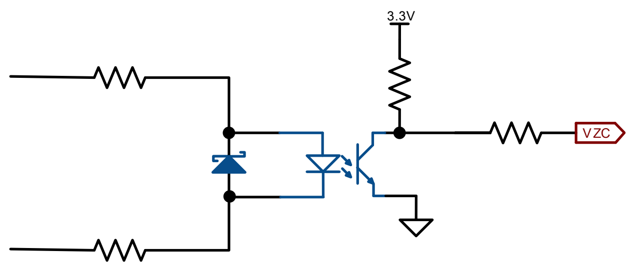
Figure 10-2. Zero-Crossing Signal



The achieved precision meets the standard requirements to track 50 Hz or 60 Hz ±10% mains.

A simple external circuit is required to adapt the mains signal to VZC input. A typical application circuit for unidirectional topologies is shown in the figure below.

Figure 10-3. Typical Circuit, Using a Unidirectional Optocoupler



11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Restricting the functional operation to the conditions given in the Recommended Operating Conditions section is recommended. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

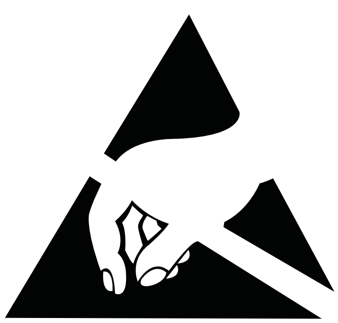
Table 11-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDDIO	-0.5 to 4.0	V
	VDDIN_AN		
	VDDIN		
	VDDAMP		
Input Voltage	VI	-0.5 to VDDIO +0.5 (≤ 4.0V)	
Output Voltage	VO	-0.5 to VDDIO +0.5 (<4.0V)	
Amplifier Supply Voltage	PVDDAMP	-0.5 to 20	V
Total current on ASO0 and ASO1 pads	I_{ASO}	1.2	A_{RMS}
Total current on OUT pads	I_{OUT}	1.5	A_{RMS}
Storage Temperature	T_{ST}	-55 to 125	ºC
Junction Temperature	T_J	-40 to 125	
Output Current(1)	IO	±8(2)	mA

Notes:

1. DC current that continuously flows for 10 ms or more, or average DC current
2. Applies to all the pins except OUT, ASO, EMIT and AGC pins. Using those pins only according to circuit configurations recommended by Microchip is recommended.

ATTENTION observe ESD precautions



Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection.

11.2 Recommended Operating Conditions

Table 11-2. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VDDIO	3.00	3.30	3.60	V
	VDDIN_AN	3.00	3.30	3.60	
	VDDIN	3.00	3.30	3.60	
	VDDPLL	1.15	1.25	1.32	
	VDDAMP	3.00	3.30	3.60	
	PVDDAMP	8.00	12.00[1]	16.00	
Voltage of Analog Switch Outputs	V_{ASO}	-15	—	15	V
Junction Temperature	T_J	-40	25	125	ºC
Ambient Temperature	T_A	-40	—	85	

Notes:

1. The PLC-protocol firmware provided by Microchip are configured by default for PVDDAMP = 12V.

Table 11-3. Thermal Resistance Data

Package	Symbol	Parameter	Condition	Typ	Unit
TFBGA81	θ_{JA}	Junction-to-Ambient Thermal Resistance	Still Air	38.75	ºC/W
	θ_{JC}	Junction-to-Case Thermal Resistance	—	12.9	

θ_{JA} is calculated based on a standard JEDEC JESD51-5 defined environment (1.6 mm thickness PCB, 4 copper layers, 76.2 mm x 114.3 mm board) and is not a reliable indicator of a device's thermal performance in a non-JEDEC environment. It is recommended that the customer always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

11.3 Electrical Pinout

Table 11-4. TFBGA81 Electrical Pinout

Pin No	Pin Name	I/O	I(mA)	Res	HY	Pin No	Pin Name	I/O	I(mA)	Res	HY
A1	GND	P	—	—	—	E6	NC	—	—	—	—
A2	TXRX1	I/O	±2/4	PU/PD/-	Y/-	E7	NC	—	—	—	—
A3	EMIT3	OT	±60[1]	—	—	E8	ASI1	I/O	±2/4	PU/PD/-	Y/-
A4	EMIT2	OT	±60[1]	—	—	E9	ASI0	I/O	±2/4	PU/PD/-	Y/-
A5	VREGP [6]	—	—	—	—	F1	VDDIN_AN	P	—	—	—
A6	PVDDAMP	P	—	—	—	F2	VREFP [6]	—	—	—	—
A7	OUT	O	±1500 [2]	—	—	F3	AGND	P	—	—	—
A8	ASO1	O	1200 [3]	—	—	F4	GND	P	—	—	—
A9	PGND	P	—	—	—	F5	VDDIO	P	—	—	—

...........continued											
Pin No	Pin Name	I/O	I(mA)	Res	HY	Pin No	Pin Name	I/O	I(mA)	Res	HY
B1	AGC	OT	±20 (4)	PU/-	—	F6	VDDIO	P	—	—	—
B2	GND	P	—	—	—	F7	THW1	I/O	±2/4	PU/PD/-	Y/-
B3	EMIT3	OT	±60(1)	—	—	F8	NTHW0	I/O	±2/4	PU/PD/-	Y/-
B4	EMIT2	OT	±60(1)	—	—	F9	MISO	I/O	±2/4	PU/PD/-	Y/-
B5	VREGN (6)	—	—	—	—	G1	VREFC (6)	—	—	—	—
B6	PVDDAMP	P	—	—	—	G2	VREFN (6)	—	—	—	—
B7	OUT	O	±1500 (2)	—	—	G3	NRST	I	—	—	Y
B8	ASO1	O	1200 (3)	—	—	G4	VDDIO	—	—	—	—
B9	PGND	P	—	—	—	G5	GND	—	—	—	—
C1	VDDCORE	P	—	—	—	G6	VDDIO	P	—	—	—
C2	VDDCORE	P	—	—	—	G7	G1	I/O	±2/4	PU/PD/-	Y/-
C3	GND	P	—	—	—	G8	CS	I/O	± 2/4	PU/PD/-	Y/-
C4	GND	P	—	—	—	G9	MOSI	I/O	± 2/4	PU/PD/-	Y/-
C5	GND	P	—	—	—	H1	VDDIN_AN	P	—	—	—
C6	GNDAMP	P	—	—	—	H2	STBY	I	—	—	Y
C7	VDDAMP	P	—	—	—	H3	XIN	I	—	—	—
C8	PGND	P	—	—	—	H4	GND	P	—	—	—
C9	ASO0	O	1200 (3)	—	—	H5	VDDCORE	P	—	—	—
D1	VDDIO	P	—	—	—	H6	VDDIN	P	—	—	—
D2	VDDIO	P	—	—	—	H7	THEN	I/O	±2/4	PU/PD/-	Y/-
D3	VDDIO	P	—	—	—	H8	EXTIN	I/O	± 2/4	PU/PD/-	Y/-
D4	GND	P	—	—	—	H9	SCK	I/O	± 2/4	PU/PD/-	Y/-
D5	GND	P	—	—	—	J1	GND	P	—	—	—
D6	NC	—	—	—	—	J2	VZC	I	—	(5)	Y
D7	GND	P	—	—	—	J3	XOUT	O	—	—	—
D8	VDDAMP	P	—	—	—	J4	VDDPLL	P	—	—	—
D9	ASO0	O	1200 (3)	—	—	J5	VDDCORE	P	—	—	—
E1	VIN	I	—	—	—	J6	VDDIN	—	—	—	—
E2	AGND	P	—	—	—	J7	ENABLE	I	—	—	Y
E3	GND	P	—	—	—	J8	TXEN	I/O	±2/4	PU/PD/-	Y/-
E4	VDDIO	P	—	—	—	J9	GND	P	—	—	—
E5	NC	—	—	—	—	—	—	—	—	—	—

I/O = pin direction (I = input, O = output, T = tri-state, P = power)

I(mA) = nominal current (+ = source, - = sink)

Res = pin pull-up/pull-down resistor (PU = pull up, PD = pull down (70-140 kΩ, typical 100 kΩ))

HY = Input Hysteresis (Y = yes)

Notes:
1. Maximum value considering the use of both balls per EMITx
2. Maximum value considering the use of both balls of OUT
3. Maximum value considering the use of both balls per ASOx
4. Selectable from 5 mA to 20 mA in 4 steps of 5 mA
5. In case of fuse programming, an external 10 kΩ serial resistor is needed (see 7.4.5. Fuse Programming).
6. VREGP, VREGN, VREFP, VREFC and VREFN are analog signals.

11.4 DC Characteristics

Table 11-5. PL460 DC Characteristics

Parameter	Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Supply Voltage		VDDIO	3.00	3.30	3.60	V
H-level Input Voltage (3.3V CMOS)		VIH	2.0	—	VDDIO +0.3	
L-level Input Voltage (3.3V CMOS)		VIL	-0.3	—	0.8	
H-level Output Voltage	3.3V I/O IOH = -100 µA	VOH	VDDIO -0.2	—	VDDIO	
L-level Output Voltage	3.3V I/O IOL = 100 µA	VOL	0	—	0.2	
Internal Pull Up Resistor(1)	3.3V I/O	Rpu	70	100	140	kΩ
Internal Pull Down Resistor(1)	3.3V I/O	Rpd	70	100	140	

Note:
1. Only applicable to pins with internal pulling

11.5 Power Consumption

The table below shows power consumption of the system (digital and analog) when it is used with typical AMR protocols. However, it is important to remember that different protocols, or even the same protocols used with different clock schemes or with different software implementations, can lead to other consumption figures.

Table 11-6. Full System Power Consumption

Frequency band	Application Case	Rating		Unit
		3V3	12V	
		Typ(1)	Typ(1)	
CENELEC-A CENELEC-B	Reception waiting for preamble detection	34	0.6	mA
	Reception processing incoming frames	45	0.6	
	Transmission with internal driver	46	104	
FCC	Reception waiting for preamble detection	65	0.6	
	Reception processing incoming frames	87	0.6	
	Transmission with internal driver	91	166	

Notes:

1. T_{AMB} = 25ºC, VDDIO = 3.3V, VDDIN = 3.3V and VDDIN_AN = 3.3V, G3-PLC

The table below shows power consumption of the analog IPs in the system. Analog parts are the PLL used for internal clock generation (supplied from VDDPLL pin) and the conversion module composed of the Programmable Gain Amplifier (PGA) and the Analog-to-Digital Converter (ADC), both supplied from VDDIN_AN pins.

Take maximum consumption cases into account for supply filter calculation. The supply voltage drop after the filters must be small enough to ensure the correct operation of the analog IPs. Voltage applied to VDDPLL and VDDIN_AN must always be greater than Vtypical-10%, VDDPLL > 1.08V and VDDIN_AN > 3.0V.

Table 11-7. Analog Power Consumption

Supply	Block	Application Case	Rating			Unit
			Min	Typ	Max	
VDDPLL	**PLL**	—	—	1.7[1]	2.1[2]	mA
VDDIN_AN	**PGA**	—	—	1.5[3]	2.2[4]	
	ADC	CENELEC-A / CENELEC-B	—	7.5[3]	10.8[4]	
		FCC	—	14.4[3]	20.9[4]	

Notes:

1. Typical case conditions: freq = 216 MHz, T_{AMB} = 25ºC, VDDPLL = 1.2V
2. Worst case conditions: freq = 216 MHz, T_{AMB} = 125ºC, VDDPLL = 1.32V
3. Typical case conditions: T_J = 25ºC, VDDIN_AN = 3.3V
4. Worst case conditions: T_J = 125ºC, VDDIN_AN = 3.6V

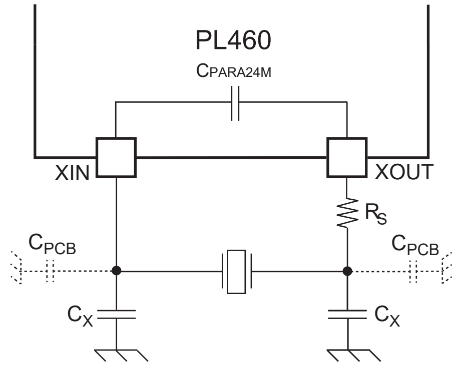
11.6 Crystal Oscillator

Table 11-8. 24 MHz Crystal Oscillator Characteristics

Parameter	Test Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Crystal Oscillator frequency	Fundamental	X_{tal}	24			MHz
Internal parasitic capacitance	Between XIN and XOUT	$C_{PARA24M}$	0.6	0.7	0.8	pF
Start-up time		t_{ON}	—	—	1	ms
Drive level		P_{ON}	—	—	400	µW
Load capacitance		C_{LOAD}	4	—	18	pF

Important: Locate the crystal as close as possible to the XOUT and XIN pins.

Figure 11-1. 24 MHz Crystal Oscillator Schematic



$$C_X = 2 \times (C_{XTAL} - C_{PARA24M} - C_{PCB}/2)$$

Where C_{XTAL} is the load capacitance of the crystal, $C_{PARA24M}$ is the internal parasitic impedance of the oscillator, typically 0.7pF and C_{PCB} is the ground-referenced parasitic capacitance of the printed circuit board (PCB) on XIN and XOUT tracks.

Table 11-9 summarizes recommendations to be followed when choosing a crystal.

The drive level indicates power consumption by the crystal unit while the oscillation circuit works. Excessive drive level might cause unexpected change of frequency, crystal damage or shorter device lifetime. The drive level is given by the following formula:

$$Drive\ Level = ESR \times I^2$$

Where:

- ESR is the equivalent series resistor (specified by the crystal manufacturer).
- I is the current flowing through the crystal in RMS. If the waveform is sine wave or similar, the effective value is calculated by Ip-p/2√2.

To keep the drive level value inside the manufacturer range, it is required to limit the current that flows through the crystal. The total power dissipated by the crystal is proportional to R_S (see Figure 11-1), so its value can be modified to obtain a drive level that complies with the requirements. As the value of R_S also relates to the safety factor, there is a maximum value of R_S that maintains a good safety factor and at the same time keeps the drive level below the crystal manufacturer maximum specifications.

Table 11-9. Recommended Crystal Characteristics

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Equivalent Series Resistor	ESR	—	—	100	Ω
Motional capacitance	C_M	2	—	3.2	fF
Shunt capacitance	C_{SHUNT}	—	—	1.3	pF
Frequency tolerance	—	—	10[1]	25	ppm

Notes:

1. As a requirement of the G3-PLC specification, the System Clock tolerance shall be ±25 ppm maximum. In the case of PRIME specification, it shall be ±50 ppm maximum. In both cases, Microchip recommends choosing a crystal with a frequency tolerance below the specification requirement because it is dependent on production tolerance, temperature stability and age.

11.7 PGA and ADC

Table 11-10. PL460 PGA and ADC Input Characteristics

Parameter	Typical Value	Unit
VIN input impedance	10	kΩ
VIN max voltage dynamic range	± 0.75	V

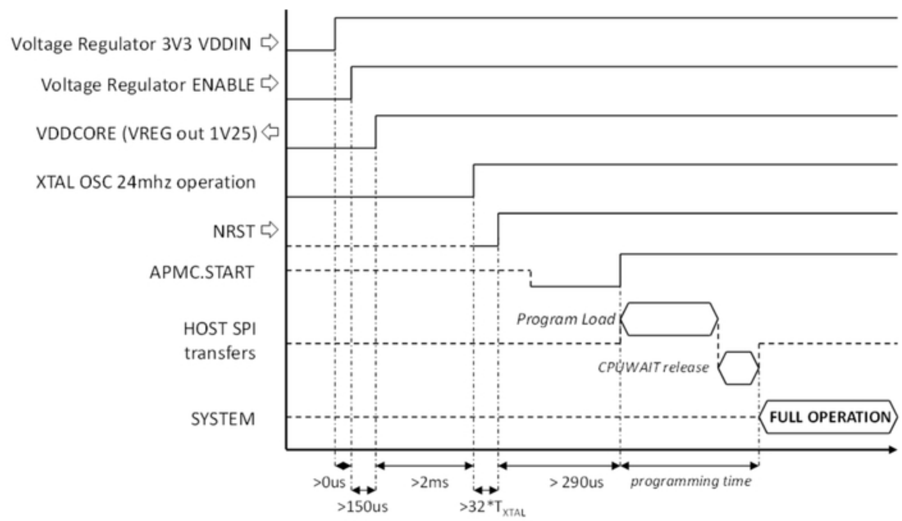
Note: Although the maximum VIN range is 0 - 3.3V, the PGA has been designed to saturate with any input value greater than the input common mode voltage (VREFC) ± 0.75V. To clamp the input signal, a pair of series diodes can be used to easily achieve it.

11.8 Power On Considerations

The Power On procedure starts after enabling the embedded voltage regulator. It is mandatory to wait for a stable 3V3 supply input to the voltage regulator before enabling it.

The crystal oscillator starts automatically after VDDCORE is stable; it takes a maximum of 2 ms to get stable operation. The NRST pin must be tied to '0' during crystal oscillation startup, and it must be released to '1' after at least 32 X_{tal} clock periods. The clock signals will start operation ≈290 µs after NRST release. Then the external host CPU will access Bootloader logic to transfer the program and release the system for operation.

Figure 11-2. Power On Timing Diagram



Timing between ENABLE active and NRST release must always be greater than {150µs + 2ms + $32Tx_{tal}$} as shown in the previous figure.

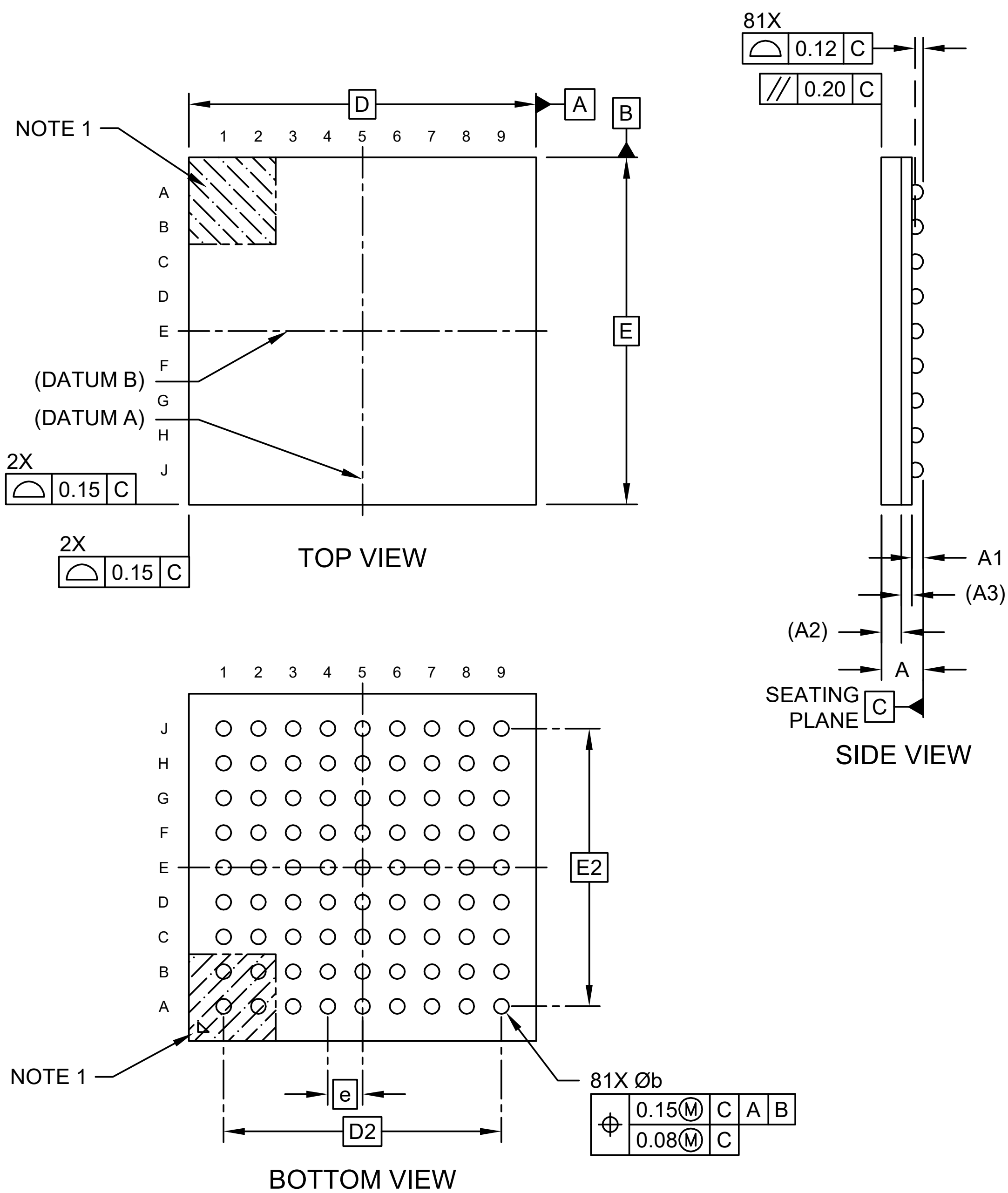
Although no special power-up sequence is required between high-voltage PVDDAMP power domain and low-voltage domain (VDDIO, VDDIN and VDDAMP), it is recommended to satisfy the ramp-up slopes defined in Table 5-2.

12. Mechanical Characteristics

12.1 81-Ball TFBGA

81-Ball Thin Fine-Pitch Ball Grid Array Package (4LB) - 10x10x1.2 mm Body [TFBGA]

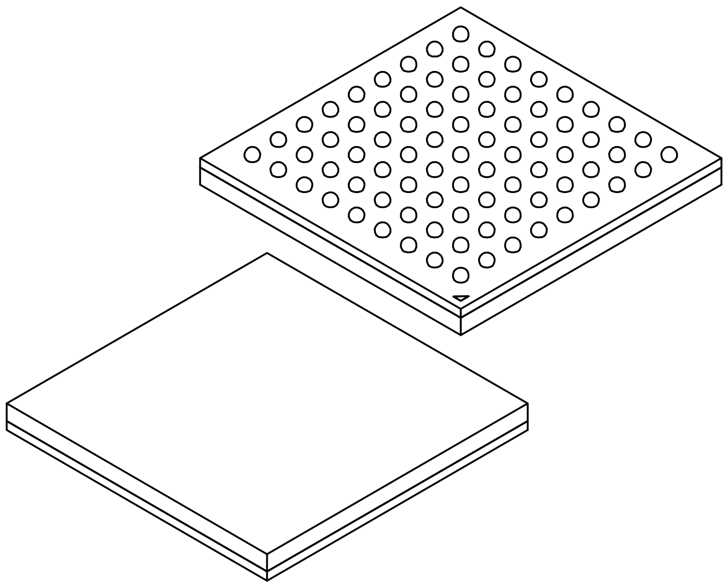
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21526 Rev A Sheet 1 of 2

81-Ball Thin Fine-Pitch Ball Grid Array Package (4LB) - 10x10x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		81	
Pitch	e		1.00 BSC	
Overall Height	A	–	–	1.20
Ball Height	A1	0.27	0.32	0.37
Mold Thickness	A2		0.53 REF	
Substrate Thickness	A3		0.26 REF	
Overall Length	D		10.00 BSC	
Ball Array Length	D2		8.00 BSC	
Overall Width	E		10.00 BSC	
Ball Array Width	E2		8.00 BSC	
Ball Diameter	b	0.38	0.40	0.48

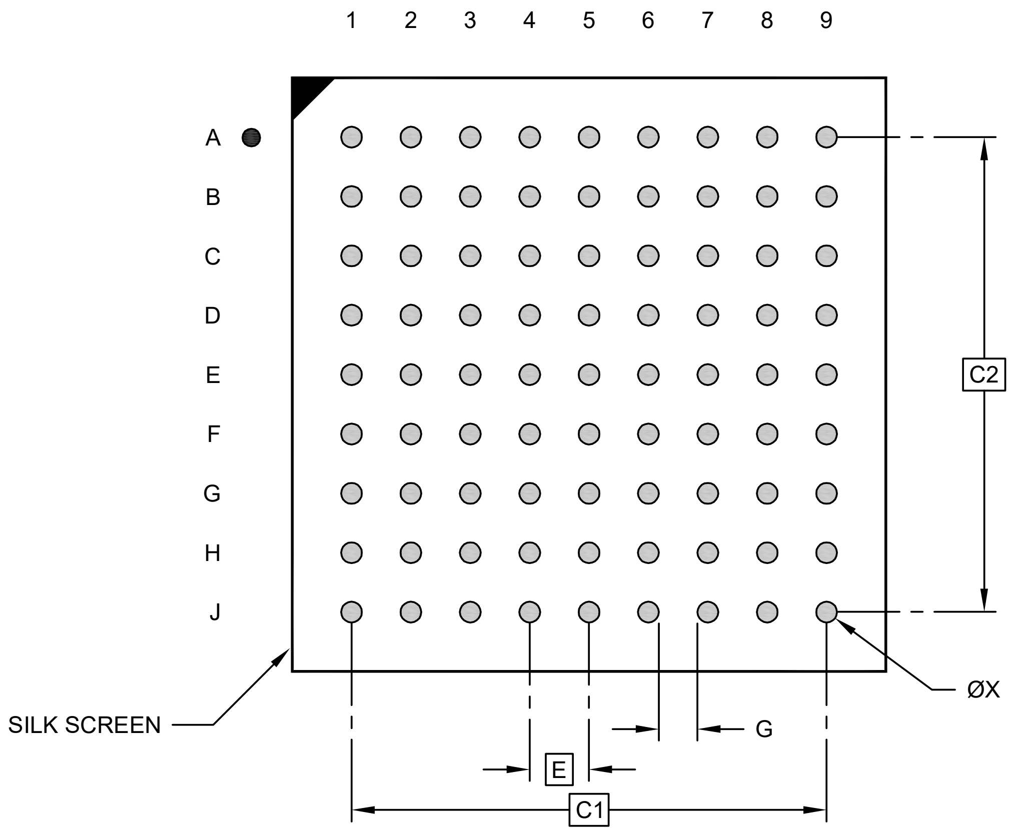
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21526 Rev A Sheet 2 of 2

81-Ball Thin Fine-Pitch Ball Grid Array Package (4LB) - 10x10x1.2 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.00 BSC	
Contact Pad Spacing	C1		8.00 BSC	
Contact Pad Spacing	C2		8.00 BSC	
Contact Pad Width (X81)	X			0.35
Contact Pad to Contact Pad	G	0.65		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23526 Rev A

Table 12-1. 81-Ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 12-2. Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

13. Recommended Mounting Conditions

Refer to application note AN233 on the Microchip website for more information.

14. Marking

All devices are marked with the Microchip logo and the ordering code.

Figure 14-1. TFBGA Marking

Where:

- M: Microchip logo
- MPL460A: Product name
- e8: Jedec code
- YYWWNNN: Traceability code
- ARM: ARM logo

15. Ordering Information

Table 15-1. Ordering Information

Ordering Code	Package	Carrier Type	Package Type	Temperature Range
MPL460A-I/4LB	81 TFBGA	Tray	Pb-Free	Industrial (-40ºC to 85ºC)
MPL460AT-I/4LB	81 TFBGA	Tape and Reel	Pb-Free	Industrial (-40ºC to 85ºC)

16. Revision History

16.1 Rev A – 10/2020

Document	Initial release.

16.2 Rev B – 10/2022

Document	Terminology replaced. The SPI standard uses the terminology "master" and "slave". The equivalent Microchip terminology used in this document is "host" and "client" respectively.
1. Typical Application of PL460	Pins of Thermal Monitor functionality included
2. Block Diagram	Pins of Thermal Monitor functionality included
3. Signal Description	• External pull-down for NRST • TXEN added • Pins of Thermal Monitor functionality included • Recommendations about coupling capacitors modified
4. Package and Ballout	In 4.2. Ballout: • TXEN added • Pins of Thermal Monitor functionality included In 4.3. Pinout Specification: • ASIx added • TXEN added • Pins of Thermal Monitor functionality included
5. Power Considerations	Recommendations about PVDDAMP included in 5.2. Power Constraints
6. Input/Output Lines	• Added descriptions for NRST, STBY, TXEN and Thermal Monitor Pins
11. Electrical Characteristics	• Added Thermal Resistance Data in 11.2. Recommended Operating Conditions • Added information about Thermal Monitor, TXEN and ASIx pins in 11.3. Electrical Pinout • Added 11.5. Power Consumption chapter • Added recommendations about crystal selection in 11.6. Crystal Oscillator

16.3 Rev C – 02/2023

3. Signal Description	Added recommendations about host controller driving configuration for NRST and STBY pins
6. Input/Output Lines	Added details about how to enable Sleep mode

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