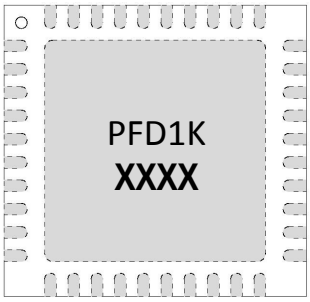
8 GHz Phase Frequency Detector IC with Dual 40 GHz Prescalers

Features

- Product Highlights
- 40 GHz Maximum Frequency
- 1-127 Variable Modulus Prescalers
- DC-8GHz Phase Detector Operation
- Single +3.3V Supply
- Single-Ended or Differential inputs and outputs
- Charge Pump digital control
- Charge Pump invert pin
- 6x6 Ceramic Leadless QFN
- Low Power Dissipation



Application

The PFD1K can be used as a general purpose phase frequency detector with integrated prescalers. It is ideally suited to phase locked loop applications. The prescalers can be programmed at a rate greater than 100MHz, which makes it an excellent choice for fractional-N digital frequency synthesizers.

Pad Metallization

The QFN package pad metallization consists of a 500-1000 micro-inch Sn63 automated solder dip process.

Description

The PFD1K is a high frequency phase frequency detector with fully differential inputs and outputs. It features dual 7 bit programmable high speed prescalers which allow the PFD1K to operate up to 40 GHz for the reference and voltage controlled oscillator input frequency. The 8 GHz phase-frequency detector allows operation at higher reference frequencies with concurrent lower phase noise and PLL figure of merit. The PFD1K operates with a single positive or negative 3.3V supply, and is packaged in a 40-pin, 6mm x 6mm ceramic leadless surface mount package.

Order Information

Part Number	Description
PFD1K	Piece Part
PFD1KE	Evaluation Board

Key Specifications (T = 25˚C)

Vcc=+3.3V, Zo=50Ω

Parameter	Description	Min	Typ	Max
Fref (GHz)	Input Reference Frequency[1]	0.01	-	40
Fvco (GHz)	Input VCO Frequency[1]	0.01	-	40
Pref (dBm)	Input Reference Power[2]	-10	0	+10
Pvco (dBm)	Input VCO Power[2]	-10	0	+10
Vout (mVp-p)	Differential Charge Pump Output[3]	-	400	-
PDC (mW)	DC Power Dissipation	-	1320	-
$\mathcal{L}$ (dBc/Hz)	SSB Phase Noise[4]	-	-153	-

[1] Minimum input frequency values assume sine wave input and divide ratio set to 1.
[2] Input frequency=20 GHz
[3] Each side terminated into 50Ω
[4] 900 MHz PFD input; 10 KHz offset

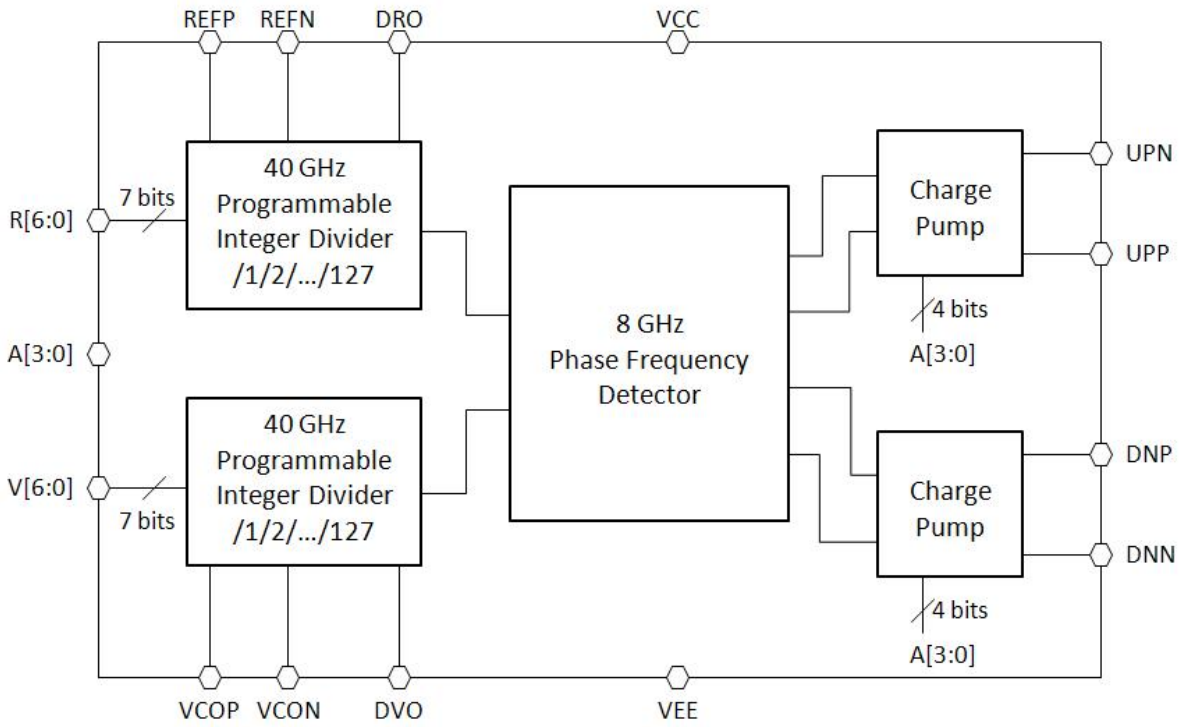
Supplemental Characteristics (@ 25˚C):

Vcc=+3.3V, Pin = 0 dBm, Zo=50Ω

Parameter	Description	Min	Typ	Max
Vdro (mVp-p)	Reference Prescaler Output[1]	450	475	500
Vdvo (mVp-p)	VCO Prescaler Output[1]	450	475	500

[1] Measured over several frequencies and divide ratios.

Theory of Operation



Functional Block Diagram

Overview:

The functional block diagram for the PFD1K is shown above. It contains two parallel programmable prescalers which frequency divide the reference and VCO inputs to the phase frequency detector. Reference input divide ratio R is determined as follows:

$$R = R6 * 26 + R5 * 25 + R4 * 24 + R3 * 23 + R2 * 22 + R1 * 21 + R0 * 20$$

where R6 thru R0 have values of 0 or 1. (All bits set to 0 results in a divide ratio of 1). Similarly, the divide ratio for the VCO input is set by V6 thru V0.

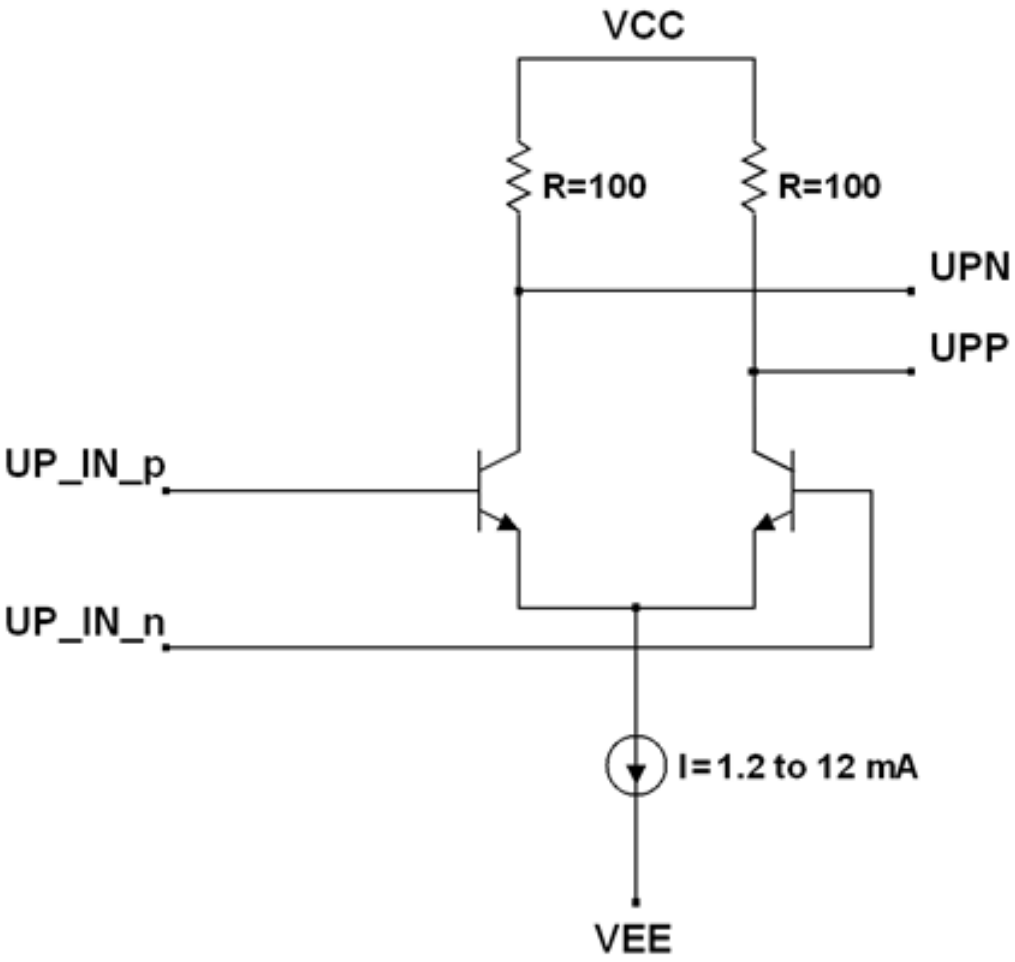
The core phase frequency detector can be operated up to a reference frequency of 8 GHz. The output of the phase frequency detector drives two programmable charge pumps. The amplitudes of the UP and Down pulses from the charge pumps can be controlled digitally by setting A[3:0]. There is also an analog adjustment at the VADJ* pin.

The divided reference and VCO signals may be monitored at the DRO and DVO outputs respectively. Analog adjustments, VADV* and VADR* can be used to control the amplitudes of DVO and DRO, or to disable DVO and DRO in order to reduce power consumption. With the exception of DRO and DVO, all of the RF inputs and outputs of the PFD1K are fully differential CML compatible levels so that they are easy to interface with other logic.

** VADJ, VADV and VADR are not shown in the block diagram.*

Charge Pump Control:

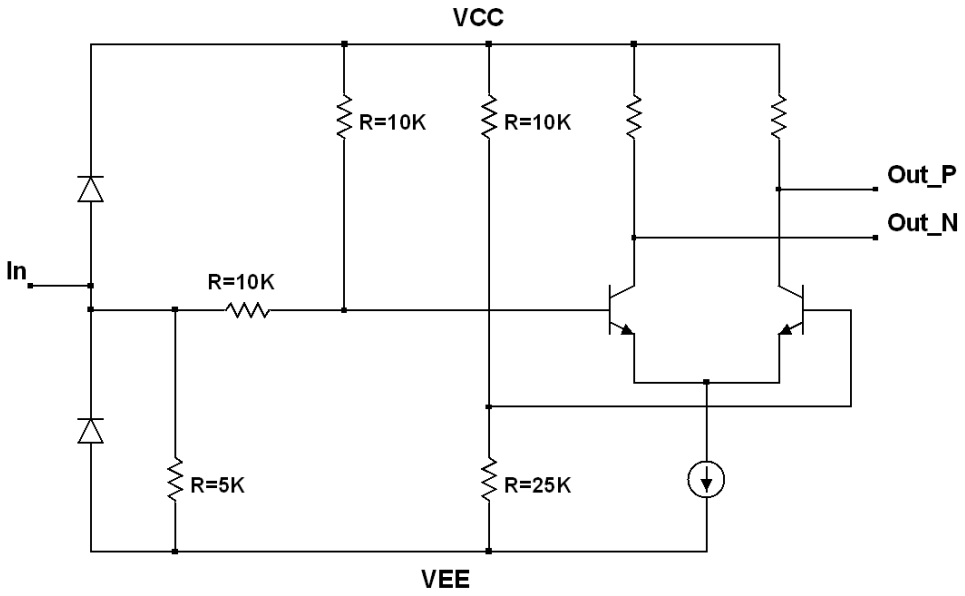
The PFD1K charge pump outputs are differential CML outputs with 100 ohm terminations. With this design the charge pump pulse width can be as small as 100 ps. The charge pump output pulses are digitally programmable with a 4 bit parallel interface. The maximum current output of the charge pump is 12 mA which will produce a pulse of 1200 mVpp into the internal 100 ohm termination resistor. When the charge pump outputs are terminated with a 50ohm load the parallel impedance of 100 ohms and 50 ohms results in a 33 ohm load, which reduces the output to 400mVpp. In addition to the digital control, there is an analog charge pump control voltage, VADJ, which can be used for fine control of the charge pump current. The maximum charge pump output of 12mA occurs when VADJ is set to VCC (which is the normal mode of operation). Logic 1 on the POL control input reverses the polarity of the charge pump outputs.



Simplified Charge Pump Output Circuit

Control Logic Circuitry:

The same circuitry is used for all control lines: A[0:3], R[0:6], V[0:6] and POL. A control pin left open defaults to logic 0.



Simplified Control Logic Input

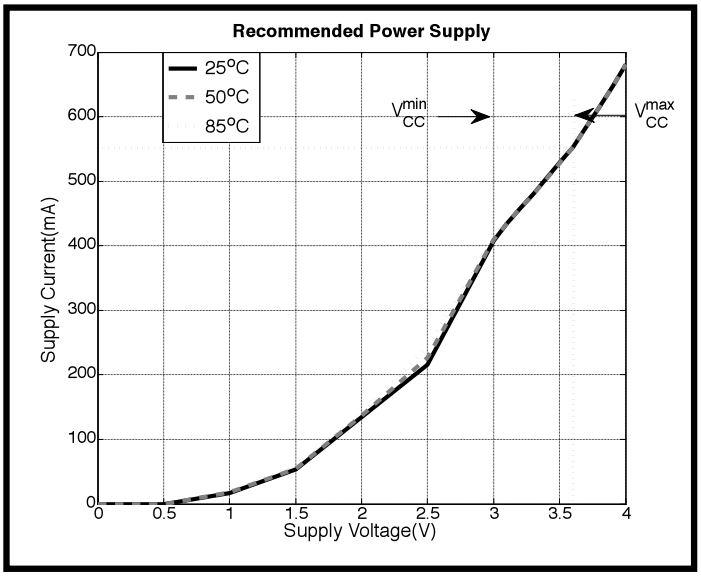
Table 1: Control Voltages (LVTTL Compatible)

Logic Level	Minimum	Typical	Maximum
1 (High)	VCC-1.3 V	VCC	VCC
0 (Low)	VEE	VEE	VEE+0.8 V

Analog Amplitude Controls:

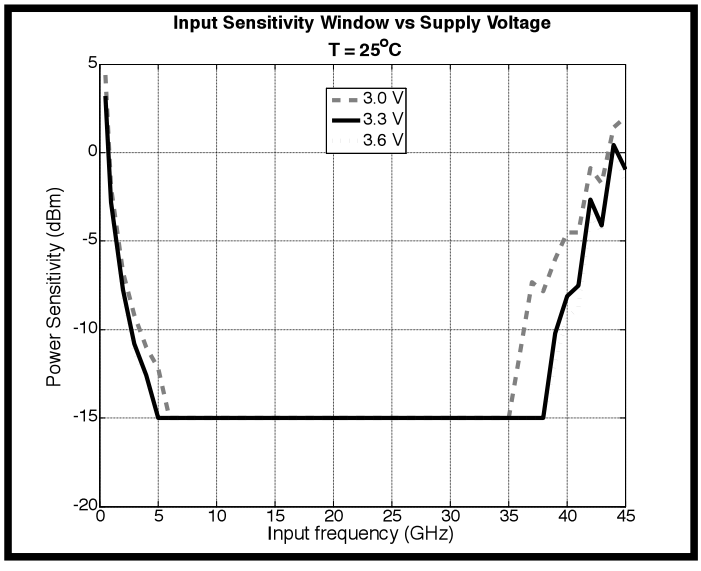
As was previously mentioned, VADJ can be used for fine tuning the charge pump current. Maximum current is achieved by setting VADJ to VCC. Similarly, the amplitudes of the prescaler outputs at DRO and DVO can be controlled with analog voltages VADR and VADV, respectively. As with VADJ, setting VADR and VADV to VCC results in maximum output amplitude.

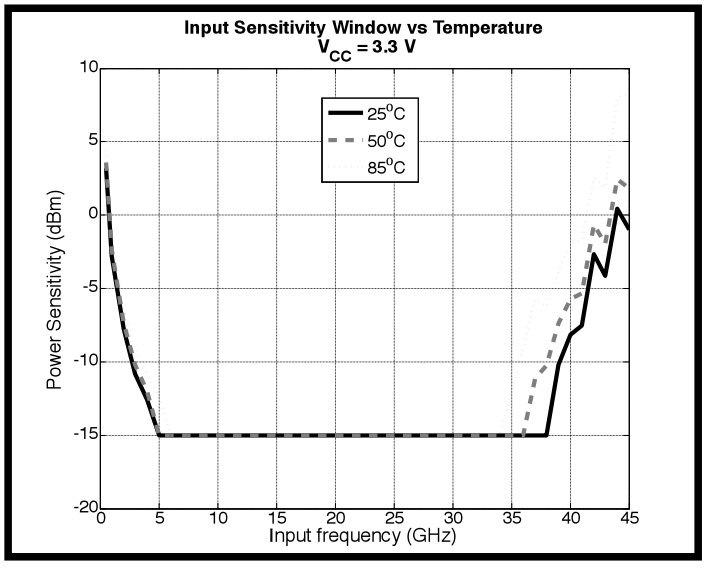
Power Supply Current



Power Supply Current

Prescaler Characteristics

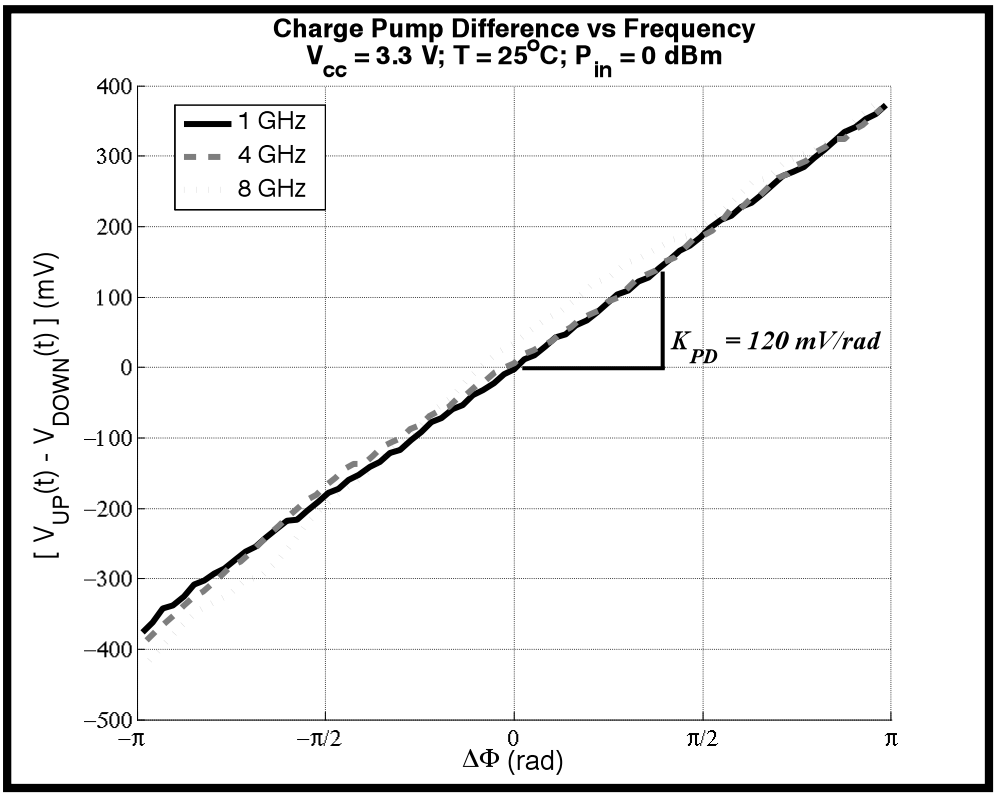


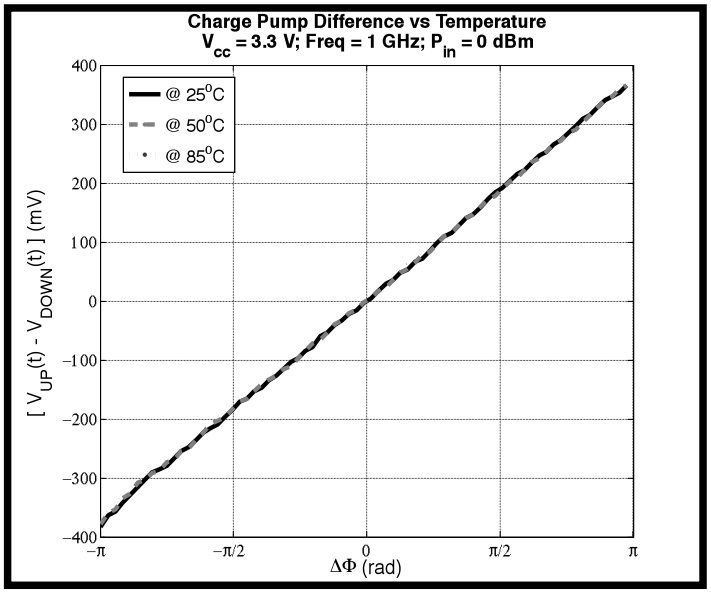


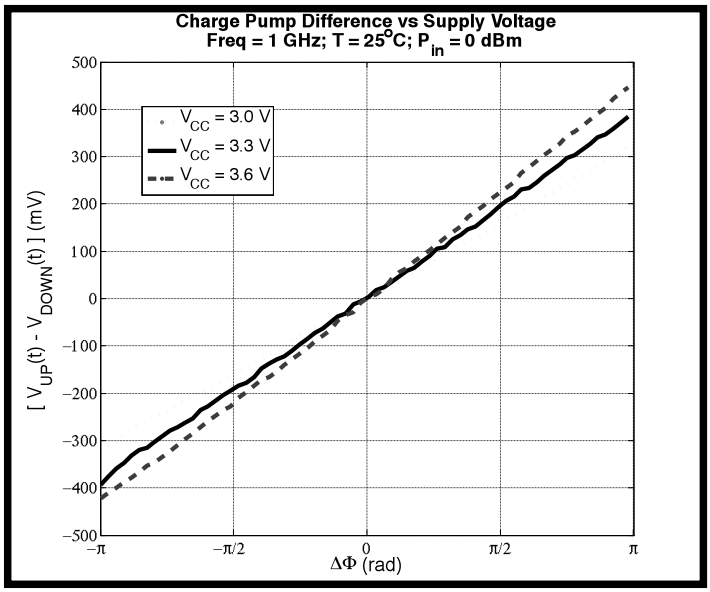
Prescaler Input Sensitivity

Phase Detector Characteristics

Divide Ratios: R = V = 1



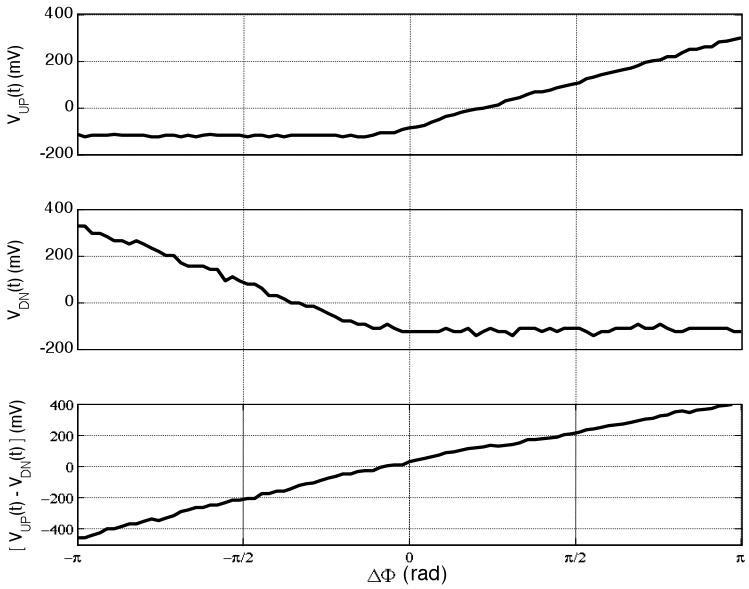




Phase Detector Characteristics

REF leads VCO

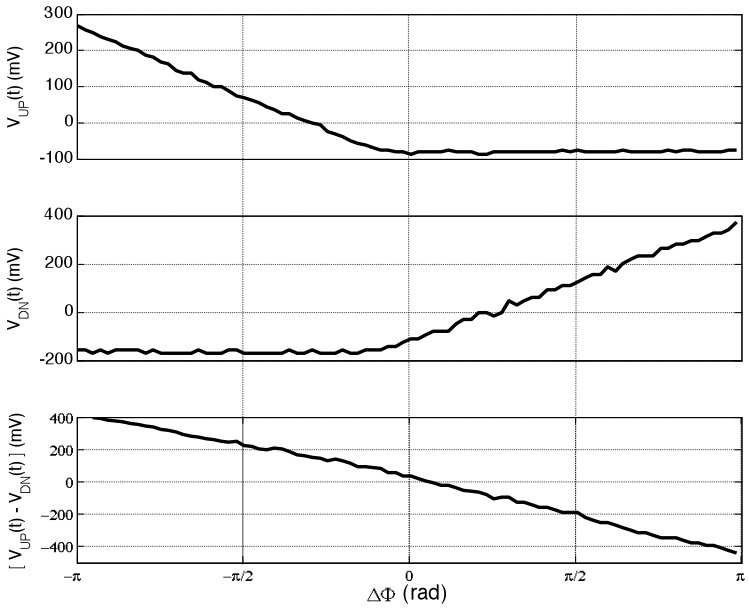
$f_{REF} > f_{VCO}$; f_{REF} = 5 GHz; V_{CC} = 3.3 V; T = 25oC; P_{in} = 0 dBm; POL = open



Charge pump outputs for REF leading VCO

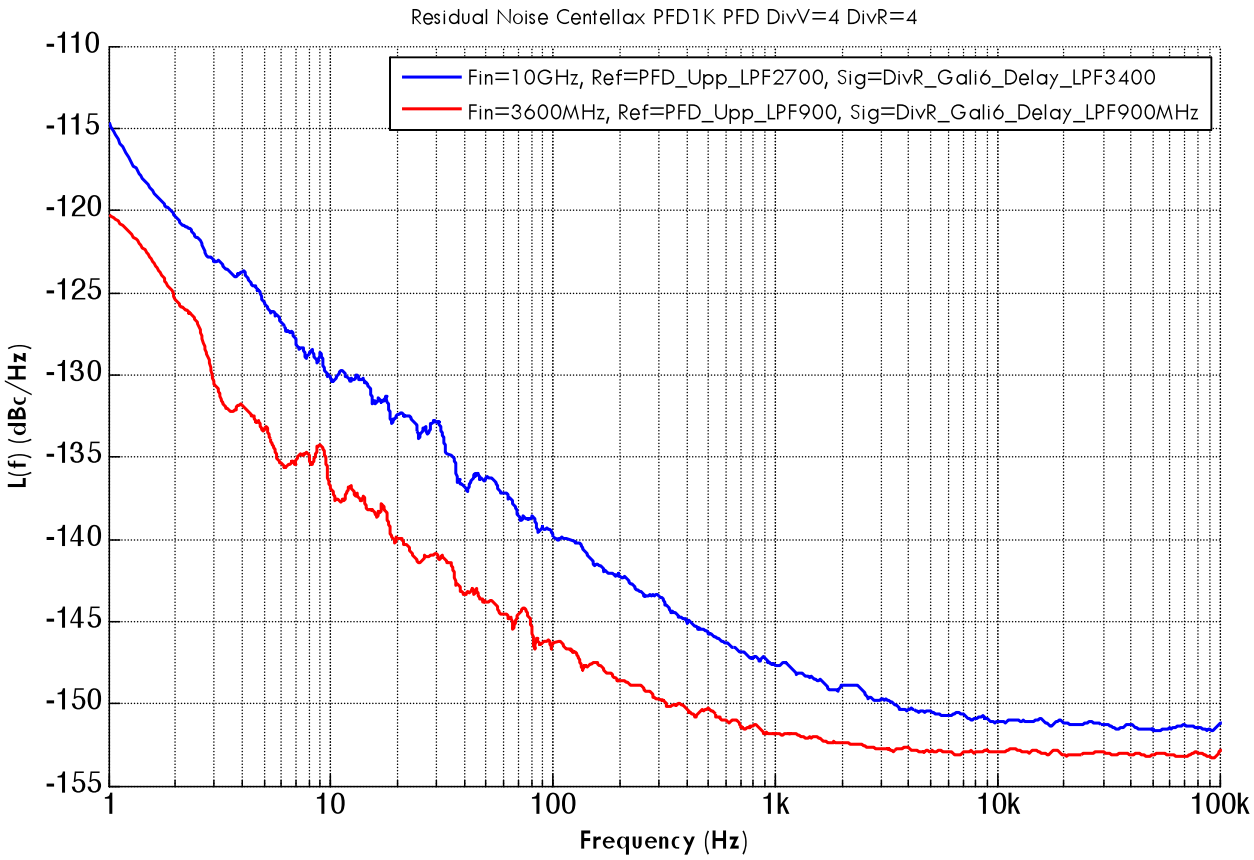
REF lags VCO

$f_{VCO} > f_{REF}$; f_{REF} = 5 GHz; V_{CC} = 3.3 V; T = 25oC; P_{in} = 0 dBm; POL = open



Charge pump outputs for REF lagging VCO

SSB Phase Noise Performance



SSB Phase Noise Performance

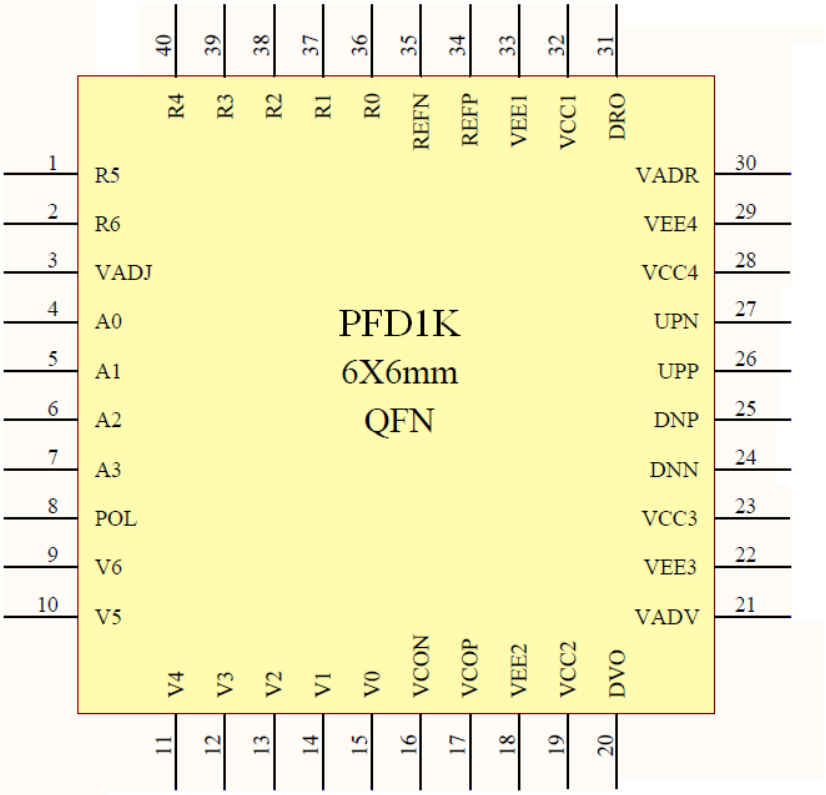
Table 2: RF Pin Description

Port Name	Description	Notes
REFP	Reference RF input, positive terminal	CML signal levels
REFN	Reference RF input, negative terminal	CML signal levels
VCOP	VCO RF input, positive terminal	CML signal levels
VCON	VCO RF input, negative terminal	CML signal levels
UPP	Up Charge Pump output, positive terminal	CML output level set by charge pump gain
UPN	Up Charge Pump output, negative terminal	CML output level set by charge pump gain
DNP	Down Charge Pump output, positive terminal	CML output level set by charge pump gain
DNN	Down Charge Pump output, negative terminal	CML output level set by charge pump gain
DRO	Divided Reference Output (single ended)	CML output level, requires DC pullup
DVO	Divided VCO Output (single ended)	CML output level, requires DC pullup

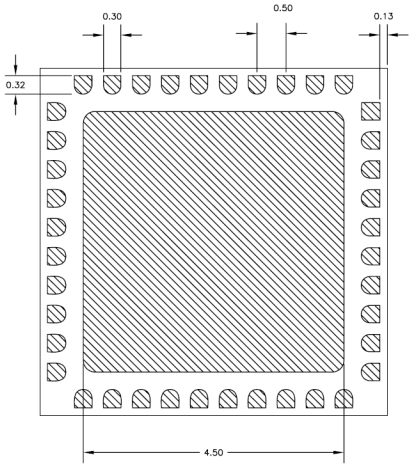
Table 3: DC Pin Descriptions

Port Name	Description	Notes
POL	Polarity of Phase Detector	3.3 V CMOS levels, defaults to logic 0 if open
R[6:0]	Reference Prescaler Divide Ratio	3.3 V CMOS levels, defaults to logic 0 if open
V[6:0]	VCO Prescaler Divide Ratio	3.3 V CMOS levels, defaults to logic 0 if open
A[3:0]	Charge Pump Gain Control	3.3 V CMOS levels, defaults to logic 0 if open
VADJ	Charge Pump Gain Analog Control	From VEE to VCC , VCC for max output
VADR	Divided Reference Output Level Control	From VEE to VCC , VCC for max output
VADV	Divided VCO Output Level Control	From VEE to VCC , VCC for max output
VCC1-4	Positive power supply	+3.3 V @ 500 mA
VEE1-4	Negative power supply	Ground

Pinout Diagram



UXN40M7K Physical Characteristics



Pkg Size:	6.00 x 6.00 mm
Pkg Thickness:	1.1 mm
Pad Dimensions:	0.30 x 0.32 mm
Center Paddle:	4.5 x 4.5 mm
JEDEC Designator:	MO-220
JEDEC designator:	MO-220

Bottom View

Table 4: Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (VCC-VEE)	4	V
RF Input Power (INP, INN)	10	dBm
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 125	ºC
Junction Temperature	125	ºC

ESD Sensitivity:

Although SiGe IC's have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling. Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the low frequency inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400 V. For performance reasons the RF inputs are not protected with ESD diodes and the ESD sensitivity is higher.

PFD1KE Evaluation Kit Datasheet

Phase Detector Evaluation Board

The PFD1KE is the evaluation board for the Microsemi PFD1K phase frequency detector with programmable integer modulus dividers. The PFD1K contains two 40 GHz dividers, an 8 GHz phase frequency detector, and its associated support charge pump circuit. See Figure 1 and 3.

Note: VCC supply voltage must be positive. The +3.3V must be turned on first before applying the +25V and -5V supply. If not turned on, it will damage the phase detector.

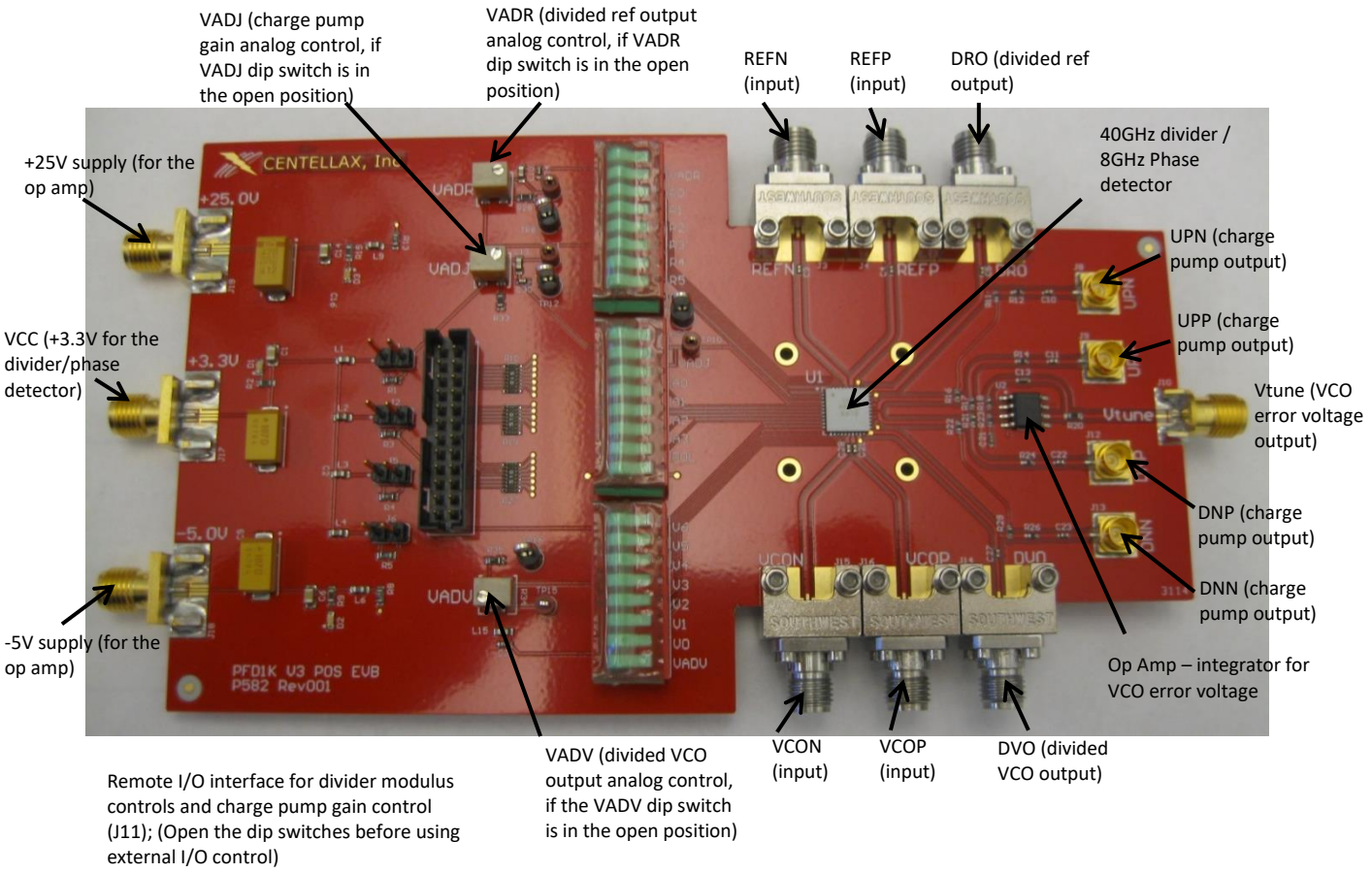


Figure 1. Evaluation board for PFD1KE (P582)

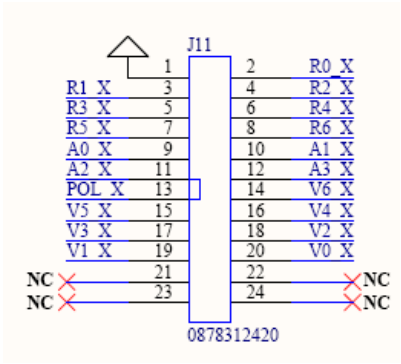


Figure 2. (J11) I/O pin configuration

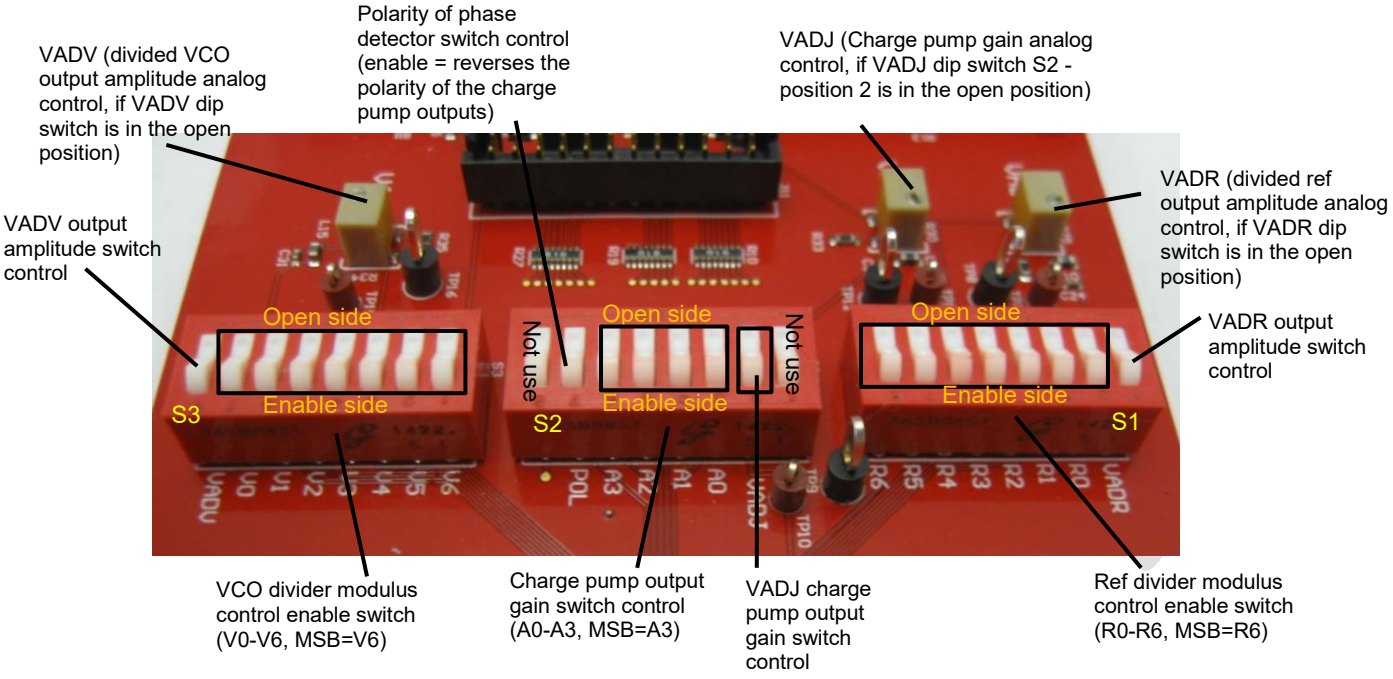


Figure 3. Close up view of the control dip switches on the Evaluation board

Turn on Sequence

1. **Please take caution of static damage as the evaluation board and the phase detector device are both sensitive to static discharge.**
2. If RF inputs/outputs are used in single-ended configuration, terminate unused inputs/outputs with 50 ohm loads.
3. Apply a +3.3V supply (VCC) to the evaluation board (J17, SMA (f) connector) for the divider/phase detector.

   Warning: In order to avoid damaging the device, +3.3V supply must be turned on before turning on the op-amp bias voltages (+25V and -5V).
4. Apply a +25V supply to the evaluation board (J19, SMA (f) connector) for the op-amp.
5. Apply a -5V supply to the evaluation board (J18, SMA (f) connector) for the op-amp.
6. Use on-board dip switches to adjust the Reference and VCO divide ratios. Note all zeros is a default divide by 1.

Switch Settings (Open = 0, Close = 1)		Division Ratio Output
VCO (S3) V6 V5 V4 V3 V2 V1 V0 (V6=MSB)	**REF (S1) R6 R5 R4 R3 R2 R1 R0 (R6=MSB)**	
0000001	0000001	1
1000000	1000000	1/64
1111111	1111111	1/127

Turn on Sequence (continue)

7. Apply RF signals at the inputs (REFP/REFN and VCOP/VCON, 2.9 mm (f) connectors).
8. Set the dip switches VADV (part of S3, VCO) and VADR (part of S1, REF) to the disable (open) position. Adjust the VADV potentiometer to control the desired VCO divider's output amplitude, and adjust the VADR potentiometer to control the desired REF divider's output amplitude.

   The divided RF output signals can be viewed at the DRO port (REF) and at the DVO port (VCO) using a spectrum analyzer or oscilloscope. Those connectors are 2.9 mm (f).

9. Or for maximum output swing on the prescalers, set the dip switches VADV and VADR to the close position. (I.e., set the VADV and VADR voltage levels to the same voltage as VCC). Note, while in logic 1 on the dip switch of VADV and VADR, the VADV and VADR potentiometers will have no effect on the prescalers' output swing voltage.
10. The charge pump output has a digital adjustment for the current which scales the maximum charge pump output. For example if VADJ is ON (S2 dip switch's positon 2 is set to CLOSE/ON), and A0 to A3 (S2) are all set to ON (i.e., logic 1) then the max charge pump output will be 12mA. The A3-A0 switch of S2 settings allow the value to be adjusted as follows:

Switch Settings (S2, Open = 0, Close = 1) **A3 A2 A1 A0 (A3=MSB)**	Charge Pump Output Current
0000	0 mA
0001	0.75 mA
0010	1.5 mA
…..	…..
1111	12 mA

11. Or to control the output of the charge pump manually using the VADJ potentiometer, then set the VADJ dip switch's (S2) - position 2 to OPEN, then uses the VADJ potentiometer to adjust the desire output current swing.
12. The POL dip switch (S2) - position 7 (see Figure 3), allows the polarity of the charge pump to be reversed. This is useful to unlock the loop momentarily.
13. The output of the charge pump can be viewed at UPP/UPN and DWP/DWN connectors (SMP plug (m)) using a spectrum analyzer or oscilloscope. 8 GHz is the maximum frequency output. See Application Notes section for additional info.
14. Optional: The divide ratio of the prescaler and the charge pump output current of the phase frequency detector can also be programmed through (J11), (a 24-pin Molex connector interface, mfg pn 87831-2420), using an external programming device, see Figure 2. If using an external programming device, set the on-board dip switches (S1: R0-R6, S2: A0-A3 and POL, and S3: V0-V6) to the open position first before making connection to the external programming device.

    Note: Do not use both on-board divider modulus control/charge pump control (dip switches) and the external I/O interfaces (J11) at the same time.

Turn on Sequence (continue)

Input voltage levels for the I/O control lines:

Logic Level	Minimum	Typical	Maximum
1 (High)	VCC-1.3V	VCC	VCC
0 (Low)	VEE	VEE	VEE + 0.8V

15. The evaluation board also included an integrator (op-amp circuitry, if the option is loaded) which generates a Vtune error voltage output signal at the Vtune port (2.9 mm (f) connector). This signal can be viewed using a spectrum analyzer or oscilloscope. See the Application Notes section for additional information.

    This error voltage represented the phase frequency difference between the REF and VCO input signals (~ 10 MHz signal, the average of this signal is the VCO's dc error correction voltage).

16. Refer to PFD1K datasheet for performance specifications.

Pin Descriptions:

Pin #	Port Name	Description	Notes
34	REFP	Reference RF input, positive terminal	CML signal levels
35	REFN	Reference RF input, negative terminal	CML signal levels
17	VCOP	VCO RF input, positive terminal	CML signal levels
16	VCON	VCO RF input, negative terminal	CML signal levels
26	UPP	Up Charge Pump output, positive terminal	CML output level set by charge pump gain
27	UPN	Up Charge Pump output, negative terminal	CML output level set by charge pump gain
25	DNP	Down Charge Pump output, positive terminal	CML output level set by charge pump gain
24	DNN	Down Charge Pump output, negative terminal	CML output level set by charge pump gain
31	DRO	Divided Reference Output (single ended)	CML output level, requires DC pullup
20	DVO	Divided VCO Output (single ended)	CML output level, requires DC pullup

Pin #	Port Name	Description	Notes
8	POL	Polarity of Phase Detector	3.3 V CMOS levels, defaults to logic 0 if open
2, 1, 40, 39, 38, 37, 36	R[6:0]	Reference Prescaler Divide Ratio	3.3 V CMOS levels, defaults to logic 0 if open
9, 10, 11, 12, 13, 14, 15	V[6:0]	VCO Prescaler Divide Ratio	3.3 V CMOS levels, defaults to logic 0 if open
7, 6, 5, 4	A[3:0]	Charge Pump Gain Control	3.3 V CMOS levels, defaults to logic 0 if open
3	VADJ	Charge Pump Gain Analog Control	From VEE to VCC, VCC for max output
30	VADR	Divided Reference Output Level Control	From VEE to VCC, VCC for max output
21	VADV	Divided VCO Output Level Control	From VEE to VCC, VCC for max output
32, 19, 23, 28	VCC1-4	Positive power supply	+3.3 V @ 500 mA
33, 18, 22, 29	VEE1-4	Negative power supply	Ground
Paddle	Paddle	Package Paddle	Tie to heatsink

Application Notes

1. All of the controls on the evaluation board are brought out to a Molex test connector (J11) for programmability. A 0V to +3.3V TTL signal can be used to override the dip switches (except for the VADV, VADR, and VADJ switches). Set those dip switch positions to **OFF** and apply a +3.3V TTL signal (i.e., a logic "High" level) to the test header.
2. The evaluation board has an OP AMP to drive a Varactor VCO oscillator with a 0V to 20V tuning voltage (see Figure 4). Make sure that the proper NO-LOAD resistors are installed to enable the OP AMP circuitry (refer to the schematic in Figure 5) and make sure that a -5VEE and +25VCC supply are connected. The -5V and +25V supplies are not needed if the OP AMP integrator circuitry is not needed.

   If evaluating the output charge pump circuit (i.e., UPN/UPP and DNP/DNN outputs), make sure R12, R14, R24 and R26 (0 Ω) resistors are loaded. Also remove R17 and R21 (200 Ω) resistors. If not, those two resistors (R17 and R21) will load down the phase detector charge pump output circuit. However, it is ok to leave them in place during the evaluation if the output level of the charge pump circuit is not a concern.

   If using the Vtune (op-amp) output (J10) for evaluation, terminate the UPN/UPP and DNP/DNN output ports with 50 Ω load to minimize reflection. This action will also lower the output amplitude signal level by a small amount.
3. Figure 4 shows a block diagram of the PFD1K phase frequency detector and the VCO error voltage integrator circuit (if loaded) that is part of the evaluation board.
4. A schematic of the evaluation board is included on the next page (figure 5).

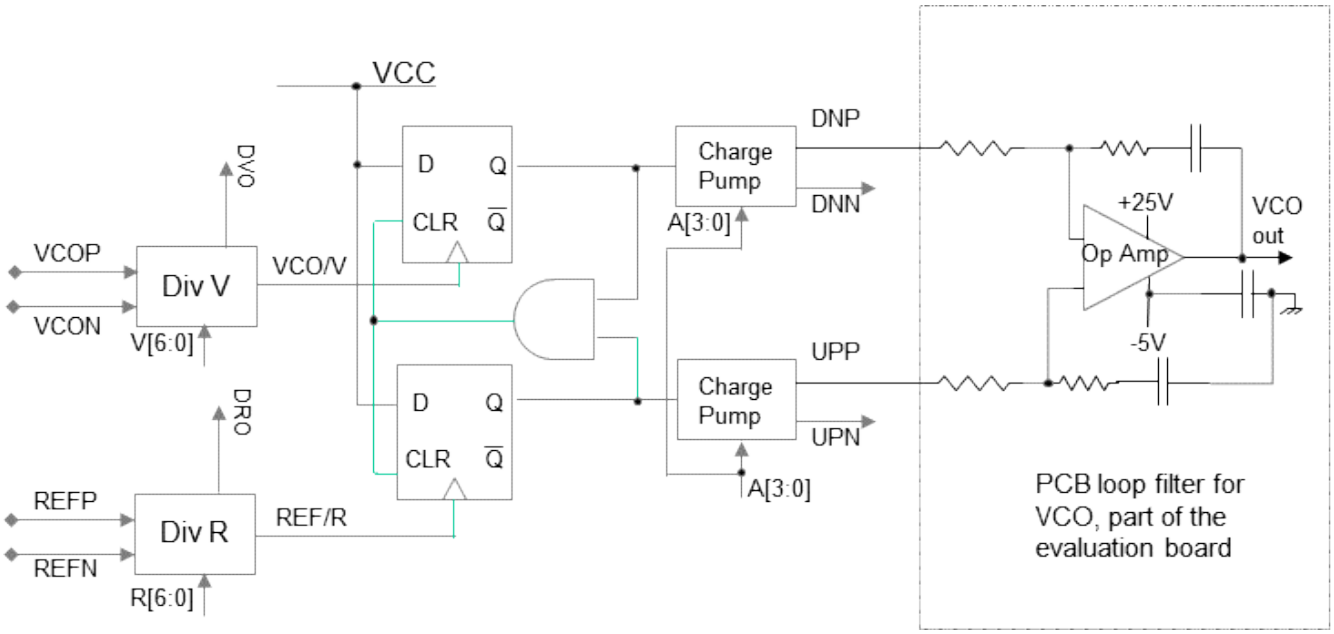


Figure 4. Block diagram for PFD1KE evaluation PC board including loop filter and VCO op-amp

PFD1KE Evaluation Board Schematic

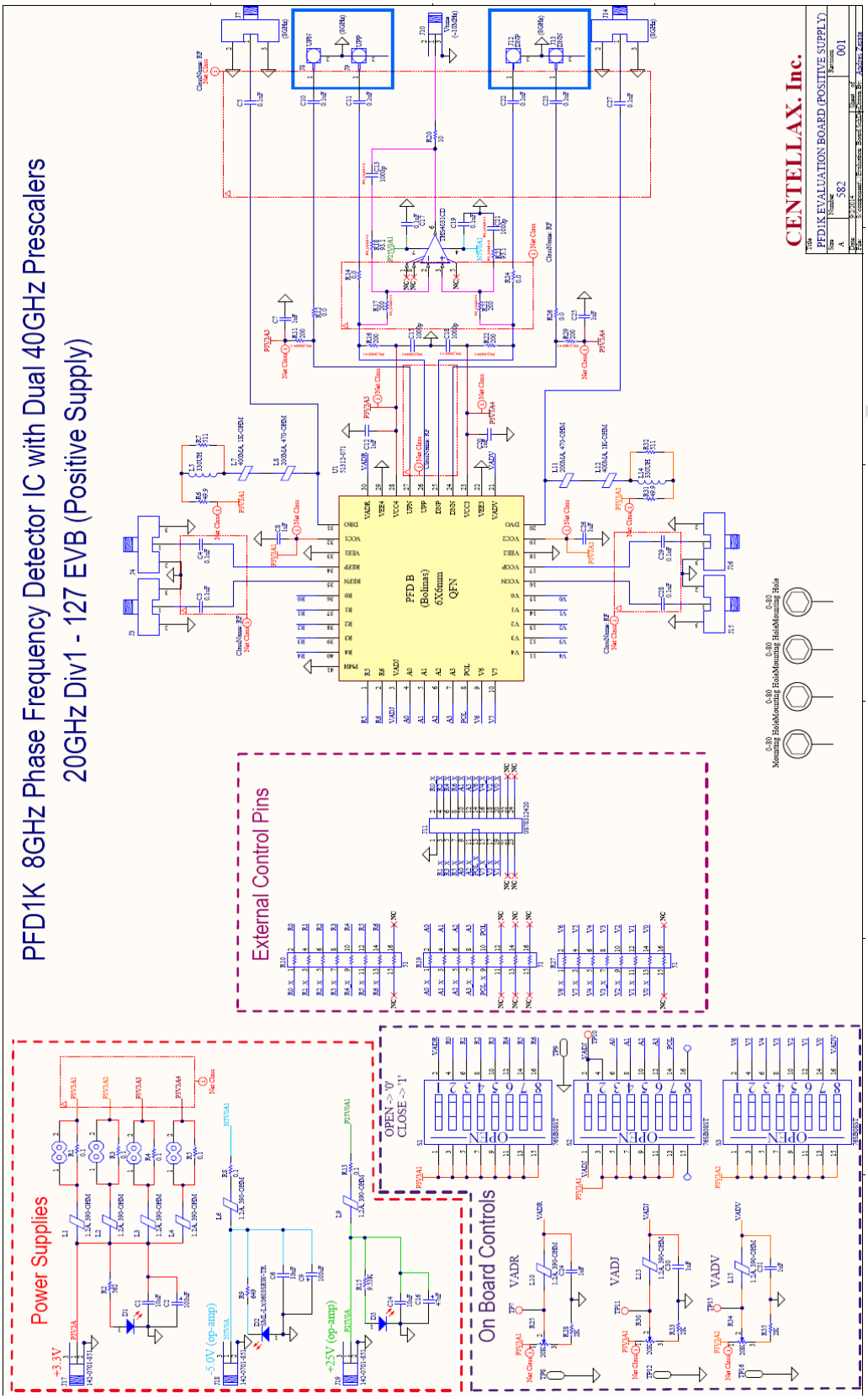


Figure 5. Schematic for the PFD1KE evaluation PC board

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