MIC5249

300 mA µCap LDO with Programmable Power-On Reset Delay

Features

- 300 mA Output Current
- High PSRR: 65 dB@120 Hz
- Stable with Ceramic Output Capacitor
- Power-on-Reset (POR) Output with Adjustable Delay Time
- High Output Accuracy:
  - ±1.0% Initial Accuracy
  - ±3.0% Over Temperature
- Low Dropout Voltage of 340 mV @ 300 mA
- Low Quiescent Current: 85 µA
- Zero Current Shutdown Mode
- Thermal Shutdown and Current-Limit Protection
- Tiny MSOP-8 Package

Applications

- Cellular Phones
- PDAs
- Fiber Optic Modules

General Description

The MIC5249 is an efficient, precise 300 mA CMOS voltage regulator with power on reset (POR) delay which can be implemented via an external capacitor. It offers 1% initial accuracy, extremely low dropout voltage (typically 400 mV @ 300 mA), and low ground current (typically 85 mA) over load.

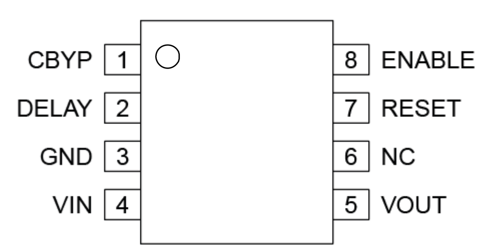
Designed specifically for noise-critical applications in hand-held or battery-powered devices, the MIC5249 comes equipped with a noise reduction feature to filter the output noise via an external capacitor. Other features of the MIC5249 include a logic-compatible enable pin, current limit, thermal shutdown, ultra-fast transient response, and an active clamp to speed up device turnoff.

The MIC5249 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices.

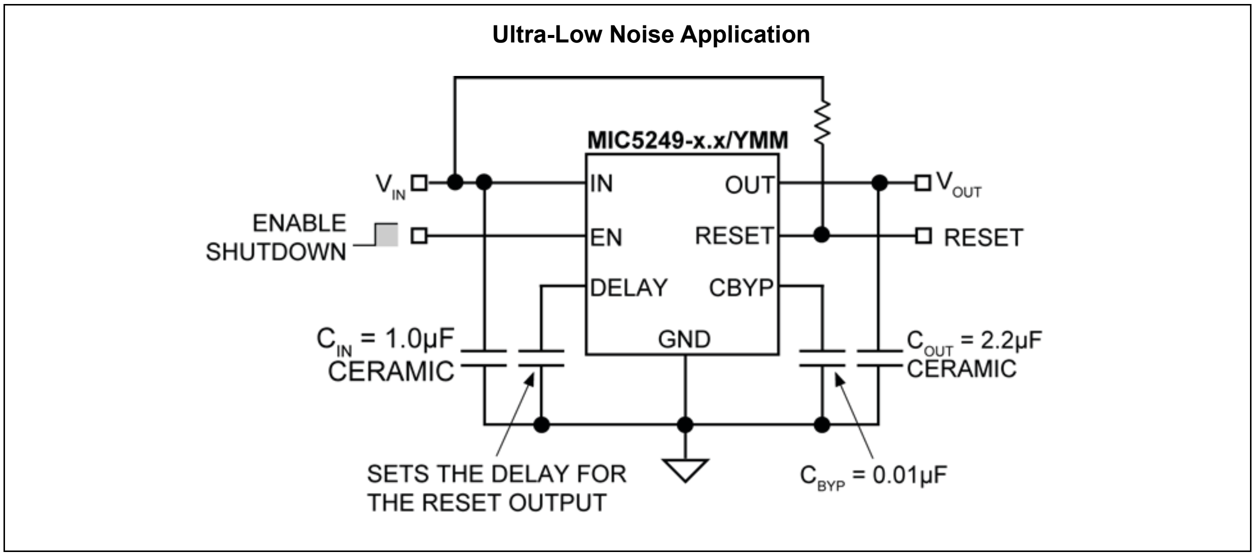
The MIC5249 is available in the MSOP-8 package.

Package Type

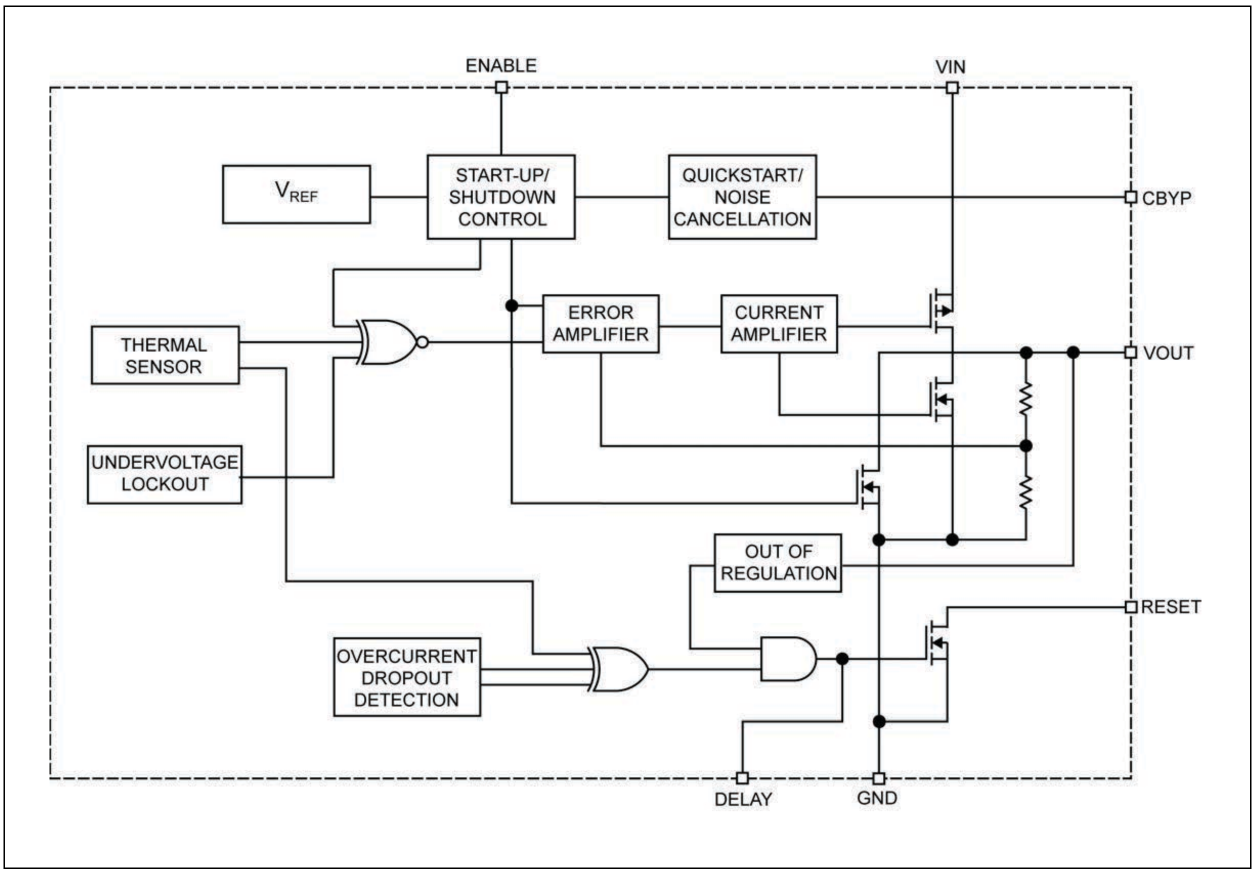
MIC5249
8-Lead MSOP (MM)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) .... 0V to +7V
Enable Input Voltage (V_{EN}) .... 0V to +7V
Power Dissipation (P_D), Note 1 .... Internally Limited
ESD Rating, Note 2 .... ESD Sensitive

Operating Ratings ‡

Supply Voltage (V_{IN}) .... +2.7V to +6V
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{OUT}$ + 1V; I_{OUT} = 100 µA; T_J = +25°C;
Bold values indicate –40°C to +125°C unless noted.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_{OUT}	–1.0	—	+1.0	%	Variation from nominal V_{OUT}
		–3.0	—	**+3.0**		
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	–0.3	0.02	+0.3	%/V	$V_{IN} = V_{OUT}$ + 1V to 6V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	1.5	3.0	%	I_{OUT} = 0.1 mA to 300 mA
Dropout Voltage	V_{DO}	—	1	—	mV	I_{OUT} = 100 µA
		—	160	225 **275**		I_{OUT} = 150 mA
		—	340	500 **600**		I_{OUT} = 300 mA
Ground Pin Current	I_{GND}	—	85	**150**	µA	I_{OUT} = 0 mA
			100	**200**		I_{OUT} = 300 mA
Ground Pin Current in Shutdown	I_{SHDN}	—	0.35	1	µA	V_{EN} < 0.4V (Regulator OFF)
Ripple Rejection	PSRR	—	65	—	dB	f = 120 Hz; C_{OUT} = 2.2 µF
Current Limit	I_{LIM}	**300**	440		mA	V_{OUT} = 0V
Enable Input						
Enable Input Voltage	V_{IL}	—	—	**0.4**	V	Logic low (regulator shutdown)
	V_{IH}	**1.6**	—	—		Logic high (regulator enabled)
Enable Input Current	I_{IL}	—	0.01	—	µA	V_{IL} < 0.4V (regulator shutdown)
	I_{IH}	—	0.01	—		V_{IH} > 1.6V (regulator enabled)

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; $I_{OUT} = 100\ \mu A$; $T_J = +25°C$;
Bold values indicate –40°C to +125°C unless noted.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Delay Input						
Delay Pin Current Source	I_{DELAY_TH}	—	0.55	1	µA	—
Delay Pin Threshold Voltage	V_{DELAY_TH}	—	1.4	—	V	Threshold for RESET = Logic high
RESET Output						
Reset Low Threshold	V_{THL}	**89**	91	—	%	% of V_{OUT} (Flag ON)
Reset High Threshold	V_{THH}	—	93	**96**		% of V_{OUT} (Flag OFF)
Reset Output Logic-Low Voltage	V_{OL}	—	0.02	**0.1**	V	I_{RESET} = 100 µA output in fault condition
Flag Leakage Current	I_{RESET}	—	0.01	—	µA	Flag OFF

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 5 sec.
Package Thermal Resistances						
Thermal Resistance, MSOP-8	θ_{JA}	—	160	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	CBYP	Reference Bypass. Connect external 0.01µF capacitor to GND to reduce output noise. May be left open.
2	DELAY	Delay Set Input. Connect external capacitor to GND to set the delay of the Error Flag.
3	GND	Ground.
4	VIN	Supply input.
5	VOUT	Regulator output.
6	NC	No connect.
7	RESET	RESET Output. Open-drain output. Active low indicates an output undervoltage condition.
8	ENABLE	Enable Input: CMOS-compatible input. Logic high = enable; Logic low = shutdown. Do not leave open.

3.0 APPLICATION INFORMATION

3.1 Enable/Shutdown

The MIC5249 comes with an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a “zero” off-mode-current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. This part is CMOS and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

3.2 Input Capacitor

The MIC5249 is a high-performance, high-bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1.0 µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors such as small valued NPO dielectric type capacitors help to filter out high frequency noise and are good practice in any RF-based circuit.

3.3 Output Capacitor

The MIC5249 requires an output capacitor of 2.2 µF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High-ESR capacitors may cause high frequency oscillation. The maximum recommended ESR is 300 mΩ. The output capacitor can be increased, but performance has been optimized for a 2.2 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than anX7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

3.4 DELAY Pin Input

The power-on-reset (POR) function can be implemented on the MIC5249 by adding an external capacitor from the DELAY pin to ground. This external capacitor sets the delay time (t_{DELAY}) of the RESET output.

The capacitor value required can be easily calculated using the formula:

EQUATION 3-1:

$$C_{DELAY} = \left(\frac{T_{DELAY} \times I_{DELAY}}{V_{DELAY}}\right)$$

Where:

I_{DELAY} = 0.55 µA

V_{DELAY} = 1.4V

When no capacitor is used, there will be no delay and the POR output acts like a standard error FLAG output.

3.5 RESET Output

The RESET output of the MIC5249 provides the power-on reset signal based on the capacitor from the DELAY pin to ground when input power is applied to the regulator. The reset signal stays low for a preset time period after power is applied to the regulator, and then goes high.

The reset output is an active-low, open-drain output that drives low when a fault condition AND an undervoltage detection occurs. Internal circuitry intelligently monitors overcurrent, overtemperature and dropout conditions and ORs these outputs together to indicate some fault condition. The output of that OR gate is ANDed with an output voltage monitor that detects an undervoltage condition. The output drives an open-drain transistor to indicate a fault. This prevents chattering or inadvertent triggering of the reset. There set must be pulled up using a resistor form the RESET pin to either the input or the output.

3.6 Bypass Pin Output

A bypass capacitor is required from the noise bypass pin to ground to reduce output voltage noise. The capacitor bypasses the internal reference. A 0.01 µF capacitor is recommended for applications that require low-noise outputs. The bypass capacitor can be increased, further reducing noise and improving PSRR. Turn-on time increases slightly with respect to bypass capacitance. A unique quick-start circuit allows the MIC5249 to drive a large capacitor on the bypass pin without significantly slowing the turn-on time.

3.7 Active Shutdown

The MIC5249 also features an active shutdown clamp, which is a N-Channel MOSFET that turns on when the device is disabled. This allows the output capacitor and load to discharge, de-energizing the load.

3.8 No-Load Stability

The MIC5249 will remain stable and in regulation with no load unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive application.

3.9 Thermal Considerations

The MIC5249 is designed to provide 300 mA of continuous current in a very small package. Maximum power dissipation can be calculated based on the output current and the voltage drop across the device. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 3-2:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}}\right)$$

Where:

$T_{J(MAX)}$ = The maximum junction temperature of the die, 125°C

T_A = The ambient operating temperature

θ_{JA} = Layout independent

Table 3-1 shows examples of the junction-to-ambient thermal resistance for MIC5249.

TABLE 3-1: MSOP-8 THERMAL RESISTANCE

Package	θ_{JA} Recommended Minimum Footprint
MSOP-8	160°C/W

The actual power dissipation of the regulator circuit can be determined using the equation:

EQUATION 3-3:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}$$

Substituting $P_{D(MAX)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, when operating the MIC5249-3.0YMM at 50°C with a minimum footprint layout, the maximum input voltage for a set output current can be determined as follows:

EQUATION 3-4:

$$P_{D(MAX)} = (125°C - 50°C)/(160°C/W)$$

The junction-to-ambient thermal resistance for the minimum footprint is 160°C/W, from Table 3-1. The maximum power dissipation must not be exceeded for proper operation. Using the output voltage of 3.0V, and an output current of 300 mA, the maximum input voltage can be determined. Because this device is CMOS and the ground current is typically 90 µA over the load range, the power dissipation contributed by the ground current is < 1.0% and can be ignored for this calculation:

EQUATION 3-5:

$$468mW = (V_{IN} - 3.0V)300mA$$

$$468mW = V_{IN} \times 300mA - 900mW$$

$$1368mW = V_{IN} \times 300mA$$

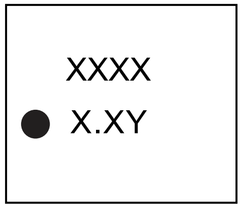
$$V_{IN(MAX)} = 4.56V$$

Therefore, a 3.0V application at 300 mA of output current can accept a maximum input voltage of 4.56V in the MSOP-8 package. For a full discussion of heat sinking and thermal effects on the voltage regulators, refer to the Regulator Thermals section of Designing with Low-Dropout Voltage Regulators handbook.

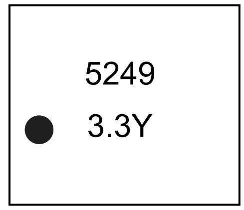
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead MSOP*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

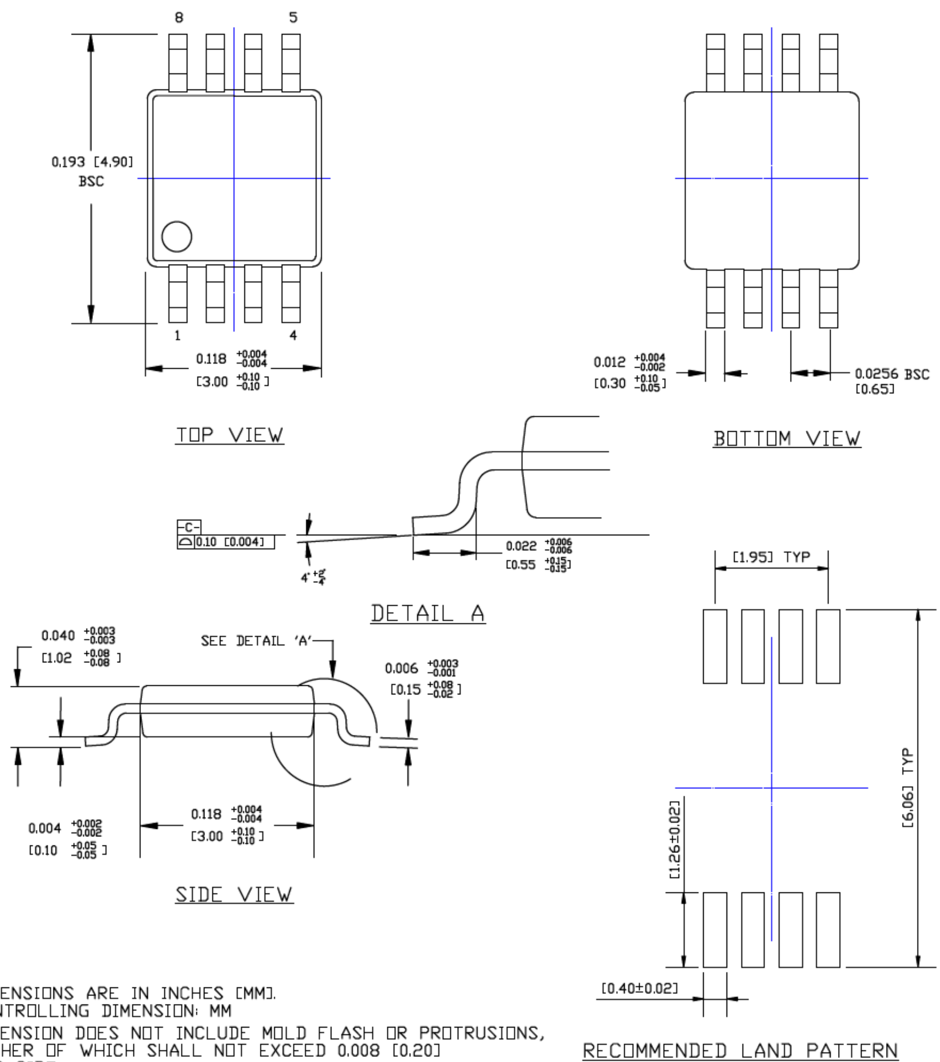
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

8-Lead MSOP Package Outline and Recommended Land Pattern

TITLE
8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	MSOP-8LD-PL-1	**UNIT**	INCH [MM]



NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.20] PER SIDE.

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2021)

- Converted Micrel document MIC5249 to Microchip data sheet DS20006602A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	-XX	X	XX	-XX
Device	Voltage Option	Junction Temperature Range	Package	Media Type

Device:	MIC5249: 300 mA µCap LDO with Programmable Power-On Reset Delay
Voltage Option	1.5 = 1.5V 1.8 = 1.8V 2.5 = 2.5V 2.6 = 2.6V 2.8 = 2.8V 2.85 = 2.85V 3.0 = 3.0V 3.3 = 3.3V
Junction Temperature Range:	Y = –40°C to +125°C
Package:	MM = 8-Lead MSOP (Pb-Free)
Media Type:	<blank> =100/Tube TR = 2,500/Reel

Examples:

a) MIC5249-1.8YMM	300 mA µCap LDO with Programmable Power-On Reset Delay, 1.8V, –40°C to +125°C, 8-Lead MSOP, 100/Tube
b) MIC5249-1.8YMM-TR	300 mA µCap LDO with Programmable Power-On Reset Delay, 1.8V, –40°C to +125°C, 8-Lead MSOP, 2,500/Reel
c) MIC5249-2.85YMM	300 mA µCap LDO with Programmable Power-On Reset Delay, 2.85V, –40°C to +125°C, 8-Lead MSOP, 100/Tube
c) MIC5249-2.85YMM-TR	300 mA µCap LDO with Programmable Power-On Reset Delay, 2.85V, –40°C to +125°C, 8-Lead MSOP, 2,500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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