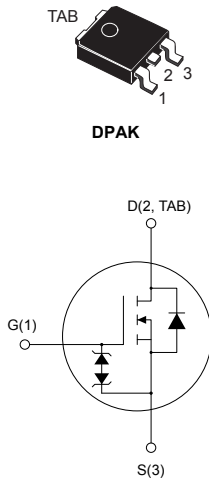


## N-channel 525 V, 730 mΩ typ., 6 A MDmesh K3 Power MOSFET in a DPAK package



AM01476v1\_tab



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD7N52K3	525 V	850 mΩ	6 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

#### Product status link

[STD7N52K3](#)

#### Product summary

Order code	STD7N52K3
Marking	7N52K3
Package	DPAK
Packing	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	525	V
$V_{GS}$	Gate-source voltage	±30	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	6	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	3.8	
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	90	W
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	3	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	110	mJ
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	2.5	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_J$	Operating junction temperature range		°C

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 3.8\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.39	°C/W
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	525			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 525\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 525\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	
$I_{GSS}$	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$		730	850	m $\Omega$

1. Specified by design, not tested in production.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	870	-	pF
$C_{oss}$	Output capacitance		-	70	-	pF
$C_{rss}$	Reverse transfer capacitance		-	13	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }420\text{ V}$	-	53	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 420\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	33	-	nC
$Q_{gs}$	Gate-source charge		-	6	-	nC
$Q_{gd}$	Gate-drain charge		-	21	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	13	-	ns
$t_r$	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	36	-	ns
$t_f$	Fall time		-	19	-	ns

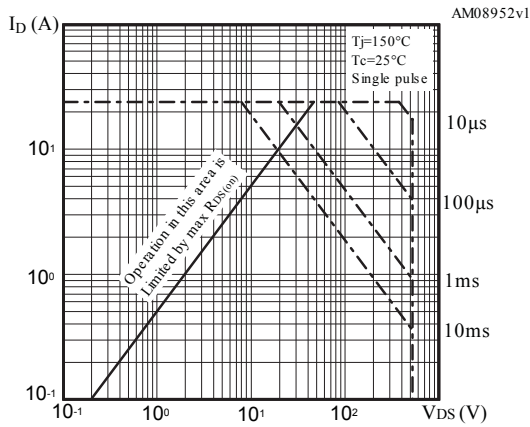
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	220		ns
$Q_{rr}$	Reverse recovery charge		-	1.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	16		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	250		ns
$Q_{rr}$	Reverse recovery charge		-	2.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A

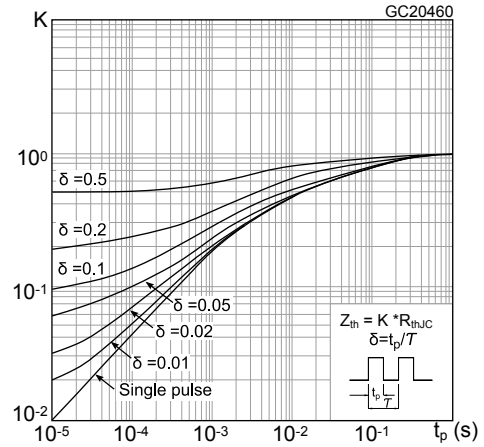
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

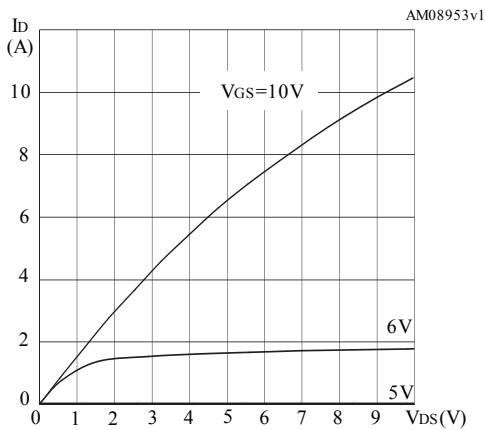
**Figure 1. Safe operating area**



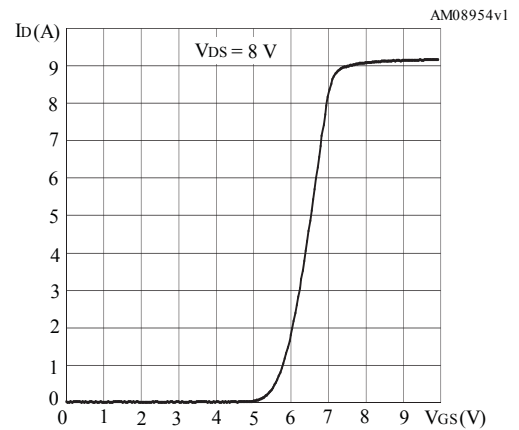
**Figure 2. Normalized transient thermal impedance**



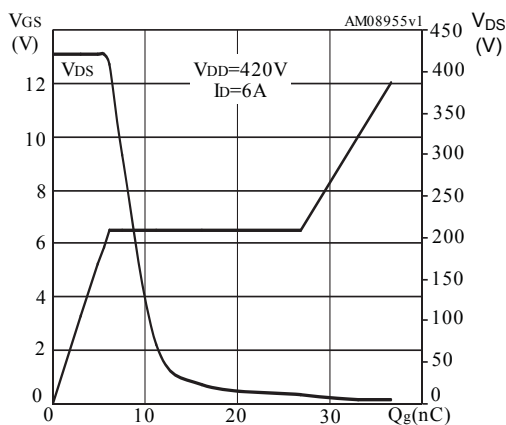
**Figure 3. Typical output characteristics**



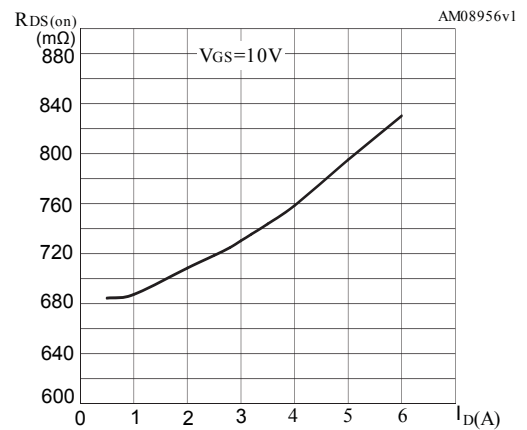
**Figure 4. Typical transfer characteristics**



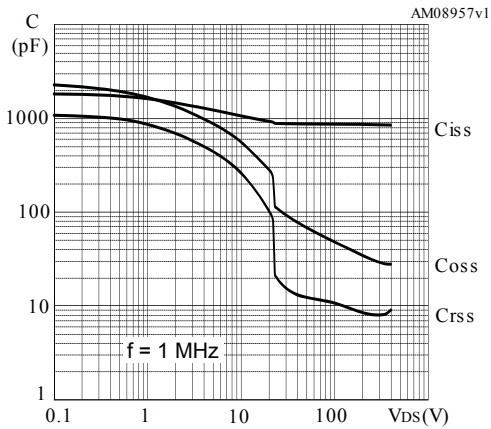
**Figure 5. Typical gate charge characteristics**



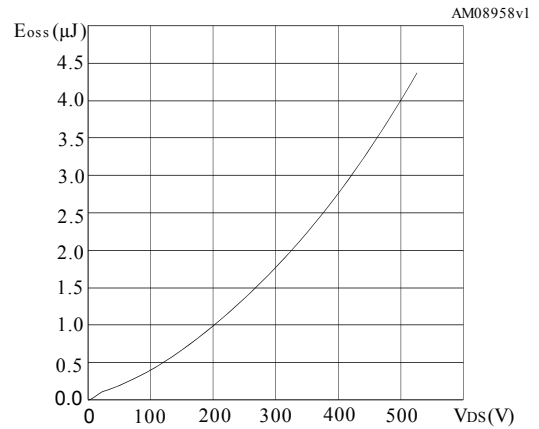
**Figure 6. Typical drain-source on-resistance**



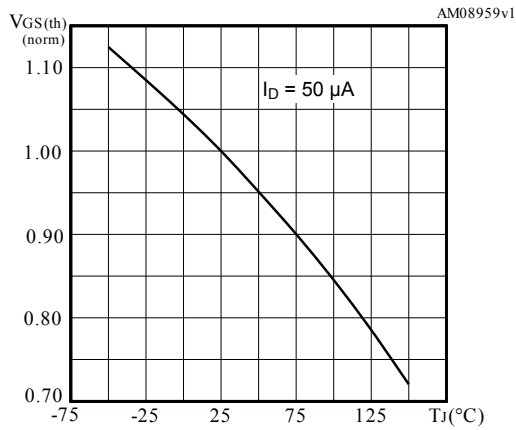
**Figure 7. Typical capacitance characteristics**



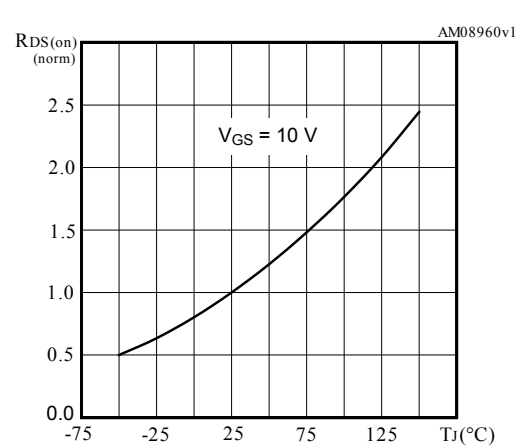
**Figure 8. Typical output capacitance stored energy**



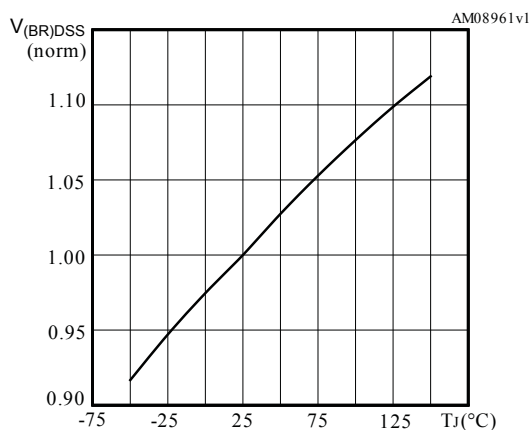
**Figure 9. Normalized gate threshold vs temperature**



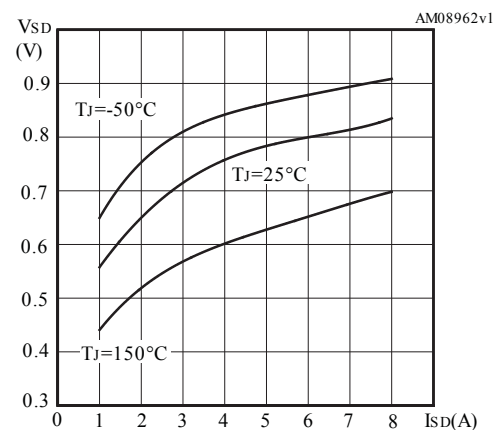
**Figure 10. Normalized on-resistance vs temperature**



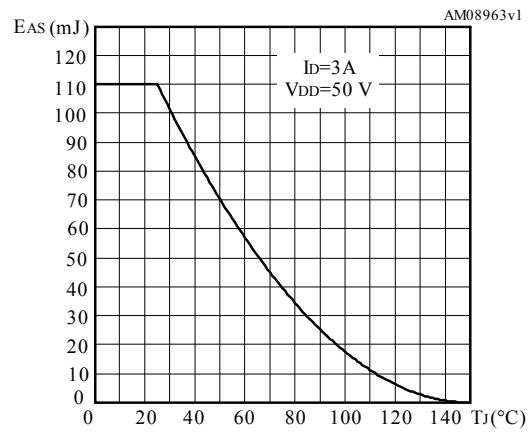
**Figure 11. Normalized breakdown voltage vs temperature**



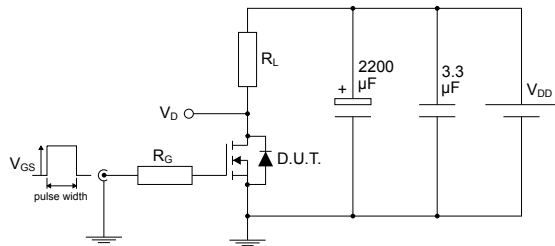
**Figure 12. Typical reverse diode forward characteristics**



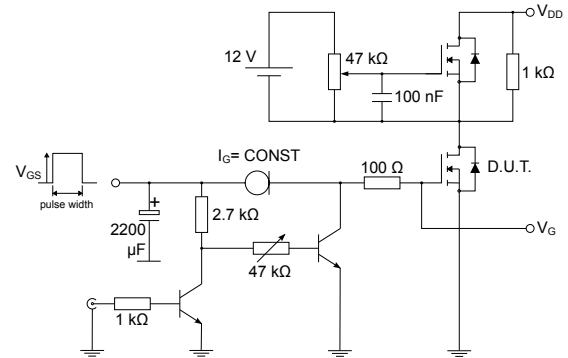
**Figure 13. Maximum avalanche energy vs starting  $T_J$**



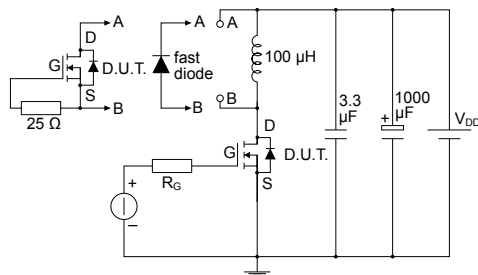
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


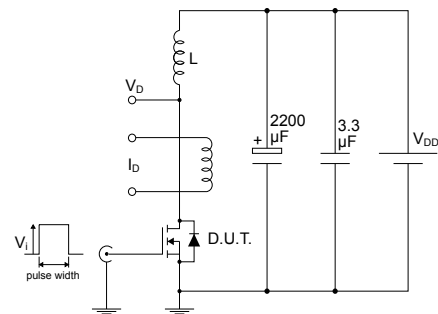
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**Figure 15. Test circuit for gate charge behavior**


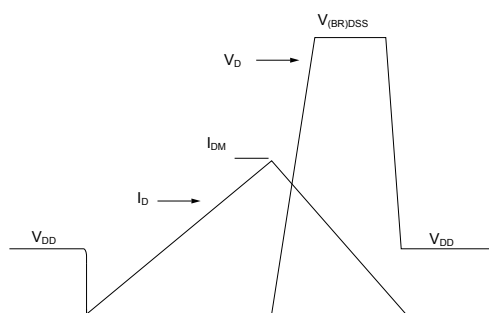
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


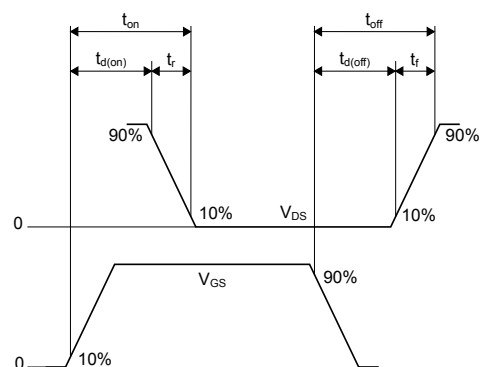
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


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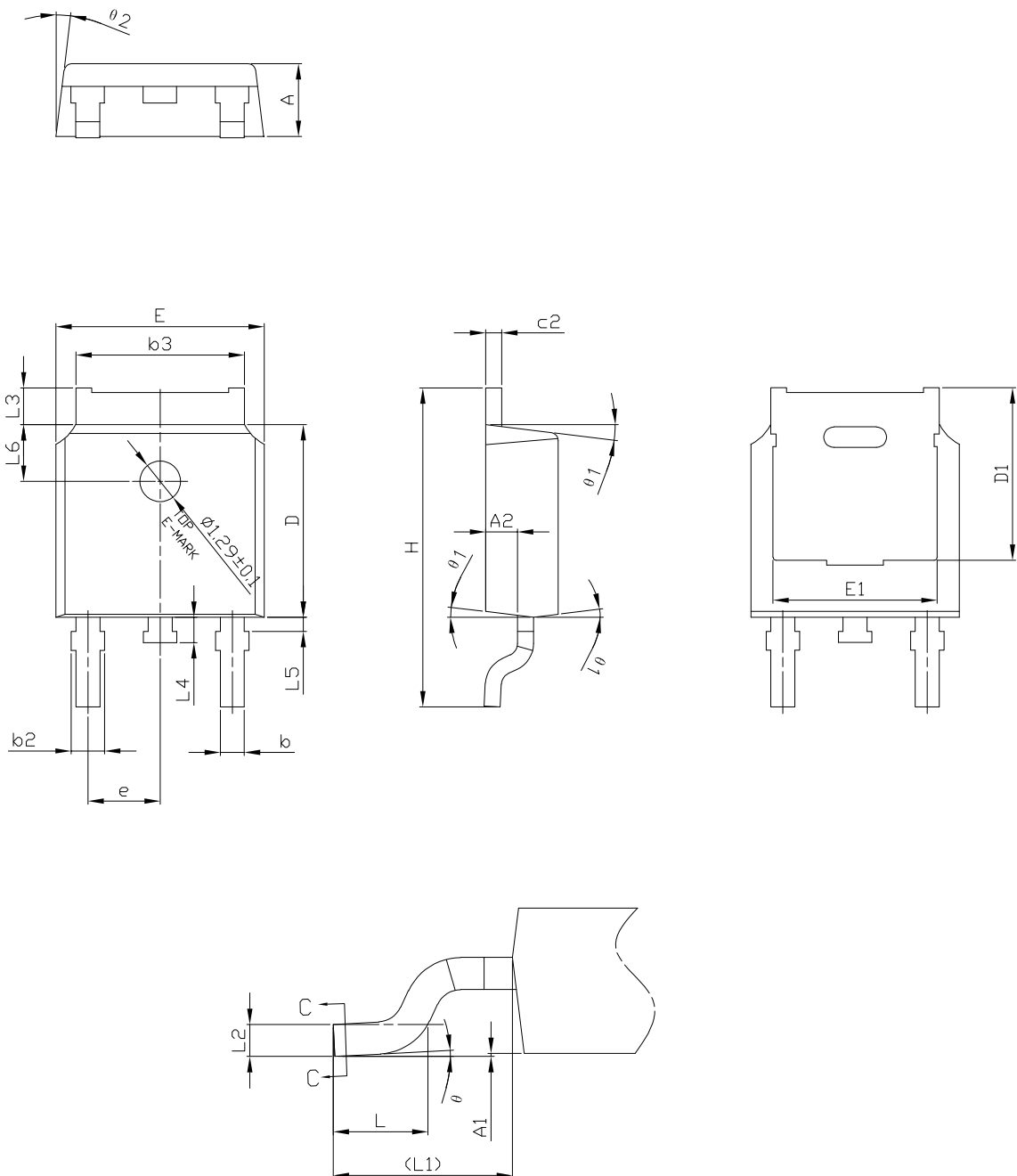


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type C3 package information

**Figure 20. DPAK (TO-252) type C3 package outline**

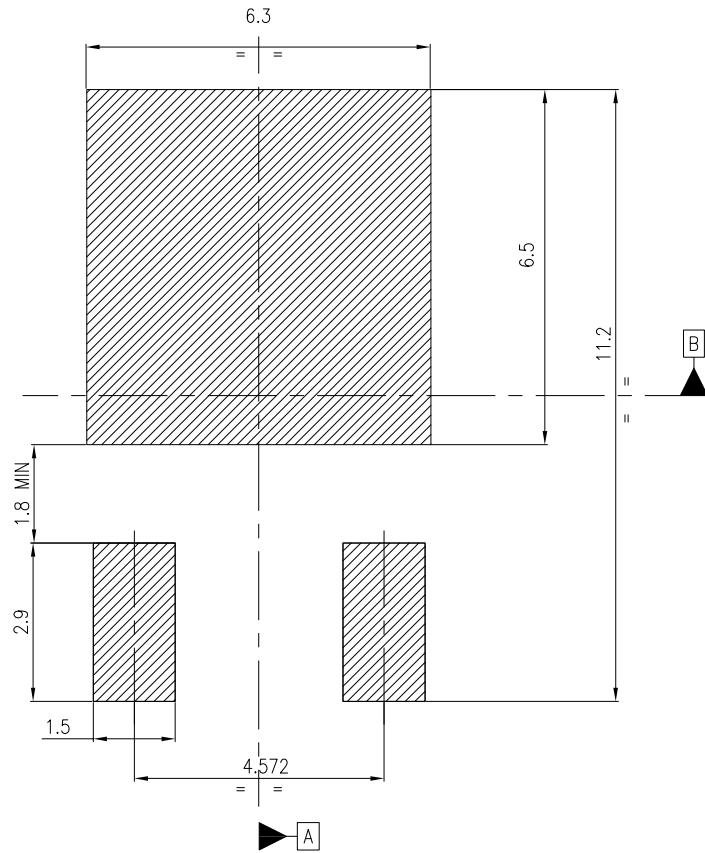


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**Table 7. DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)



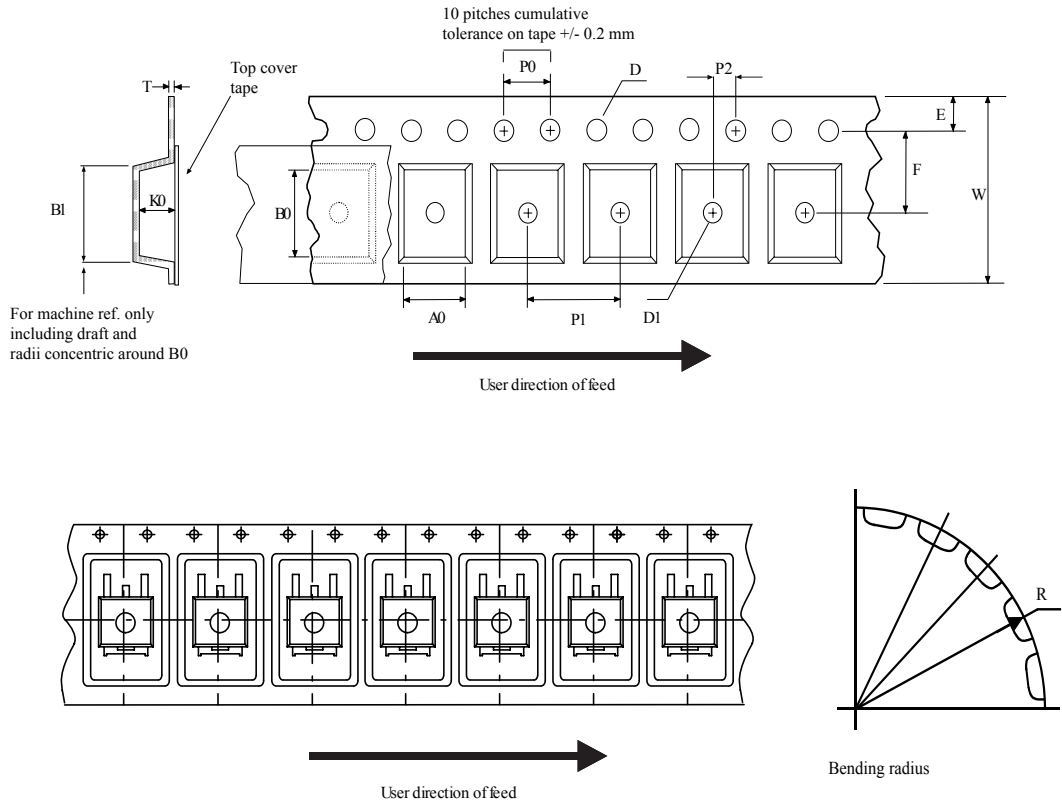
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within  $\boxed{\oplus 0.05 \text{ A B}}$

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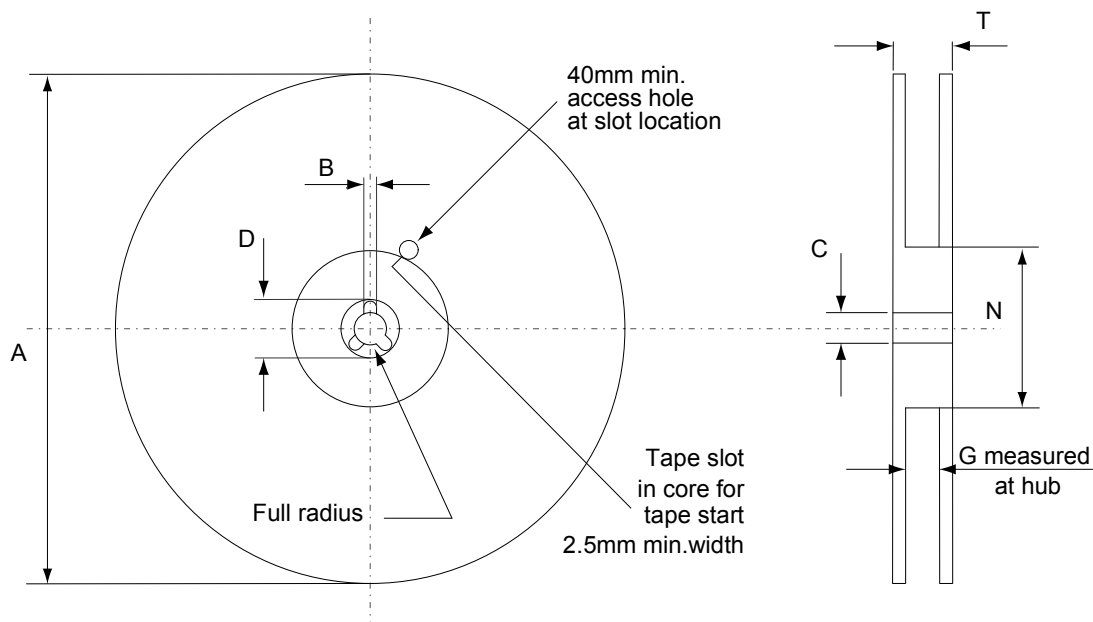
## 4.2 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



AM08852v1

**Figure 23. DPAK (TO-252) reel outline**



AM06038v1

**Table 8. DPAK (TO-252) tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
07-Jul-2008	1	First release.
10-Sep-2009	2	Document status promoted from preliminary data to datasheet.
27-Jun-2011	3	<i>Section 2.1: Electrical characteristics (curves)</i> has been updated.
07-Mar-2012	4	Updated <i>Section 4: Package mechanical data</i> . Minor text changes.
11-Jul-2018	5	Part numbers STB7N52K3 and STF7N52K3 have been moved to a different datasheet, and the document has been updated accordingly. Updated features and description on cover page. Updated <i>Table 1. Absolute maximum ratings</i> . Updated <i>Section 4.1 DPAK (TO-252) type A2 package information</i> . Minor text changes.
01-Aug-2018	6	Updated <i>Table 1. Absolute maximum ratings</i> .
17-Jul-2023	7	The part number STP7N52K3 has been moved to separate datasheet and the document has been updated accordingly. Modified the entire <i>Section 4 Package information</i> . Minor text changes.

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