5.5V-60V Vin, 3A, High Efficiency Step-down DCDC Converter

FEATURES

- Wide Input Range: 5.5V-60V
- Up to 3A Continuous Output Current
- 1.221V ±2% Feedback Reference Voltage
- Integrated 220mΩ High-Side MOSFET
- Low Quiescent Current: 300uA
- Pulse Skipping Mode (PSM) in light load
- 100ns Minimum On-time
- 16ms Internal Soft-start Time
- Internal compensation for Ease of Use
- Fixed Frequency 500kHz
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Over-voltage and Over-Temperature Protection
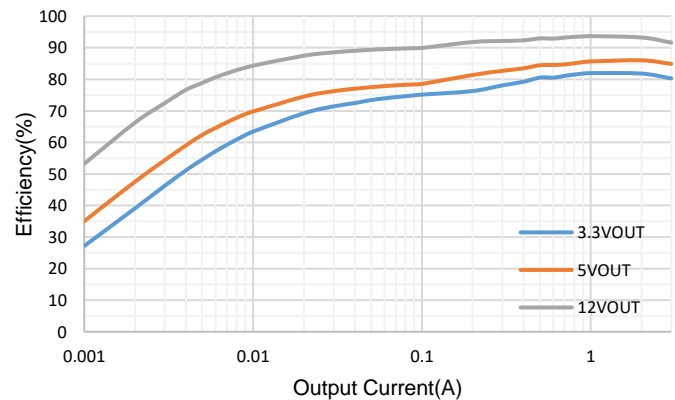- Available in an ESOP-8 Package

APPLICATIONS

- 12-V, 24-V, 48-V Industry and Telecom Power System
- Industrial Automation and Motor Control
- Vehicle Accessories

TYPICAL APPLICATION
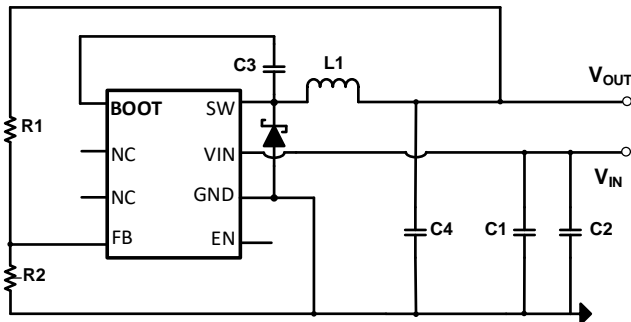
5.5V-60V, Asyncronous Buck Converter

Efficiency, Vin=24V

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
LM22676MRX	LM22676	SOP-8-EP
1) For Tape & Reel, Add Suffix R		

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted[1]

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	65	V
BOOT	-0.3	72	V
SW	-1	65	V
BOOT-SW	-0.3	6	V
SS, FB, RT/CLK	-0.3	6	V
Operating junction temperature TJ[2]	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.
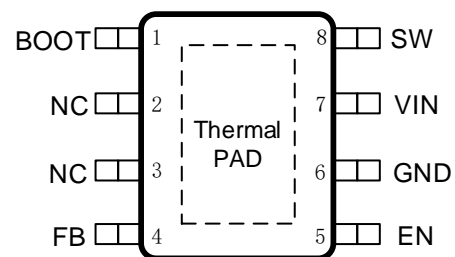
PIN CONFIGURATION

Figure 1. 8-Lead Plastic ESOP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
NC	2	NC
NC	3	NC
FB	4	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 1.221V typical.
EN	5	Enable pin to the regulator with internal pull-up current source. Pull below 1.05V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
GND	6	Ground
VIN	7	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	5.5	60	V
V_{OUT}	Output voltage range	0.8	57	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins[1]	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins[2]	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.34	°C/W
$R_{\theta JCtop}$	Junction to case thermal resistance	61.49	
$R_{\theta JCbot}$	Junction to case(bottom) thermal resistance	4.52	
$R_{\psi JT}$	Junction-to-top characterization parameter	5.62	

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		5.5		60	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		4.3		V
	Hysteresis			400		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		2	5	µA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		300		µA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		220		mΩ
Reference						
V_{REF}	Reference voltage of FB		1.196	1.221	1.246	V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		4.25	4.75	5.25	A
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1.6		µA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5		uA
T_{ss}	Internal soft start time			16		ms
Switching Frequency and External Clock Synchronization						
F_{SW}	Switching frequency		450	500	550	kHz
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		100		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}	reference voltage	BOOT-SW rising		2.52		V
		Hysteresis		230		mV
T_{SD}	Thermal shutdown threshold*	T_J rising		172		°C
		Hysteresis		12		°C

*Derived from bench characterization
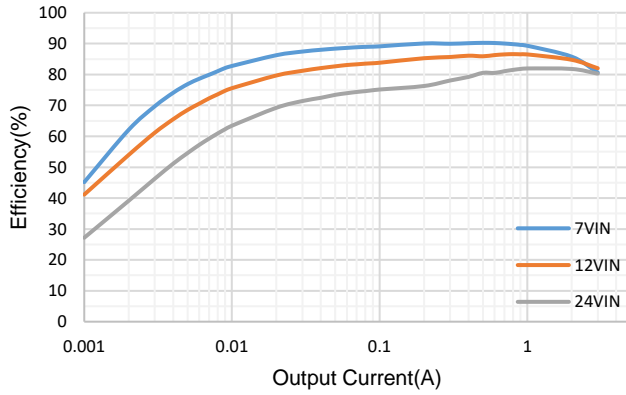
TYPICAL CHARACTERISTICS

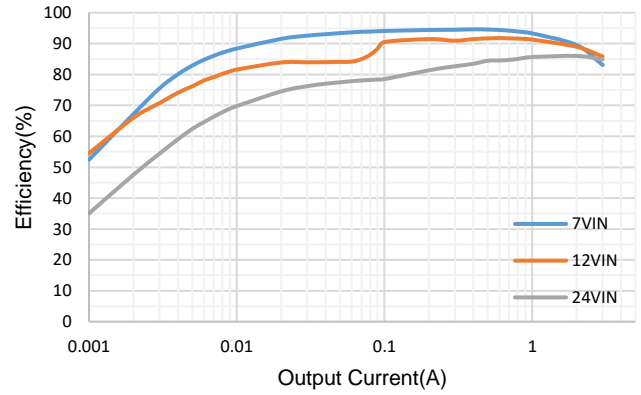Figure 2. Efficiency vs Load Current, Vout=3.3V

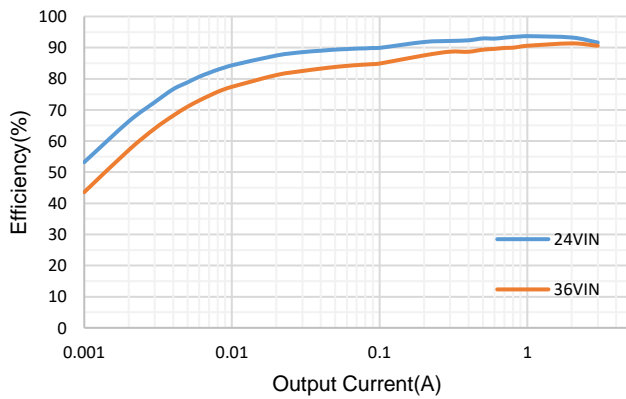Figure 3. Efficiency vs Load Current, Vout=5V

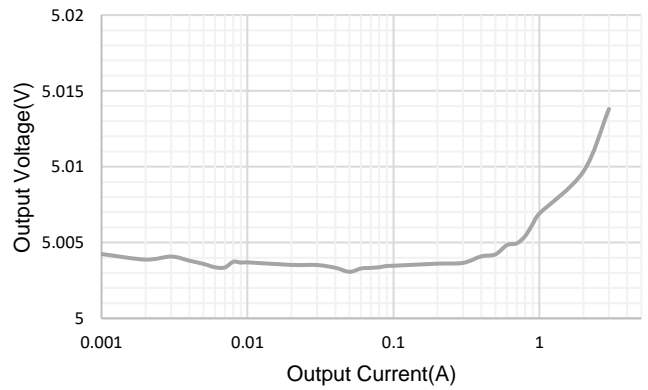Figure 4. Efficiency vs Load Current, Vout=12V
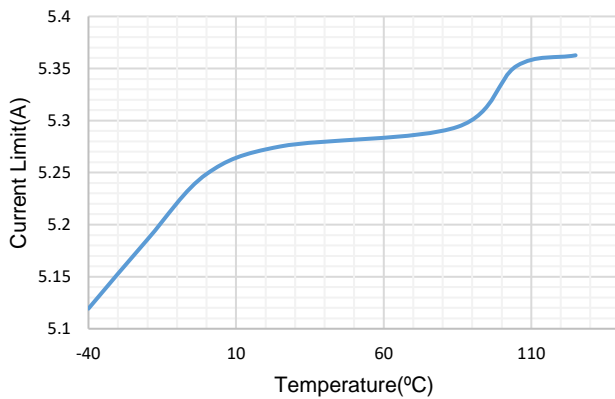
Figure 5. Load Regulation, Vin=24V, Vout=5V

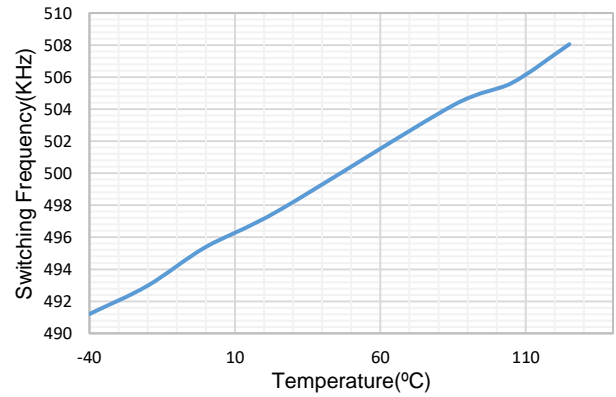Figure 6. Current Limit VS Temperature

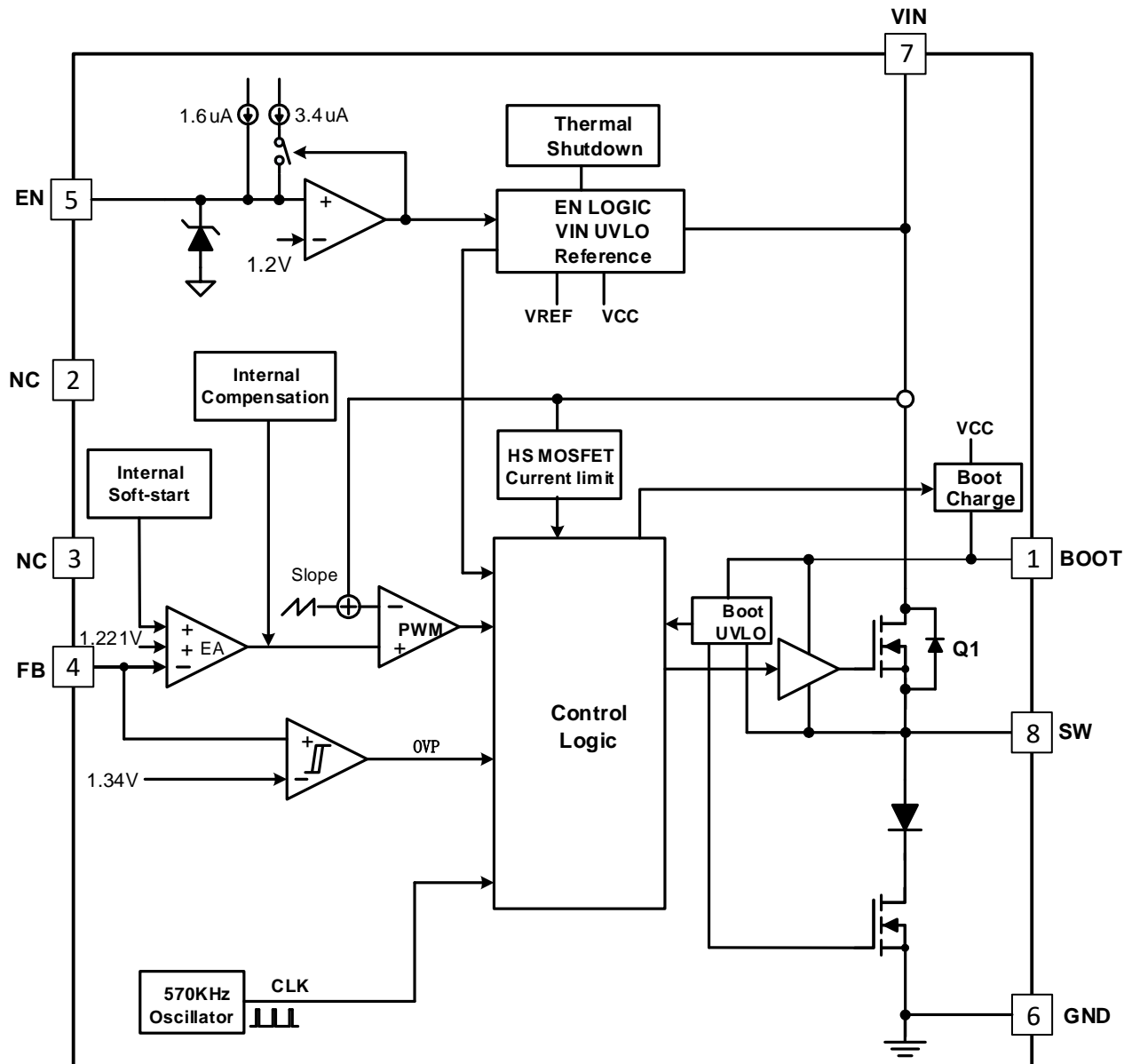Figure 7. Switching Frequency VS Temperature

FUNCTIONAL BLOCK DIAGRAM

Figure 8. Functional Block Diagram

OPERATION

Overview

The LM22676 is a 5.5V-60V input, 3A output, buck converter with integrated 220mΩ Rdson high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response.

The LM22676 features 16ms internal soft-start time to avoid large inrush current and output voltage overshoot during startup and the switching frequency is 500kHz fixed. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 300uA under no load or sleep mode condition to achieve high efficiency at light load.

The LM22676 has a default input start-up voltage of 4.3V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The LM22676 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The LM22676 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 1.221V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The LM22676 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (470mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 200mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 100uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The LM22676 is enabled when the VIN pin voltage rises above 4.3V and the EN pin voltage exceeds the enable threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 3.9V or when the EN pin voltage is below 1V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R1 = \frac{V_{rise} * 0.833 - V_{fall}}{3.667uA} \quad (1)$$

$$R2 = \frac{R_1}{V_{fall} - 1 + R_1 * 5uA} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
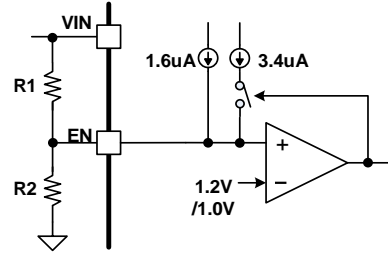- V_{fall} is falling threshold of Vin UVLO

Figure 9. System UVLO by enable divide

Output Voltage

The LM22676 regulates the internal reference voltage at 1.221V with ±2% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF

The UVLO of high-side MOSFET gate driver has rising threshold of 2.5V and hysteresis of 230mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.27V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, LM22676 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.5V. When the voltage from BOOT to SW drops below 2.27V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.5V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the LM22676 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Over Current Limit

The LM22676 implements over current protection with fold back current limit. The LM22676 cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously.

The LM22676 implements frequency foldback to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The LM22676 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency foldback effectively increases the off-time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 6 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to V_{OUT_SHORT}. The selected operating frequency must not exceed the calculated value.

$$f_{sw(\max skip)} = \frac{f_{DIV}}{t_{min\_ON}} \times \left(\frac{I_{LIMIT} \times R_{DC} + V_{OUT\_SHORT} + V_d}{V_{IN\_MAX} - I_{LIMIT} \times R_{DS(on)} + V_d}\right) \tag{4}$$

where

I_{LIMIT}: Limited average current

R_{DC}: Inductor DC resistance

V_{IN_MAX}: Maximum input voltage

V_{OUT_SHORT}: Output voltage during short

V_d: Diode voltage drop

$R_{DS(on)}$: Integrated high side FET on resistance

T_{min_ON}: Controllable minimum on time

f_{DIV}: Frequency divide equals (1,2,4 or 8)

Over voltage Protection

The LM22676 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 1.221V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 1.221V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The LM22676 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 172 ˚C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160 ˚C, the device restarts with soft start phase.

APPLICATION INFORMATION
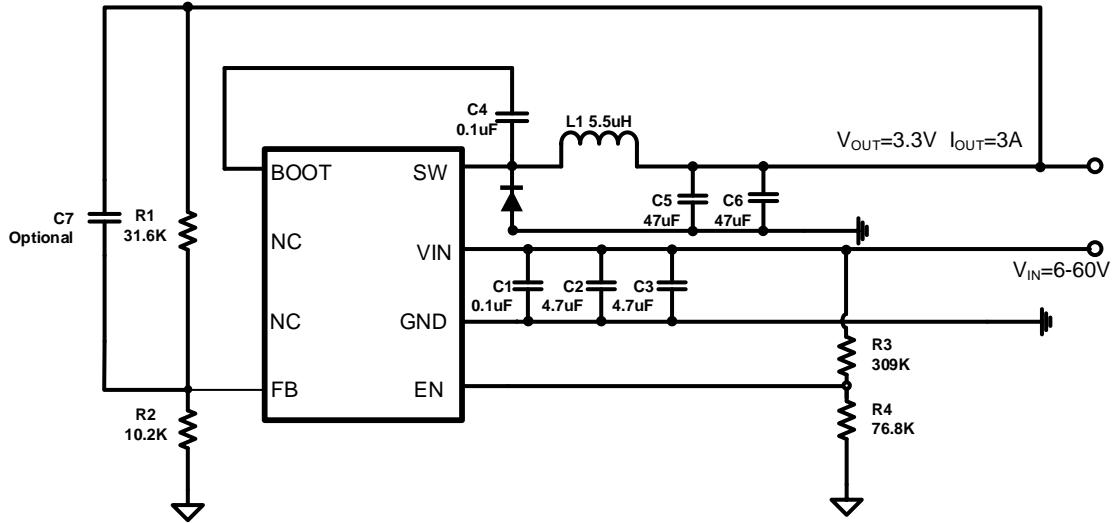
Typical Application

Figure 10. LM22676 **Design Example, 5V Output with Programmable UVLO**

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 6V to 60V
Output Voltage	5V
Maximum Output Current	3A
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	16mV
Transient Response 0.75A to 2.25A load step	∆Vout = 160mV
Start Input Voltage (rising VIN)	5.73V
Stop Input Voltage (falling VIN)	4.045V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 5 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \qquad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.221V

Table 1. R₅, R₆Value for Common Output Voltage (Room T、emperature)

V$_{OUT}$	R$_5$	R$_6$
2.5 V	10.7 KΩ	10.2 KΩ
3.3 V	17.4 KΩ	10.2 KΩ
5 V	31.6 KΩ	10.2 KΩ
12 V	90.9 KΩ	10.2 KΩ
24V	191 KΩ	10.2 KΩ
36V	287 KΩ	10.2 KΩ
48V	383 KΩ	10.2 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.73V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.045 V (stop or disable). Use Equation 6 and Equation 7 to calculate the values 198.5 kΩ and 49.2kΩ of R_1 and R_2 resistors.

$$R1 = \frac{V_{rise} * 0.833 - V_{fall}}{3.667uA} \qquad (6)$$

$$R2 = \frac{R_1}{V_{fall} - 1 + R_1 * 5uA} \qquad (7)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I$_{LPP}$ can be calculated as in Equation 8.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \qquad (8)$$

Where
- I$_{LPP}$ is the inductor peak-to-peak current
- L is the inductance of inductor
- f$_{SW}$ is the switching frequency
- V$_{OUT}$ is the output voltage
- V$_{IN}$ is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \qquad (9)$$

Where
- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 10 and equation 11.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \tag{10}$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \tag{11}$$

Where
- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.75A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.75A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the LM22676 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

The LM22676 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the LM22676.

For the example design, the B360B-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B360B-13-F is 0.7 volts at 3 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 14 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B360B-13-F diode has a junction capacitance of 200 pF. Using Equation 12, the total loss in the diode at the maximum input voltage is 1W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN\_MAX} - V_{OUT}) \times I_{OUT} \times V_d}{V_{IN\_MAX}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_d)^2}{2} \tag{12}$$

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \tag{13}$$

The worst case condition occurs at $V_{IN} = 2 * V_{OUT}$, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \tag{14}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \tag{15}$$

For this example, two 4.7μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}}$$

(16)

Where
- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47μF ceramic output capacitors work for most applications.

Application Waveforms

Vin=24V, Vout=5V, unless otherwise noted
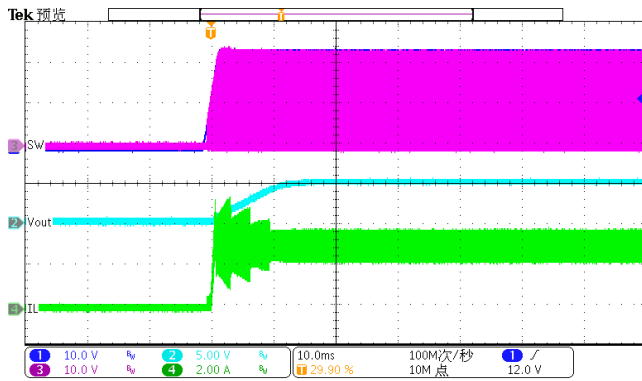
Figure 11. Power up(Iload=3A)
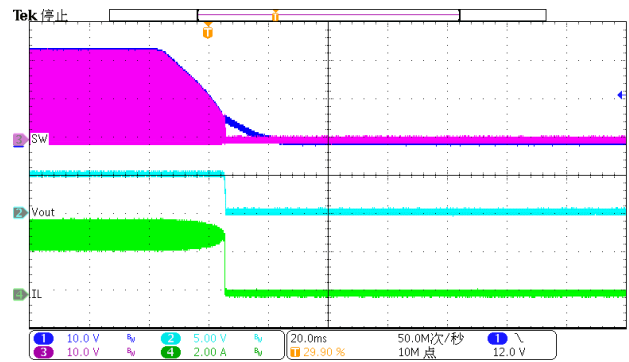
Figure 12. Power down(Iload=3A)
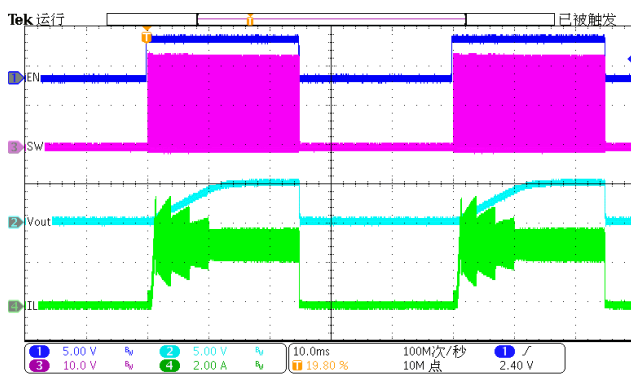
Figure 13.EN toggle (Iload=3A)
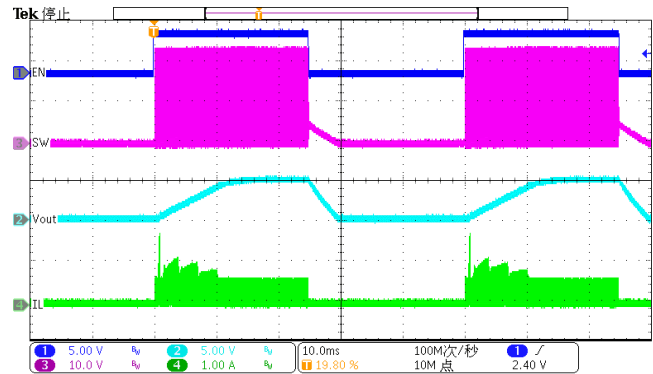
Figure 14. EN toggle (Iload=100mA)
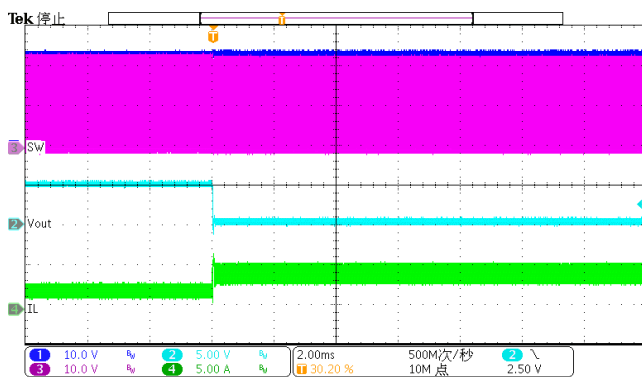
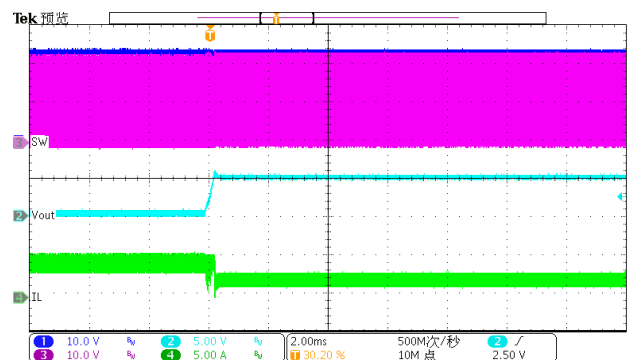Figure 15. Over Current Protection(2A to hard short)

Figure 16. Over Current Release (hard short to 2A)

Application Waveforms(continued)

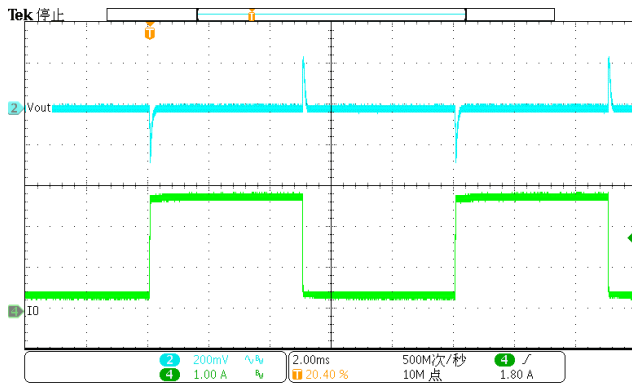Vin=24V, Vout=5V, unless otherwise noted
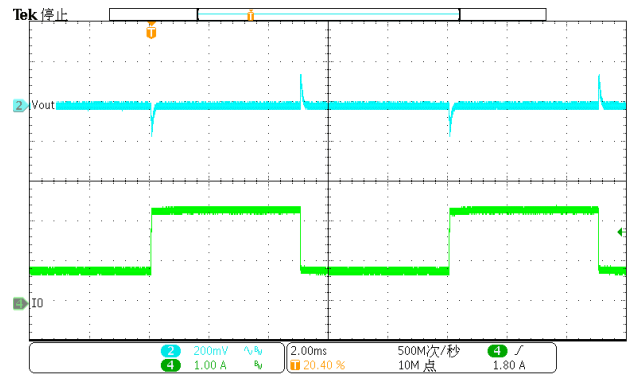

Figure 17. Load Transient (0.3A-2.7A, 1.6A/us)

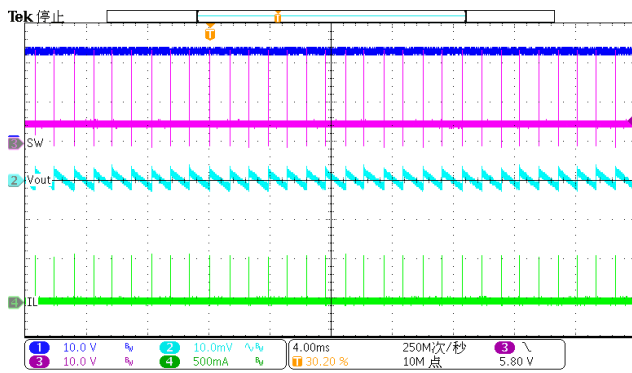Figure 18. Load Transient (0.75A-2.25A, 1.6A/us)

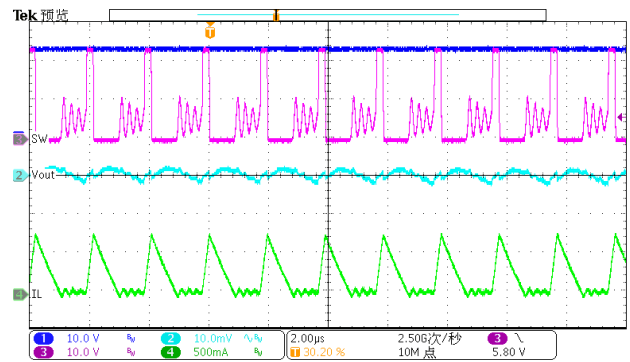Figure 19. Output Ripple (Iload=0A)

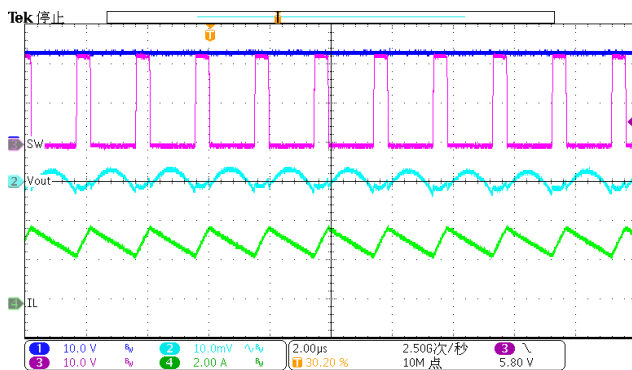Figure 20. Output Ripple (Iload=200mA)

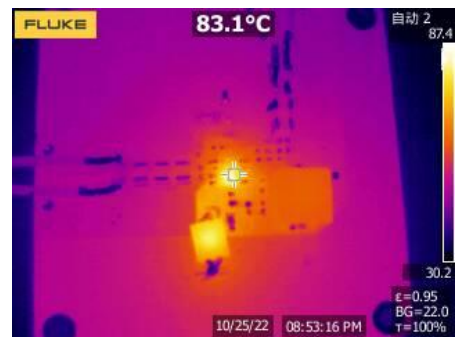Figure 21. Output Ripple (Iload=3A)

Figure 22. Thermal, 24VIN, 5Vout, 3A

Layout Guideline

Proper PCB layout is a critical for LM22676's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.

3. Freewheeling diode should be place as close to SW pin and the ground as possible to reduce parasitic effect.

4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

6. Output inductor and freewheeling diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

7. UVLO adjust resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

8. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.

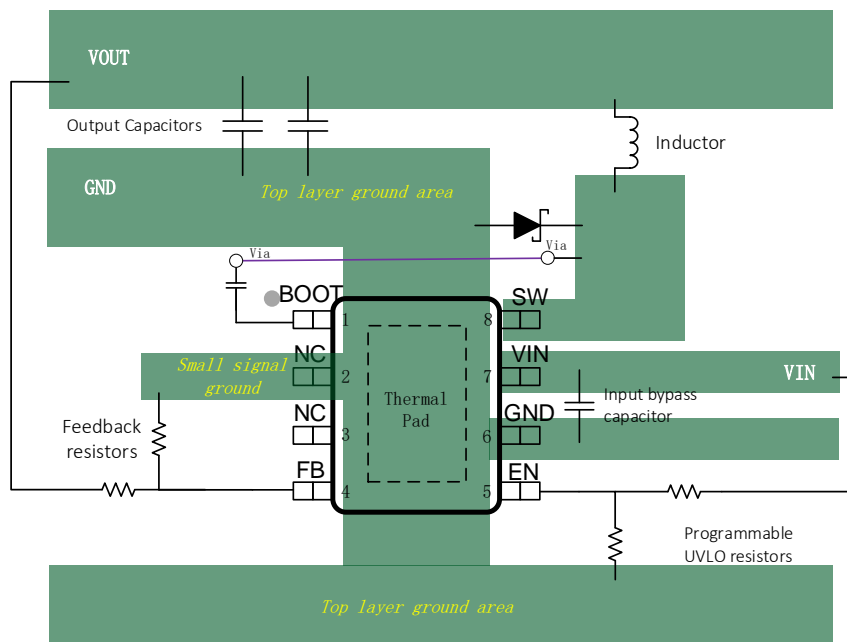9. For achieving better thermal performance, a four-layer layout is strongly recommended.
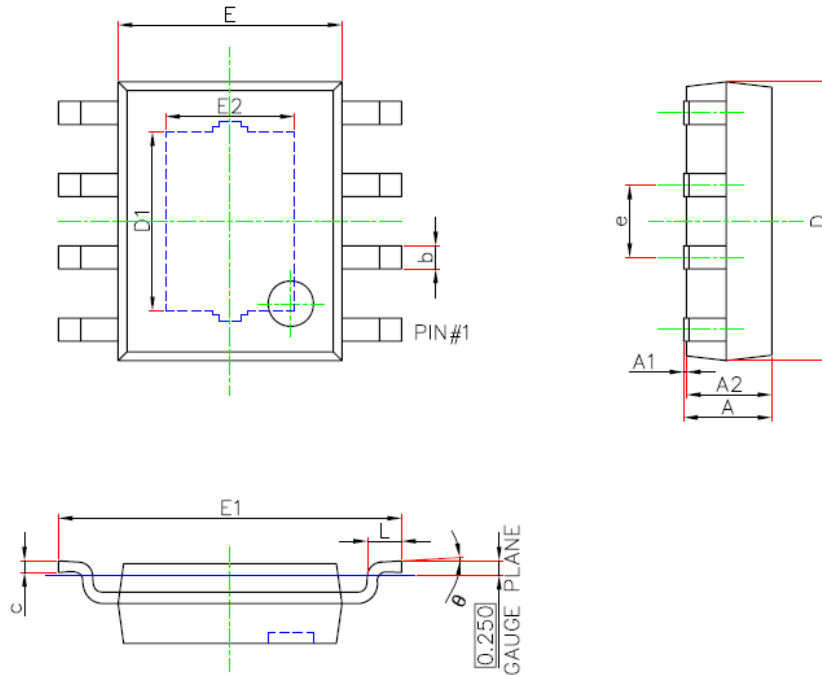

Figure 23. PCB Layout Example

PACKAGE INFORMATION

SOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
LM22676MRX	SOP-8-EP	8	4000