3.75kVrms /5.0kVrms Isolated Single Channel Gate Driver

FEATURES

Feature options

- Split outputs 1EDI60N12A
- Miller clamp 1EDI60N12C

6A peak source and sink drive current
2.5V to 5.5V input supply voltage
Up to 33V driver supply voltage
8V and 12V UVLO options
3.75kVrms and 5.0kVrms isolation voltage
100kV/us minimum CMTI
51ns typical propagation delay
CMOS inputs
Operating temperature range: -40°C to 125°C
RoHS-compliant, NB SOIC-8 and WB SOIC-8 package

APPLICATIONS

Switched-Mode Power Supplies
EV/HEV Inverters and DC/DC Converters
Solar Inverters
Motor Control
UPS and PSU

Device Information

PART SERIES	UVLO	PIN CONFIGURATION
1EDI60N12A	8V	Split output
1EDI60N12C	12V	Miller clamp

FUNCTIONAL BLOCK DIAGRAMS

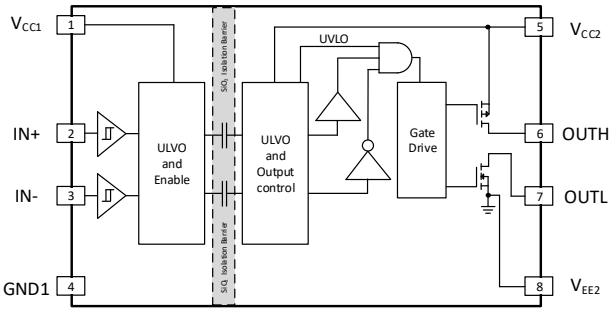


Figure1. 1EDI60N12A *Functional Block Diagrams*

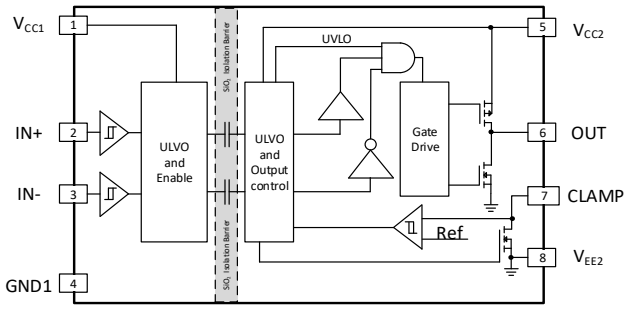


Figure2. 1EDI60N12C *Functional Block Diagrams*

PIN CONFIGURATIONS AND FUNCTIONS

Table1. 1EDI60N12A Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V_{CC1}	P	Input power supply
2	IN+	I	Positive input
3	IN-	I	Negative input
4	GND1	G	Input ground
5	V_{CC2}	P	Output power supply
6	OUTH	O	Pull high output
7	OUTL	O	Pull low output
8	V_{EE2}	G	Output ground

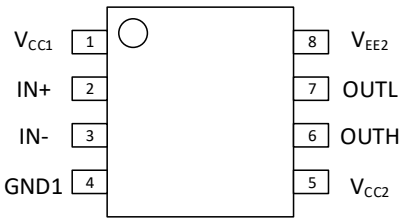


Figure3. 1EDI60N12A *Pin Configuration*

Table2.1EDI60N12C Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V_{CC1}	P	Input power supply
2	IN+	I	Positive input
3	IN-	I	Negative input
4	GND1	G	Input ground
5	V_{CC2}	P	Output power supply
6	OUT	O	Gate drive output
7	CLAMP	O	Active miller clamp
8	V_{EE2}	G	Output ground

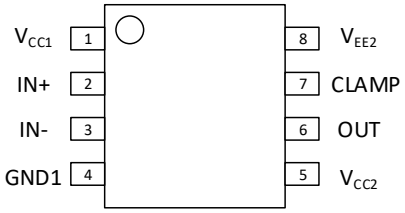


Figure4. 1EDI60N12C *Pin Configuration*

SPECIFICATIONS

Absolute Maximum Ratings

Table3.1EDI60N12x Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

DESCRIPTION		MIN	MAX	UNIT
V_{CC1}	Input supply voltage (reference to GND1)	-0.3	7	V
V_{In+}/V_{In-}	Signal input voltage	-0.3	V_{CC1}+0.3	V
V_{CC2}	Output supply voltage (reference to V_{EE2})	-0.3	36	V
Output signal voltage	V_{OUTH}-V_{EE2}, V_{OUTL}-V_{EE2}, V_{OUT}-V_{EE2}, V_{CLAMP}-V_{EE2}	V_{EE2}-0.3	V_{CC2}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

ESD Rating

Table4. 1EDI60N12x ESD Ratings

DESCRIPTION		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-6000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-2000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Table5.1EDI60N12x Recommended Operating Conditions

DESCRIPTION		MIN	MAX	UNIT
V_{CC1}	Input supply voltage	2.5	5.5	V
V_{In+}/V_{In-}	Input side signal voltage	0	V_{CC1}	V
V_{CC2}	Output supply voltage for 60N12A	9.5	33	V
V_{CC2}	Output supply voltage for 60N12C	13.2	33	V

DESCRIPTION		MIN	MAX	UNIT
T_A	Ambient temperature	-40	125	°C

Truth Table

Table6. 1EDI60N12A Truth Table

V_{CC1}	IN+	IN-	V_{CC2}	OUTH	OUTL
above UVLO	L[(1)] or floating	X	above UVLO	Hi-Z	L
above UVLO	H	H or floating	above UVLO	Hi-Z	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	Hi-Z	L
below UVLO	X	X	X	Hi-Z	L

(1) L = Logic Low, H = Logic High, X = H, L or floating, Hi-Z = High impedance.

Table7. 1EDI60N12C Truth Table

V_{CC1}	IN+	IN-	V_{CC2}	OUT	CLAMP
above UVLO	L[(1)] or floating	X	above UVLO	L	L
above UVLO	H	H or floating	above UVLO	L	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	L	L
below UVLO	X	X	X	L	L

(1) L = Logic Low, H = Logic High, X = H, L or floating, Hi-Z = High impedance.

Thermal Information

Table8. 1EDI60N12x Thermal Information

PACKAGE THERMAL RATINGS	NB SOIC-8	WB SOIC-8	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	110	100	°C/W
Ψ_{JT} Junction–to-top characterization parameter	18	16	°C/W

Supply Power Ratings

Table9. 1EDI60N12x NB SOIC-8 Package Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation on input and output	V_{CC1} = 5V, V_{CC2} = 15V, f = 1.8MHz, 50% duty cycle, square wave, 2.2nF load			1.14	W
P_{D1} Maximum input power dissipation				0.01	W
P_{D2} Maximum output power dissipation				1.13	W

Table10. 1EDI60N13x WB SOIC-8 Package Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation on input and output	V_{CC1} = 5V, V_{CC2} = 15V, f = 2.0MHz, 50% duty cycle, square wave, 2.2nF load			1.26	W
P_{D1} Maximum input power dissipation				0.01	W
P_{D2} Maximum output power dissipation				1.25	W

Electrical Specifications

Table11.1EDI60N12x Electrical Specifications

V_{CC1} = 2.5V or 3.3V or 5V, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1nF. T_A = –40°C to 125°C (Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS					
I_{VCC1} V_{CC1} quiescent current	V_{IN-} = 0V, V_{IN+} = 0V		0.8	1.2	mA
I_{VCC2} V_{CC2} quiescent current	V_{IN-} = 0V, V_{IN+} = 0V		1.8	2.7	mA
SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS					
$V_{UV+(VCC1)}$	V_{VCC1} under voltage rising threshold	2.10	2.25	2.40	V
$V_{UV-(VCC1)}$	V_{VCC1} under voltage falling threshold	2.00	2.10	2.20	V
$V_{HYS(VCC1)}$	V_{VCC1} UVLO threshold hysteresis	0.10	0.15		V
60N12A DRIVER SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS					
$V_{UV+(VCC2)}$	V_{VCC2} under voltage rising threshold		8.4	9.4	V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UV-(VCC2)}$	V_{VCC2} under voltage falling threshold	7.1	7.8		V
$V_{HYS(VCC2)}$	V_{VCC2} UVLO threshold hysteresis		0.6		V
60N12C DRIVER SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS					
$V_{UV+(VCC2)}$	V_{VCC2} under voltage rising threshold		12	13	V
$V_{UV-(VCC2)}$	V_{VCC2} under voltage falling threshold	9.8	10.8		V
$V_{HYS(VCC2)}$	V_{VCC2} UVLO threshold hysteresis		1.2		V
INPUT					
V_{INH} Input rising threshold			0.50*V_{CC1}	0.60*V_{CC1}	V
V_{INL} Input falling threshold		0.30*V_{CC1}	0.35*V_{CC1}		V
V_{HYS}			0.15*V_{CC1}		
OUTPUTS (60N12A ONLY)					
I_{OH}/I_{OL} Peak source and sink current	C_{LOAD} = 0.22uF, without external current limiting resistors, 1kHz switching frequency	6	10		A
V_{OH} High-level output voltage (V_{CC2}-V_{OUTH})	I_{OUTH} = –20mA		100	150	mV
V_{OL} Low-level output voltage (V_{OUTL}-V_{EE2})	I_{OUTL} = 20mA		7.5	11.5	mV
OUTPUTS (60N12C ONLY)					
I_{OUT} Peak source current	C_{LOAD} = 0.22uF, without external current limiting resistors, 1kHz switching frequency	6	10		A
V_{OUTH} High-level output voltage (V_{CC2}-V_{OUT})	I_{OUT} = –20mA		100	150	mV
V_{OUTL} Low-level output voltage (V_{OUT}-V_{EE2})	I_{OUT} = 20mA		7.5	11.5	mV
ACTIVE MILLER CLAMP (60N12C ONLY)					
V_{CLAMP} Low level clamp voltage	I_{CLAMP} = 20mA		7	10	mV
I_{CLAMP} Clamp low level current	V_{CLAMP} = V_{EE2} + 15V	6	10		A
$V_{CLAMP-TH}$ Clamp threshold voltage	IN+ = high, IN- = low		2.1	2.3	V
SHORT CIRCUIT CLAMPING (60N12C ONLY)					
$V_{CLP-OUT}$ Clamping voltage (V_{OUT}-V_{CC2})	IN+ = high, IN- = low, t_{CLAMP} = 10us, I_{OUT} = 500mA		1.0	1.3	V
$V_{CLP-OUT}$ Clamping voltage (V_{EE2}-V_{CLAMP})	IN+ = low, IN- = high, I_{CLAMP} = -20mA		0.9	1.0	V
ACTIVE PULLDOWN (60N12C ONLY)					
V_{OUTSD} Active pulldown voltage on CLAMP	I_{OUT} = 0.1 x $I_{OUTL(typ)}$, V_{CC2} = open		1.8	2.5	V
TIMING					
t_{PLH} Propagation delay, high(1)	C_{LOAD} = 1.8nF		51	65	ns
t_{PHL} Propagation delay, low(1)	C_{LOAD} = 1.8nF		51	65	ns
t_{PWD} Pulse width distortion	C_{LOAD} = 1.8nF		1	10	ns
t_r Rise time(2)	C_{LOAD} = 1.8nF		8	15	ns
t_f Fall time(2)	C_{LOAD} = 1.8nF		7	12	ns
CMTI	Common-mode transient immunity(3)	100			kV/us

(1) t_{PLH} = low-to-high propagation delay time, t_{PHL} = high-to-low propagation delay time. See Figure22.
(2) t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal. See Figure21.
(3) See Figure28 for Common-mode transient immunity (CMTI) measurement.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Insulation Specifications

Table12. 1EDI60N12x Insulation Specifications

PARAMETER	SYMBOL	VALUE		UNIT	TEST CONDITIONS/COMMENTS
		NB SOIC-8	WB SOIC-8		
Rated dielectric insulation voltage		3750	5000	Vrms	1-minute duration
Minimum external air gap (Clearance)	L (CLR)	≥4	≥8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum external tracking (Creepage)	L (CRP)	≥4	≥8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum internal gap (Internal clearance)		≥21	≥21	µm	Insulation distance through insulation
Tracking resistance (Comparative tracking index)	CTI	>400	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material group		II	II		According to IEC 60664-1

Package Specifications

Table13. 1EDI60N12x Package Specifications

PARAMETER	SYMBOL	TYPICAL VALUE	UNIT	TEST CONDITIONS/COMMENTS
Resistance (Input to Output)(1)	R_{I-O}	>10 ^{12}	Ω	T_A = 25°C
Capacitance (Input to Output)(1)	C_{I-O}	1.5	pF	@ 1MHz
Input Capacitance(2)	C_I	3	pF	@ 1MHz

(1) The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 are shorted together as the other terminal.

(2) Testing from the input signal pin to ground.

VDE Insulation Characteristics

Table14. VDE Insulation Characteristics

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC		Unit
			1EDI60N12x NB SOIC-8	1EDI60N13x WB SOIC-8	
Overvoltage category per IEC 60664-1	For rated mains voltage ≤ 150Vrms For rated mains voltage ≤ 300Vrms For rated mains voltage ≤ 600Vrms For rated mains voltage ≤ 1000Vrms		I to IV I to III NA NA	I to IV I to IV I to III I to II	
Climatic category			40/125/21	40/125/21	
Pollution degree			2	2	
Maximum repetitive peak isolation voltage		V_{IORM}	1200	1200	Vpeak
Input to output test voltage, method B1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, 100% production test, $t_{ini} = t_m$ = 1sec, partial discharge < 5pC	$V_{pd\,(m)}$	1800	1800	Vpeak
Input to output test voltage, method A After environmental tests subgroup 1 After input and/or safety test subgroup 2 and subgroup 3	 $V_{IORM} \times 1.3 = V_{pd\,(m)}$, t_{ini} = 60sec, t_m = 10sec, partial discharge < 5pC $V_{IORM} \times 1.2 = V_{pd\,(m)}$, t_{ini} = 60sec, t_m = 10sec, partial discharge < 5pC	$V_{pd\,(m)}$	 1560 1440	 1560 1440	 Vpeak Vpeak
Highest allowable overvoltage		V_{IOTM}	5300	7071	Vpeak
Surge isolation voltage basic	Basic insulation, 1.2/50 µs combination wave, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	V_{IOSM}	5000	5000	Vpeak
Safety limiting values	Maximum value allowed in the event of a failure (see Figure6)				
Maximum safety temperature		T_S	150	150	°C
Maximum power dissipation at 25°C		P_S	1.14	1.26	W
Insulation resistance	V_{IO} = 500V at T_A = 25°C	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	V_{IO} = 500V at T_S = 150°C	R_{IO}	$>10^{9}$	$>10^{9}$	Ω

V_{CC1} = 2.5V or 3.3V or 5V, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1nF. T_A = –40°C to 125°C (Unless otherwise noted).

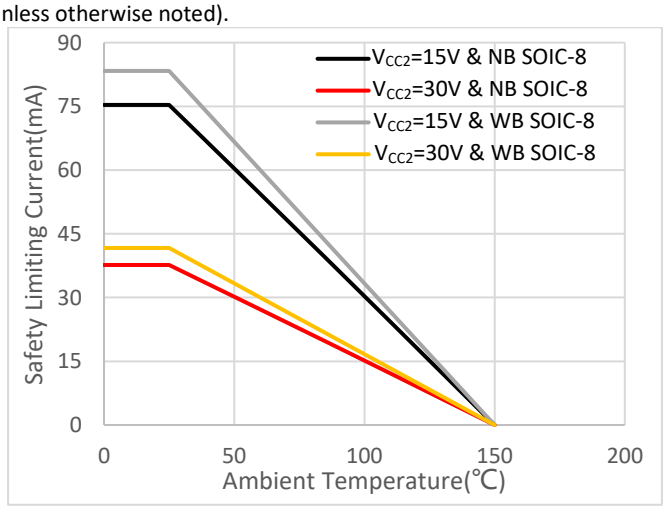


Figure5. NB/WB SOIC-8 Thermal Derating Curve For Limiting Current With Ambient Temperature Per VDE

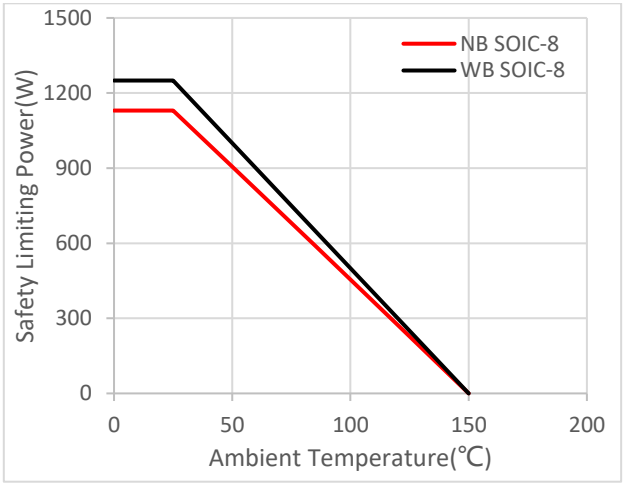


Figure6. NB/WB SOIC-8 Thermal Derating Curve For Limiting Power With Ambient Temperature Per VDE

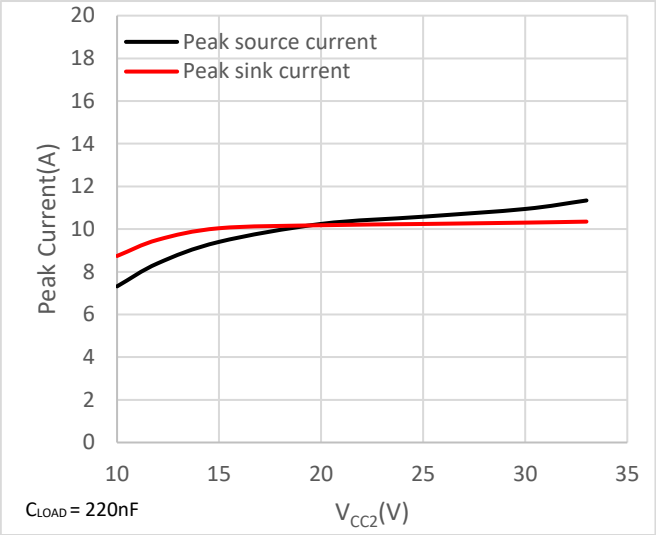


Figure7. Output High Drive Current Vs V_{CC2}

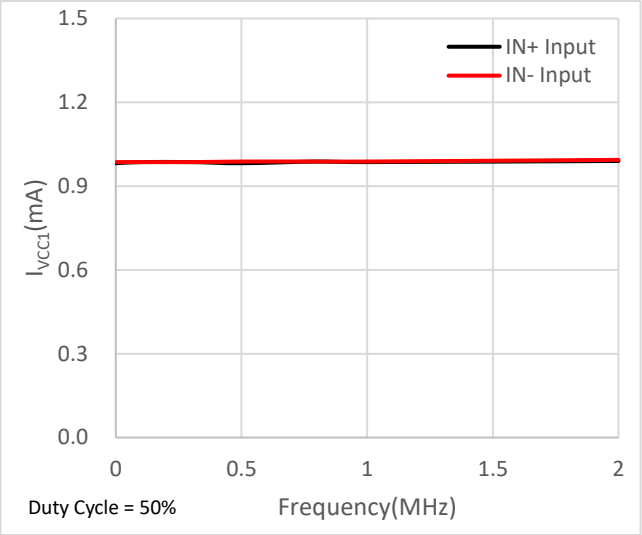


Figure8. I_{VCC1} Supply Current Vs Input Frequency

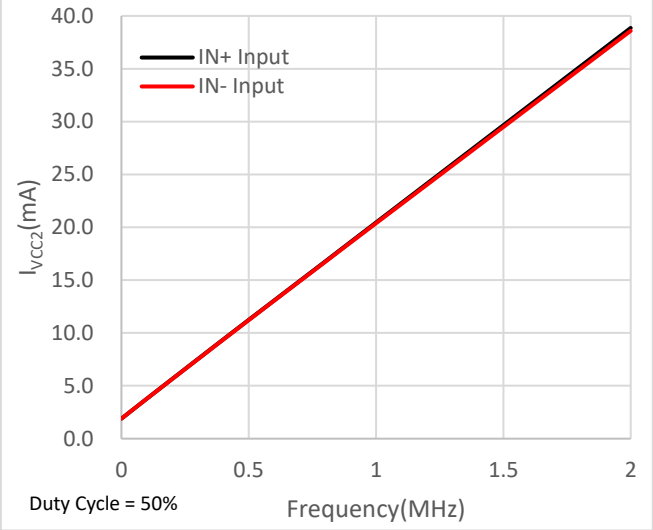


Figure9. I_{VCC2} Supply Current Vs Input Frequency

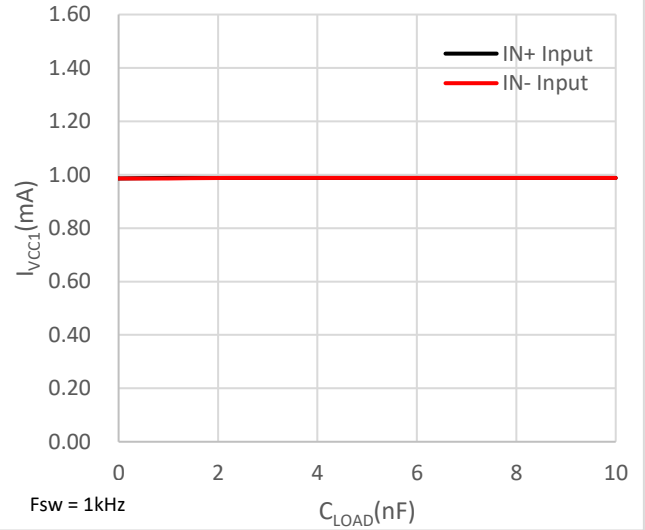


Figure10. I_{VCC1} Supply Current Vs Load Capacitance

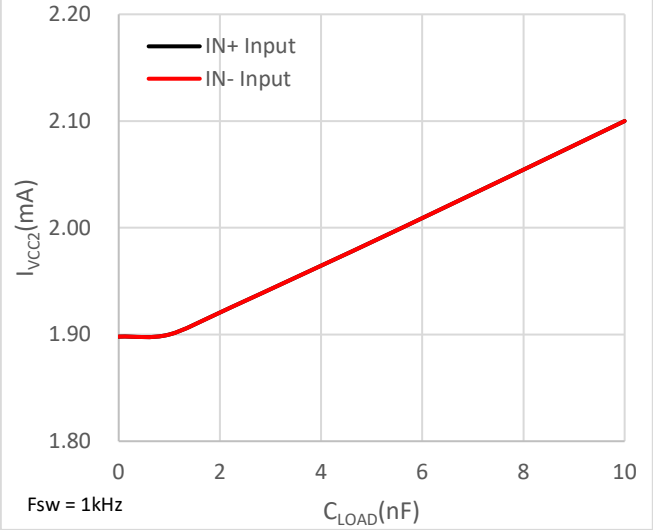


Figure11. I_{VCC2} Supply Current Vs Load Capacitance

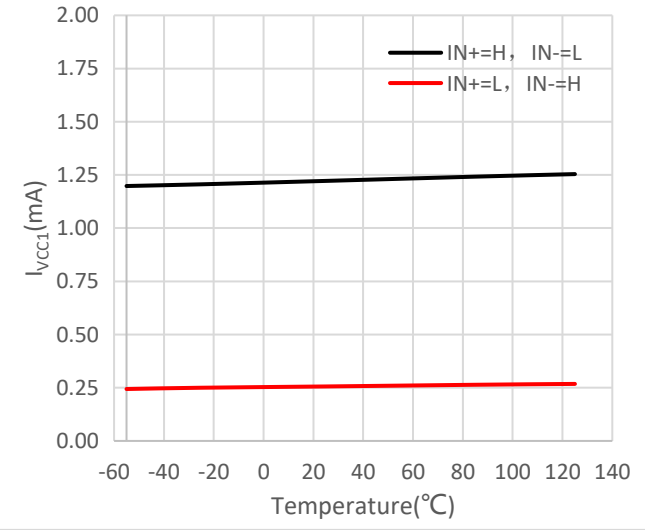


Figure12. I_{VCC1} Supply Current Vs Ambient Temperature

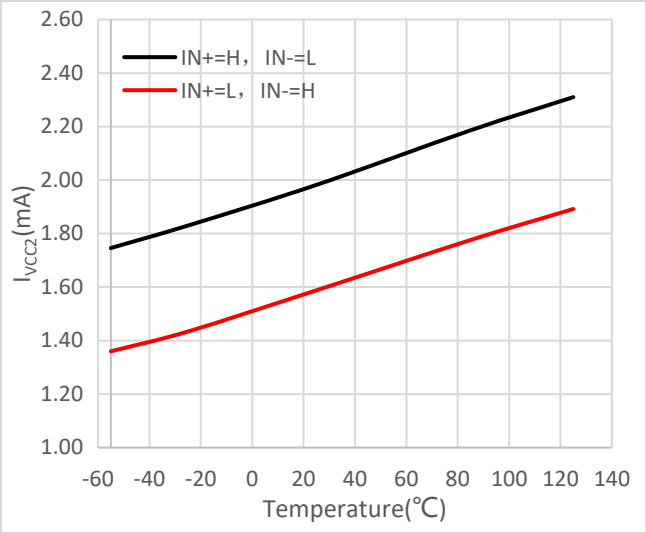


Figure13. I_{VCC2} Supply Current Vs Ambient Temperature

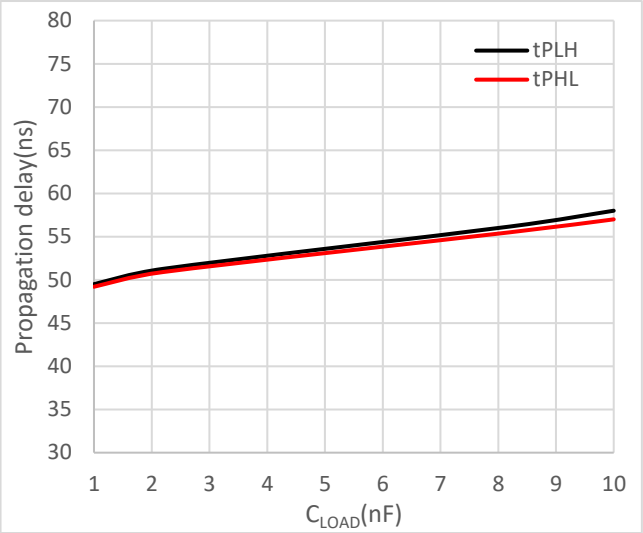


Figure14. Propagation Delay Vs Load Capacitance

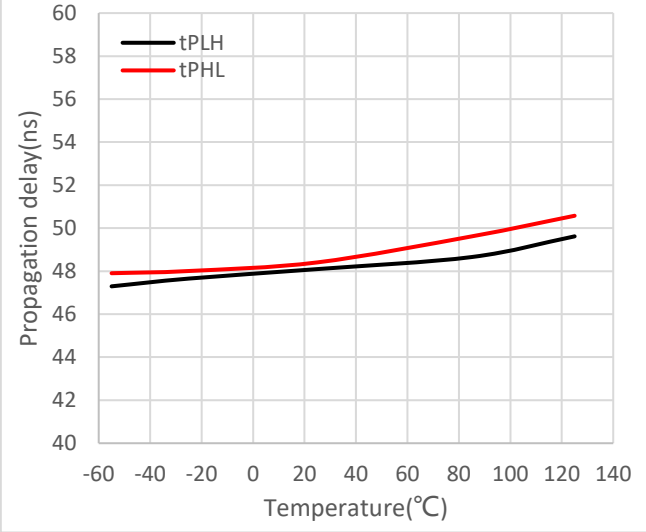


Figure15. Propagation Delay Vs Ambient Temperature

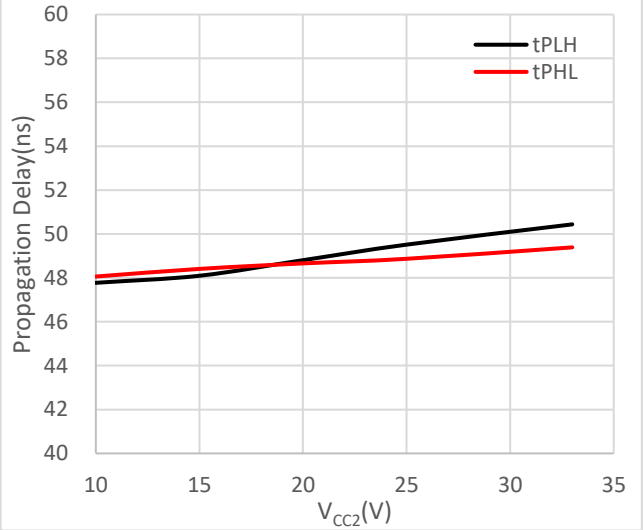


Figure16. Propagation Delay Vs V_{CC2}

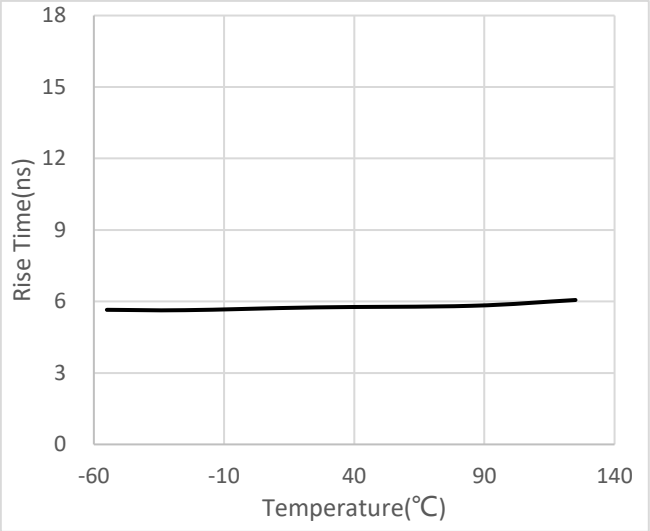


Figure17. Rise Time Vs Ambient Temperature

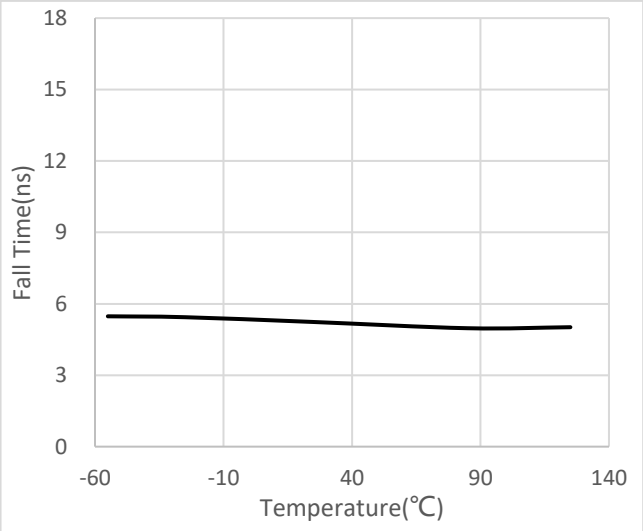


Figure18. Fall Time Vs Ambient Temperature

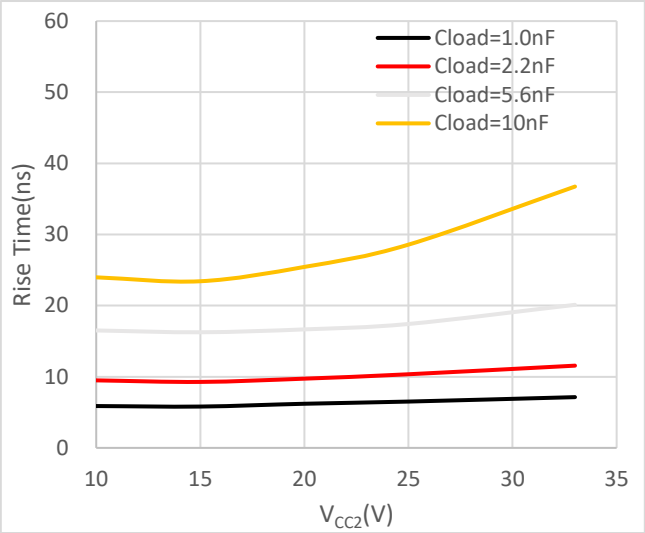


Figure19. Rise Time Vs C_{LOAD} And V_{CC2}

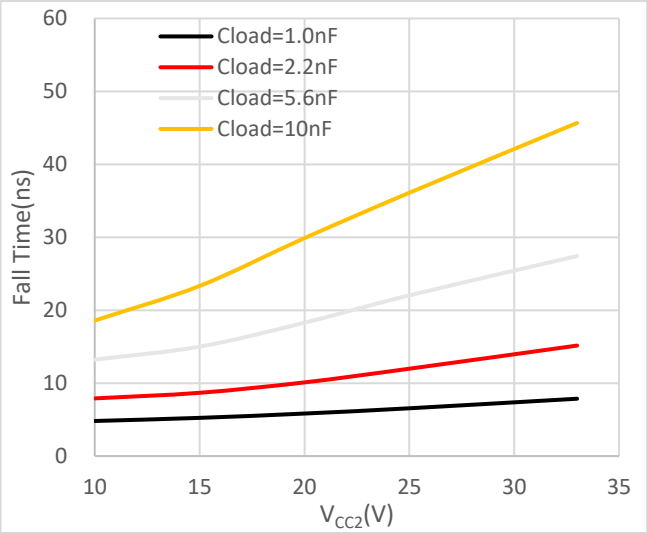


Figure20. Fall Time Vs C_{LOAD} And V_{CC2}

TIMING TEST INFORMATION

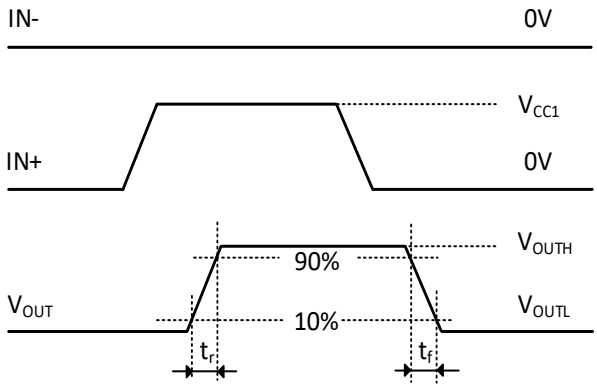


Figure21. Transition Time Waveform Measurement

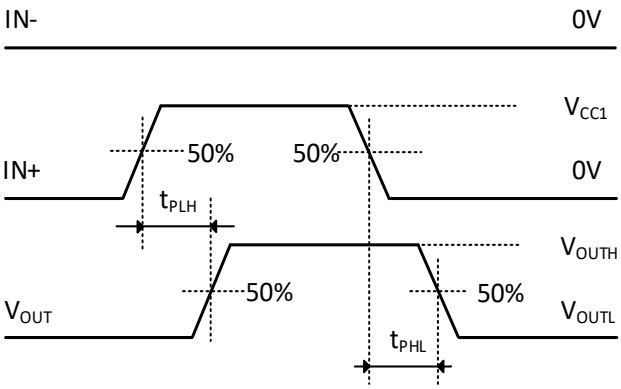


Figure22. Propagation Delay Time Waveform Measurement

APPLICATIONS INFORMATION

Typical Application

The circuit figure below is a typical application for driving IGBTs.

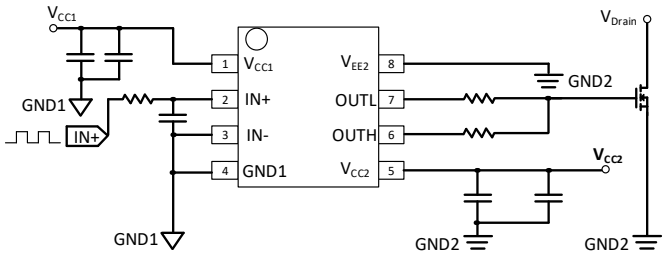


Figure23. 60N12A Typical Application Circuit (IN+ Input)

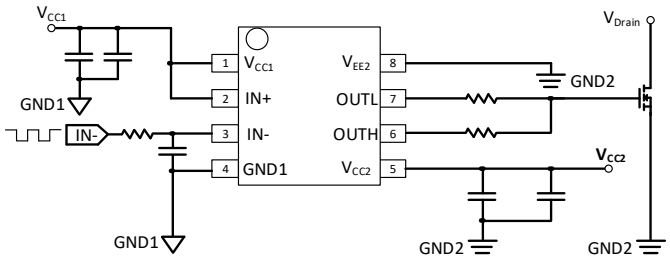


Figure24. 60N12A Typical Application Circuit (IN- Input)

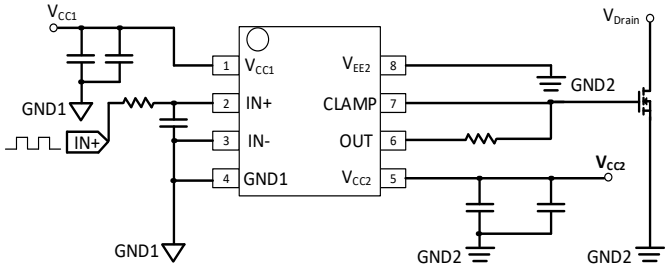


Figure25. 60N12C Typical Application Circuit (IN+ Input)

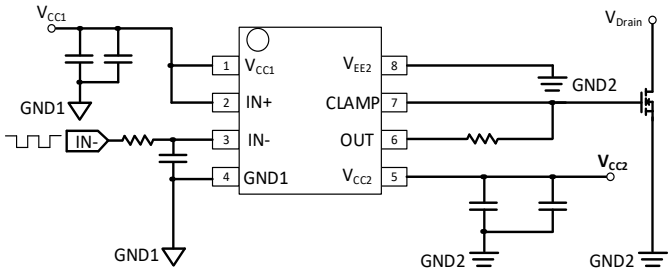


Figure26. 60N12C Typical Application Circuit (IN- Input)

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{CC1} and GND1 and between V_{CC2} and V_{EE2}. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value between V_{CC1} and GND1 is between 0.1µF and 1µF, bypass capacitor value between V_{CC2} and V_{EE2} is between 1µF and 10µF. Additional 100nF capacitor in parallel with the isolator device bypass capacitor is recommended for high frequency filtering.

To avoid large negative transients on the V_{EE2} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To avoid reducing the isolation capability, keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

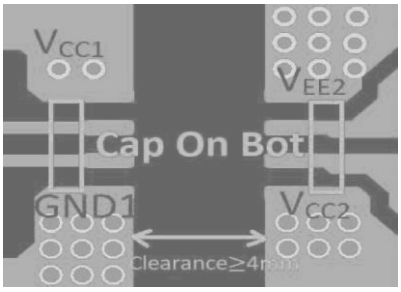


Figure27. Layout Example

MILLER CLAMP (60N12C ONLY)

The active Miller-clamp function is used to prevent false turn-on of the power switches caused by Miller current with applications where a unipolar power supply is used. Low impedance path between the power-switch gate terminal and Miller clamp pins to sink the Miller current is available for the active Miller-clamp function implemented. Witch the Miller-clamp function, the power-switch gate voltage is clamped to less than 2V during the off state.

The 60N12C provides short-circuit clamping function to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the V_{CC2} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the V_{CC2} pin inside the driver. The internal diodes can conduct up to 500mA current for a duration of 10µs, and a continuous current of 20mA. To improve current conduction capability can use external schottky diodes if needed.

The active pulldown function is used to pull the IGBT or MOSFET gate to the low state, when no power is connected to the V_{CC2} supply. This feature prevents IGBT and MOSFET false turn-on on the OUT and CLAMP pins by clamping the output voltage to approximately 2V.

Figure25 and Figure26 show a typical application circuit of 60N12C.

CMTI MEASUREMENT

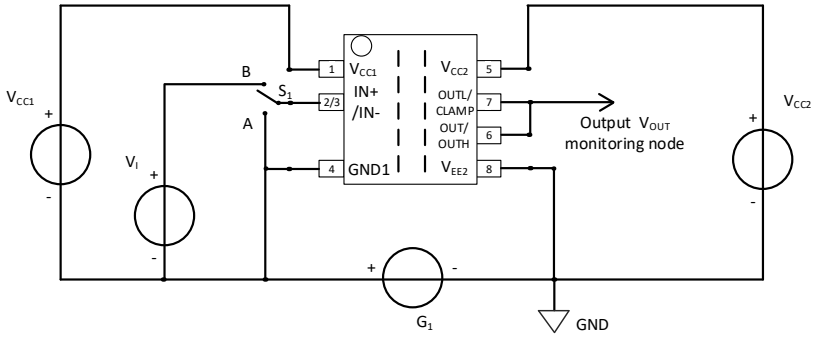
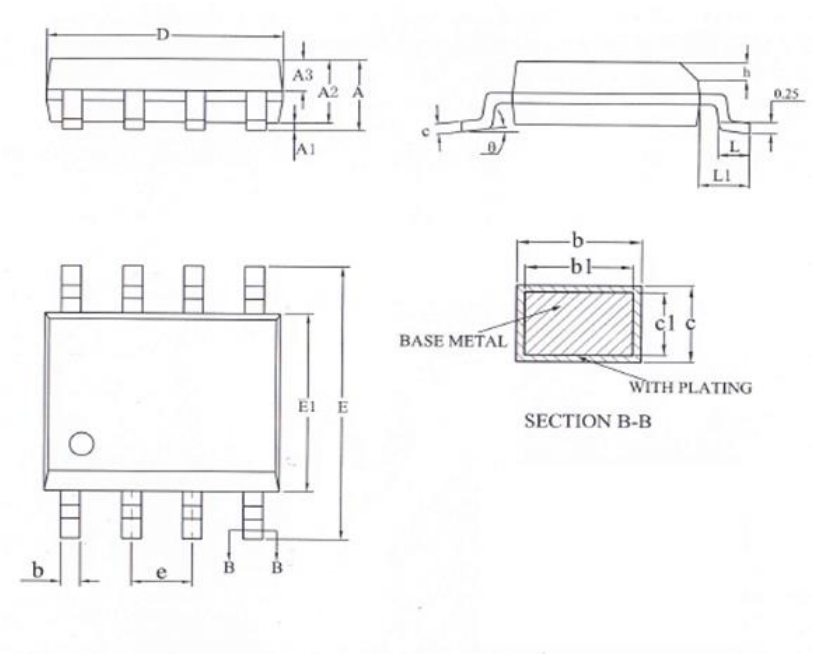


Figure28. Common-mode Transient Immunity (CMTI) Measurement

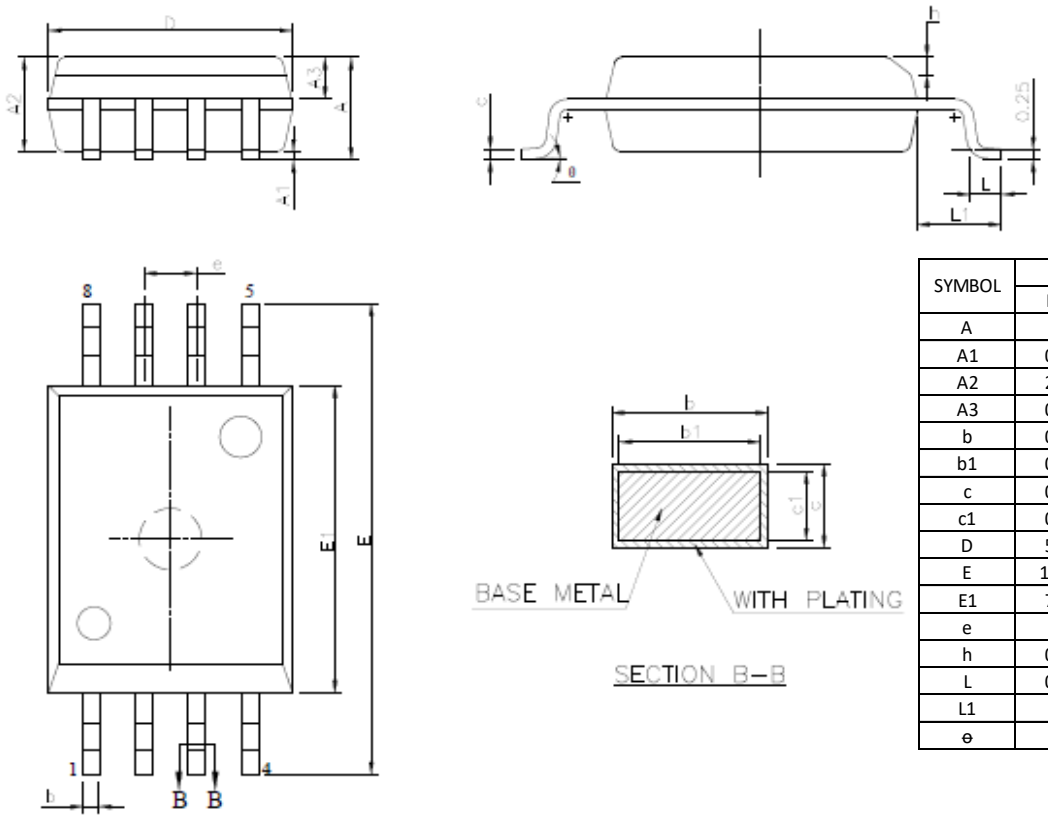
Common-Mode Transient Immunity (CMTI) can be measured, under specified common-mode pulse magnitude (VCM), and specified slew rate of the common-mode pulse (dVCM/dt). The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM), such that the maximum common-mode slew rates (dVCM/dt) can be applied to 60N12x isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground V_{EE2} of 60N12x isolated gate driver, with positive transients as well as negative transients.

OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

Figure29. 8-Lead Narrow Body SOIC [NB SOIC-8] *Outline Package–Dimension Unit(mm)*

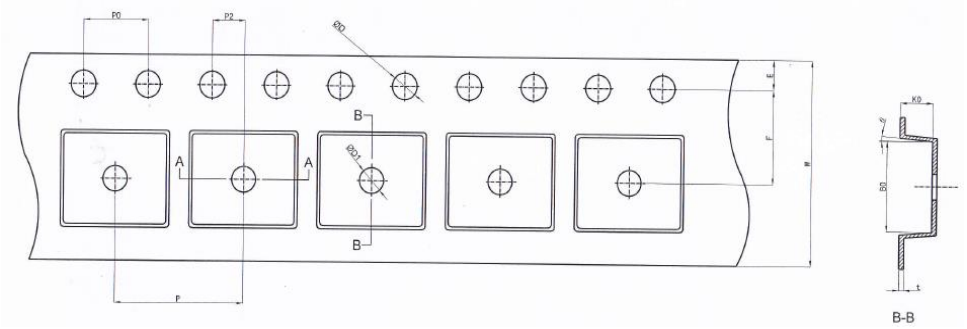


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	1.00
L1	2.00REF		
θ	0	-	8°

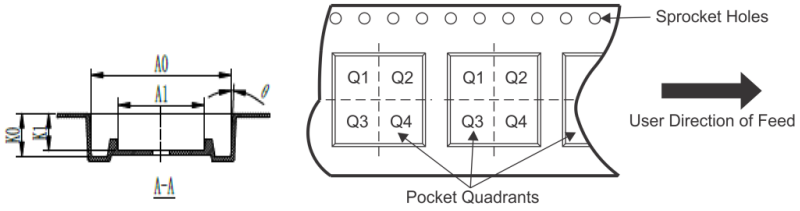
Figure30. 8-Lead Wide Body SOIC [WB SOIC-8] *Outline Package–Dimension Unit(mm)*

REEL INFORMATION

8-Lead Narrow Body SOIC [NB SOIC-8]



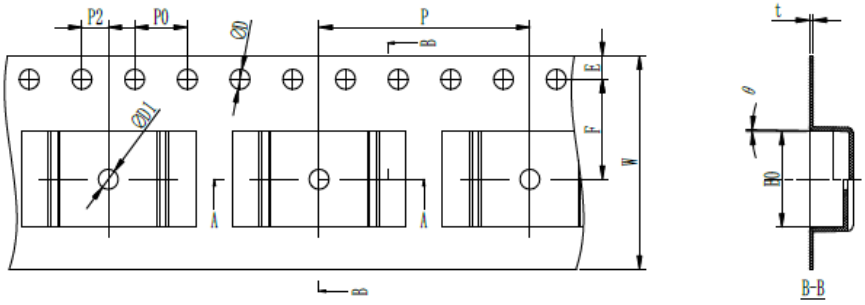
COMMON SIZE		POCKET SIZE	
APPEARANCE	DIMENSION(MM)	APPEARANCE	DIMENSION(MM)
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10	t	0.30±0.05
10P0	40.0±0.20	θ	3° TYP



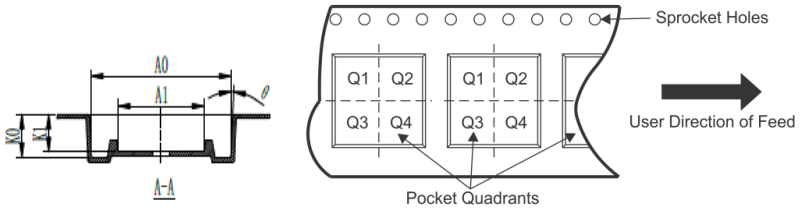
Note: The pin1 of the chip is in the quadrant Q1

Figure33. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information–*Dimension Unit(mm)*

8-Lead Wide Body SOIC [WB SOIC-8]



COMMON SIZE		POCKET SIZE	
APPEARANCE	DIMENSION(MM)	APPEARANCE	DIMENSION(MM)
E	1.75±0.10	W	16.00±0.30
F	7.50±0.10	P	16.00±0.10
P2	2.00±0.10	A0	11.98±0.10
D	$1.50^{+0.1}_{0}$	A1	7.37±0.10
D1	$1.50^{+0.1}_{0}$	B0	6.11±0.10
P0	4.00±0.10	K0	3.00±0.10
10P0	40.0±0.20	K1	2.60±0.10
		t	0.3±0.05
		θ	5° TYP



Note: The pin1 of the chip is in the quadrant Q1

Figure34. 8-Lead Wide Body SOIC [WB SOIC-8] Reel Information–*Dimension Unit(mm)*