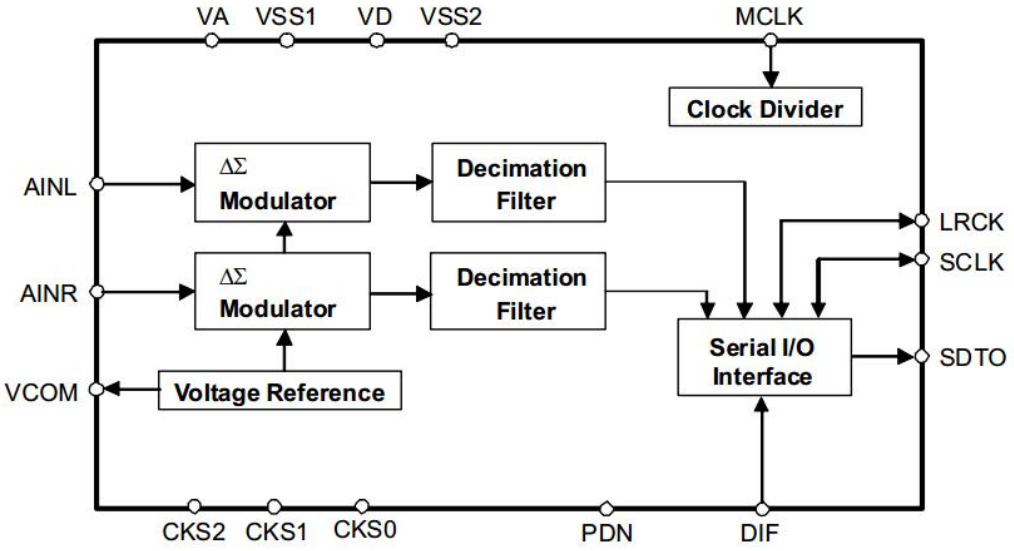
96 kHz、24bit 立体声音频 ADC

概述：

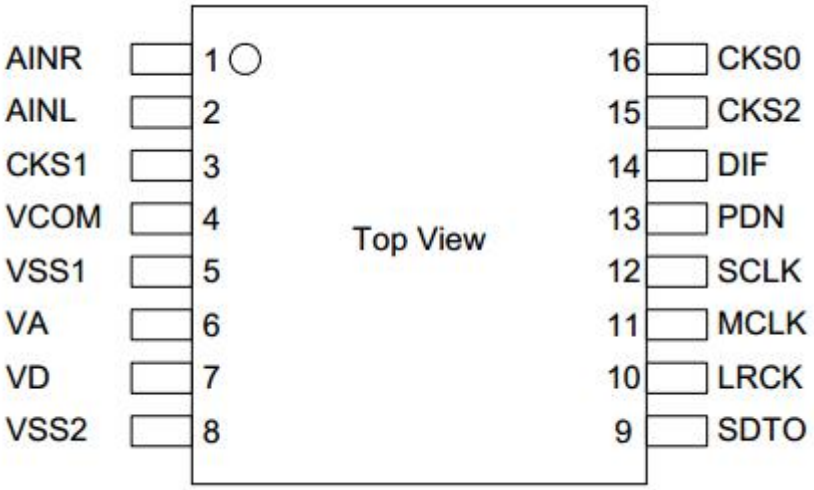
GC5358 是一款高性能、宽采样率、立体声音频模数转换器。其采样率范围是 8KHz~96KHz，非常适合从消费级到专业级的音频应用系统。单端模拟输入不需要外围器件。GC5358 音频有两种数据格式：MSB 对齐和 I2S 格式，和各种如 DTV、DVR、AV 音频系统兼容。

特点：

- 相位线性的数字抗混叠滤波
- 单端输入
- 数字HPF消除直流失调
- S/(N+D):92dB
- DR:102DB
- S/N:102dB
- 采样率从8KHz~96KHz
- 主时钟：256fs/384fs/512fs/768fs (8kHz ~ 48kHz)
  256fs/384fs (48kHz ~ 96kHz)
- 输入电平：TTL、CMOS
- 主机、从机模式
- 数据格式：24-Bit MSB对齐、I2S
- 4.5V~5.5V 模拟电源 (VA)
- 2.7V~5.5V数字电源 (VDD)
- 温度范围：-20~85℃
- 封装：TSSOP16


VA
VSS1
VD
VSS2
MCLK
Clock Divider
AINL
ΔΣ Modulator
Decimation Filter
AINR
ΔΣ Modulator
Decimation Filter
LRCK
SCLK
Serial I/O Interface
SDTO
VCOM
Voltage Reference
CKS2
CKS1
CKS0
PDN
DIF

■ Pin Layout


AINR 1
AINL 2
CKS1 3
VCOM 4
VSS1 5
VA 6
VD 7
VSS2 8
Top View
16 CKS0
15 CKS2
14 DIF
13 PDN
12 SCLK
11 MCLK
10 LRCK
9 SDTO

No.	Pin Name	I/O	Function
1	AINR	I	Rch Analog Input Pin
2	AINL	I	Lch Analog Input Pin
3	CKS1	I	Mode Select 1 Pin
4	VCOM	O	Common Voltage Output Pin, VA/2 Bias voltage of ADC input.
5	VSS1	-	Ground Pin
6	VA	-	Analog Power Supply Pin, 4.5 ~ 5.5V
7	VD	┣	Digital Power Supply Pin, 2.7 ~ 5.5V
8	VSS2	-	Ground Pin
9	SDTO	O	Audio Serial Data Output Pin "L" Output at Power-down mode.
10	LRCK	I/O	Output Channel Clock Pin "L" Output in Master Mode at Power-down mode.
11	MCLK	I	Master Clock Input Pin
12	SCLK	I/O	Audio Serial Data Clock Pin "L" Output in Master Mode at Power-down mode.
13	PDN	I	Power Down Mode & Reset Pin "H": Power up, "L": Power down & Reset
14	DIF	I	Audio Interface Format Pin "H": 24bit I^2S Compatible, "L": 24bit MSB justified
15	CKS2	I	Mode Select 2 Pin
16	CKS0	I	Mode Select 0 Pin

■ Handling of Unused Pin

Classification	Pin Name	Setting
Analog	AINL	This pin must be open.
	AINR	This pin must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	VA	−0.3	6.0	V
	Digital	VD	−0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (AINL, AINR, CKS1 pins)		VINA	−0.3	VA+0.3	V
Digital Input Voltage (Note 2)		VIND	−0.3	VD+0.3	V
Ambient Temperature (powered applied)		Ta	−20	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. PDN, DIF, MCLK, SCLK, LRCK, CKS0, CKS2 pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	VA	4.5	5.0	5.5	V
	Digital	VD	2.7	5.0	VA	V

Note 3. The power up sequence between VA and VD is not critical.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=5.0, VD=5.0V; VSS1=VSS2=0V; fs=48kHz, 96kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics:						
Resolution					24	Bits
Input Voltage		(Note 4)	2.7	3.0	3.3	Vpp
S/(N+D)	fs=48kHz	−1dBFS	82	92		dB
	BW=20kHz	−60dBFS	-	39		dB
	fs=96kHz	−1dBFS	-	90		dB
	BW=40kHz	−60dBFS	-	38		dB
DR	(−60dBFS, A-weighted)		94	102		dB
S/N	(A-weighted)		94	102		dB
Input Resistance	fs=48kHz		13	20		kΩ
	fs=96kHz		9	14		kΩ
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				100	-	ppm/°C
Power Supply Rejection		(Note 5)	-	50		dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
VA				12	18	mA
VD	(fs=48kHz)	(Note 6)		3	5	mA
VD	(fs=96kHz)	(Note 7)		6	9	mA
Power down mode (PDN pin = "L")		(Note 8)				
VA+VD				10	100	μA

Note 4. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage. Vin = 0.6 x VA (Vpp).
Note 5. PSR is applied to VA and VD with 1kHz, 50mVpp.
Note 6. VD=2mA@3V
Note 7. VD=4mA@3V
Note 8. All digital input pins and CKS1 pin are held VD or VSS2.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=-20°C ~ 85°C; VA=4.5 ~ 5.5V; VD=2.7 ~ 5.5V)

Parameter			Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):							
Passband	(Note 9)	±0.1dB	PB	0		18.9	kHz
		−0.2dB		-	20.0	-	kHz
		−3.0dB		-	23.0	-	kHz
Stopband			SB	28			kHz
Passband Ripple			PR			±0.04	dB
Stopband Attenuation			SA	68			dB
Group Delay Distortion			ΔGD		0		μs
Group Delay		(Note 10)	GD		16		1/fs
ADC Digital Filter (HPF):							
Frequency Response	(Note 9)	−3dB	FR		1.0		Hz
		−0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=-20°C ~ 85°C; VA=4.5 ~ 5.5V; VD=2.7 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	±0.1dB	PB	0		37.8	kHz
	−0.2dB		-	40.0	-	kHz
	−3.0dB		-	46.0	-	kHz
Stopband		SB	56			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay Distortion		ΔGD		0		μs
Group Delay (Note 10)		GD		16		1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	−3dB	FR		2.0		Hz
	−0.1dB			13.0		Hz

Note 9. The passband and stopband frequencies scale with fs. For example, PB=48kHz@±0.1dB is 0.39375 × fs.
Note 10. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS (CMOS Level Mode)

(Ta=-20°C ~ 85°C; VA=4.5 ~ 5.5V; VD=2.7 ~ 5.5V; CKS2/1/0 = "LLL", "LHL", "LHH", "HHL", "HHH")

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%VD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%VD	V
High-Level Output Voltage	(Iout=−1mA)	VOH	VD−0.5	-	-	V
Low-Level Output Voltage	(Iout=1mA)	VOL	-	-	0.5	V
Input Leakage Current		Iin	-	-	±10	μA

DC CHARACTERISTICS (TTL Level Mode)

(Ta=-20°C ~ 85°C; VA=4.5 ~ 5.5V; VD=4.5 ~ 5.5V; CKS2/1/0 = "HLL")

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(CKS2-0 pins)	VIH	70%VD	-	-	V
	(All pins except CKS2-0 pins)	VIH	2.2	-	-	V
Low-Level Input Voltage	(CKS2-0 pins)	VIL	-	-	30%VD	V
	(All pins except CKS2-0 pins)	VIL	-	-	0.8	V
High-Level Output Voltage	(Iout=−1mA)	VOH	VD−0.5	-	-	V
Low-Level Output Voltage	(Iout=1mA)	VOL	-	-	0.5	V
Input Leakage Current		Iin	-	-	±10	μA

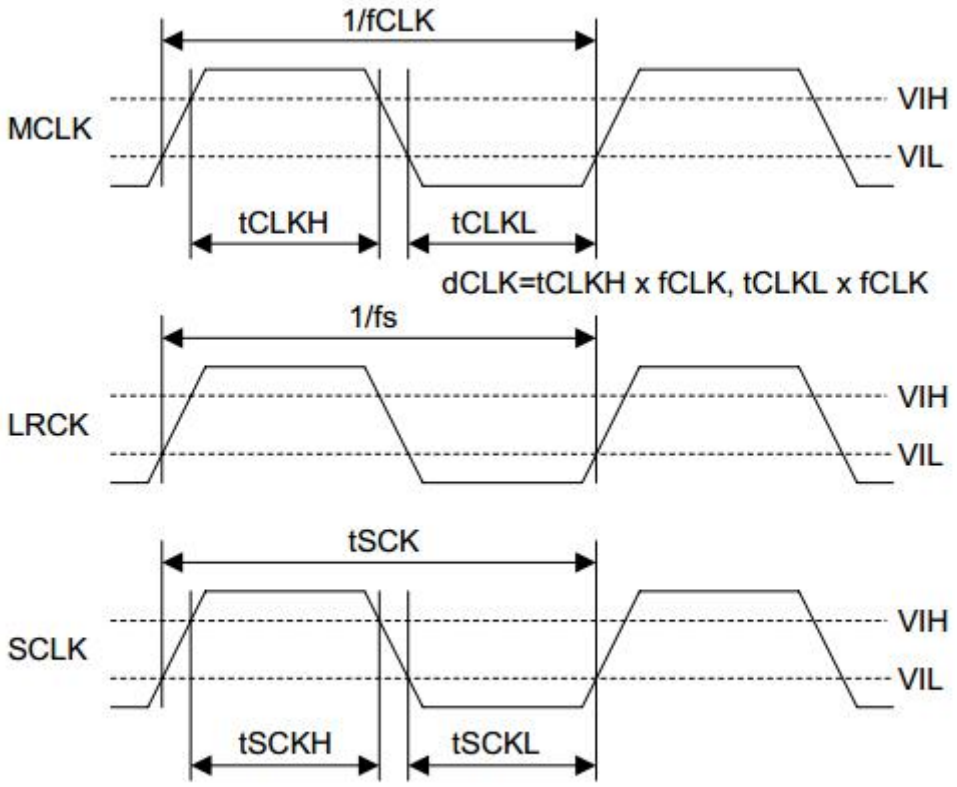
SWITCHING CHARACTERISTICS

(Ta=-20°C ~ 85°C; VA=4.5 ~ 5.5V; VD=2.7 ~ 5.5V; C_L=20pF)

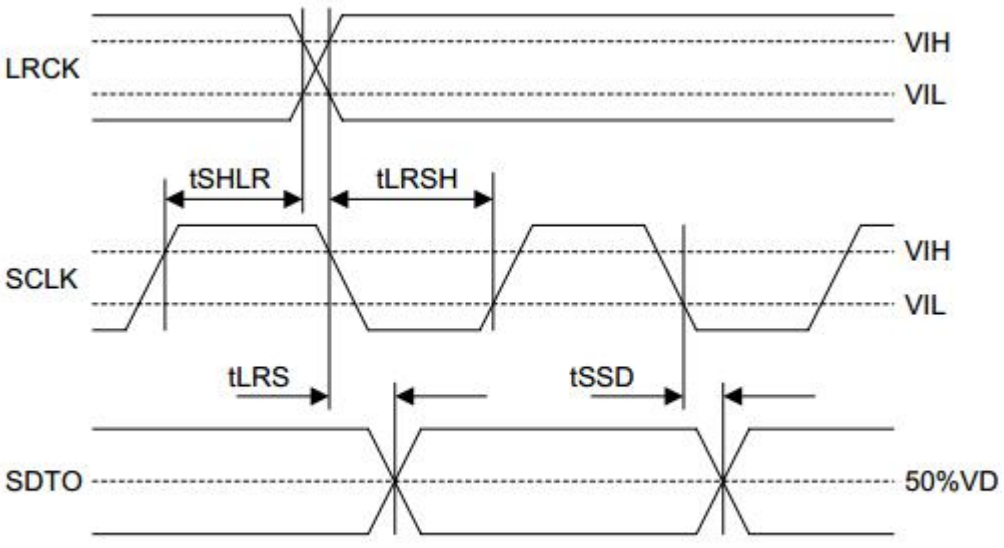
Parameter		Symbol	min	typ	max	Units
Master Clock Timing (Note 11)						
512fs, 256fs Frequency		fCLK	2.048		24.576	MHz
Duty cycle		dCLK	40		60	%
768fs, 384fs Frequency		fCLK	3.072		36.864	MHz
Duty cycle		dCLK	40		60	%
LRCK Frequency		fs	8		96	kHz
Duty Cycle	Slave mode		45		55	%
	Master mode			50		%
Audio Interface Timing						
Slave mode						
SCLK Period		tSCK	160			ns
SCLK Pulse Width Low		tSCKL	65			ns
Pulse Width High		tSCKH	65			ns
LRCK Edge to SCLK "↑" (Note 12)		tLRSH	30			ns
SCLK "↑" to LRCK Edge (Note 12)		tSHLR	30			ns
LRCK to SDTO (MSB) (Except I^2S mode)		tLRS			35	ns
SCLK "↓" to SDTO		tSSD			35	ns
Master mode						
SCLK Frequency		fSCK		64fs		Hz
SCLK Duty		dSCK		50		%
SCLK "↓" to LRCK		tMSLR	−20		20	ns
SCLK "↓" to SDTO		tSSD	−20		35	ns
Reset Timing						
PDN Pulse Width (Note 13)		tPD	150			ns
PDN "↑" to SDTO valid at Slave Mode (Note 14)		tPDV		4132		1/fs
PDN "↑" to SDTO valid at Master Mode (Note 14)		tPDV		4129		1/fs

Note 11. The AK5358B is reset by more than 13us "L" period of MCLK. The data is output after initializing.
Note 12. SCLK rising edge must not occur at the same time as LRCK edge.
Note 13. The AK5358B can be reset by bringing the PDN pin = "L".
Note 14. This cycle is the number of LRCK rising edges from the PDN pin = "H".

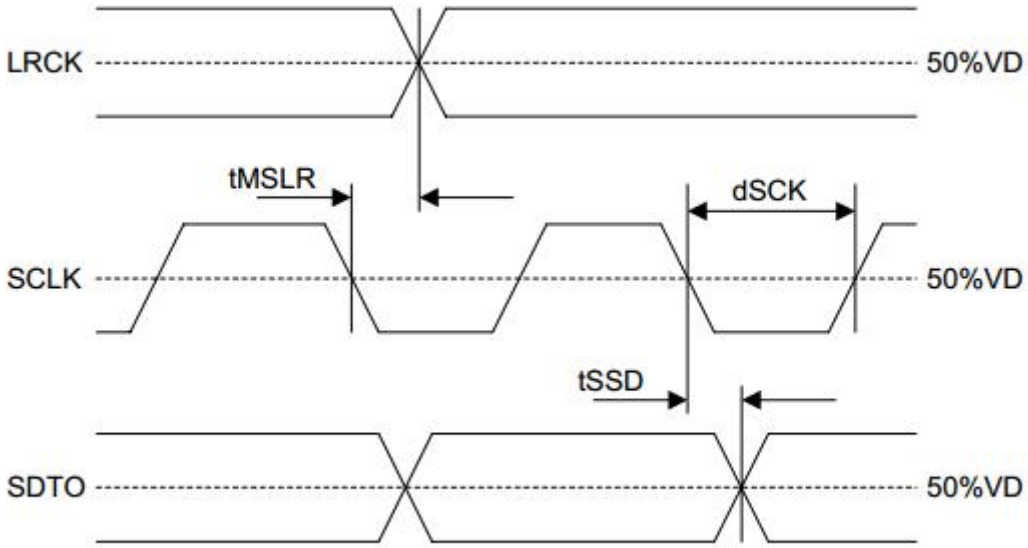
■ Timing Diagram



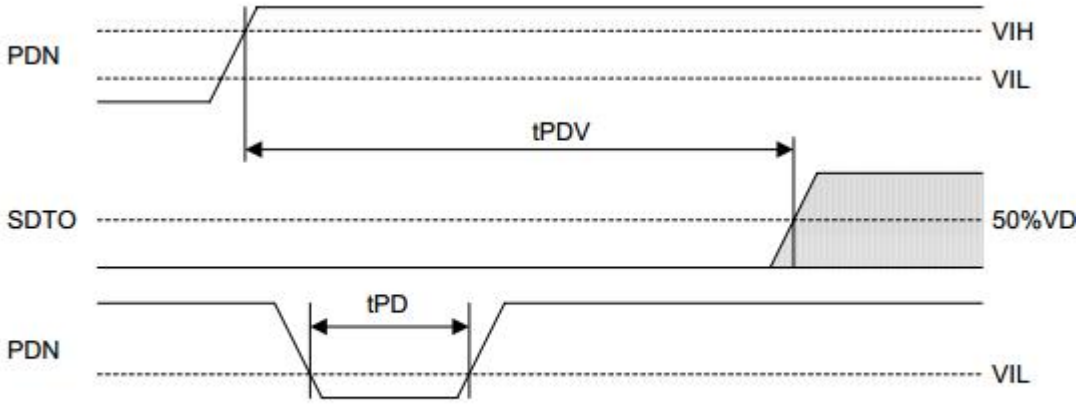
Clock Timing



Audio Interface Timing (Slave mode)



Audio Interface Timing (Master mode)



Power Down & Reset Timing

■ System Clock

MCLK, SCLK and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. MCLK frequency, SCLK frequency and master/slave modes are selected by CKS2-0 pins as shown in Table 2.

fs	MCLK			
	256fs	384fs	512fs	768fs
32kHz	8.192MHz	12.288MHz	16.384MHz	24.576MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz
48kHz	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	24.576MHz	36.864MHz	N/A	N/A

Table 1. System Clock Example

Mode	CKS2	CKS1	CKS0	Input Level	Master/Slave	MCLK	SCLK
0	L	L	L	CMOS	Slave	256/384fs (8k≤fs≤96k) 512/768fs (8k≤fs≤48k)	≥ 48fs or 32fs (Note 15)
1	L	L	H			Reserved	
2	L	H	L	CMOS	Master	256fs (8k≤fs≤96k)	64fs
3	L	H	H	CMOS	Master	512fs (8k≤fs≤48k)	64fs
4	H	L	L	TTL	Slave	256/385fs(~ 96kHz) 512/768fs(~ 48kHz)	≥ 48fs or 32fs (Note 15)
5	H	L	H			Reserved	
6	H	H	L	CMOS	Master	384fs (8k≤fs≤96k)	64fs
7	H	H	H	CMOS	Master	768fs (8k≤fs≤48k)	64fs

Table 2. Operation Mode Select

Note 15. SDTO outputs 16bit data at SCLK=32fs.

■ Audio Interface Format

Two kinds of data formats can be selected by the DIF pin (Table 3). In both modes, the serial data is in MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of SCLK. The audio interface supports both master and slave modes. In master mode, SCLK and LRCK are output with the SCLK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

Mode	DIF pin	SDTO	LRCK	SCLK	Figure
0	L	24bit, MSB justified	H/L	≥ 48fs or 32fs	Figure 1
1	H	24bit, I^2S Compatible	L/H	≥ 48fs or 32fs	Figure 2

Table 3. Audio Interface Format

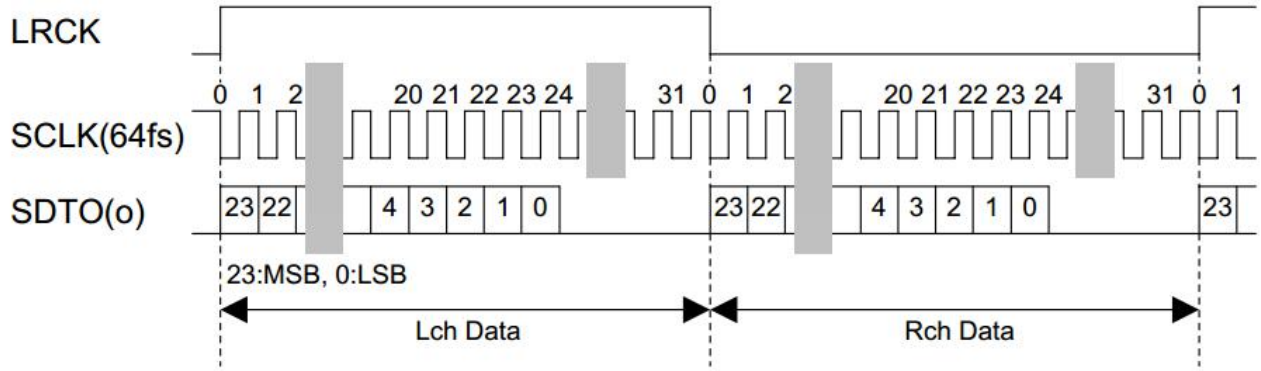


Figure 1. Mode 0 Timing

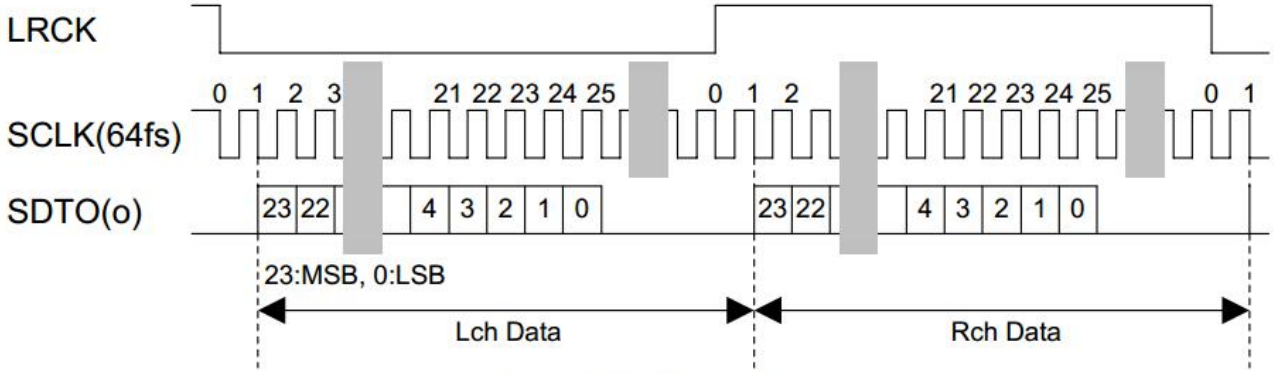


Figure 2. Mode 1 Timing

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and it scales with sampling rate (fs).

■ Power Down

The GC5358 is placed in power-down mode by bringing the PDN pin “L” or MCLK stop more than 13us, and the digital filter is also reset at the same time. This reset should always be made after power-up. In power-down mode, the VCOM is same level as VSS1. MCLK and LRCK must be input when the PDN pin is “H” to release the power down mode. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 4129 cycles of LRCK clock in master mode or 4132 cycles of LRCK clock in slave mode.

During initialization, the ADC digital data outputs of both channels are forced to a 2’s complement “0”. The ADC outputs are settled in the data corresponding to the input signals after the end of initialization (Settling approximately takes the same time as group delay).

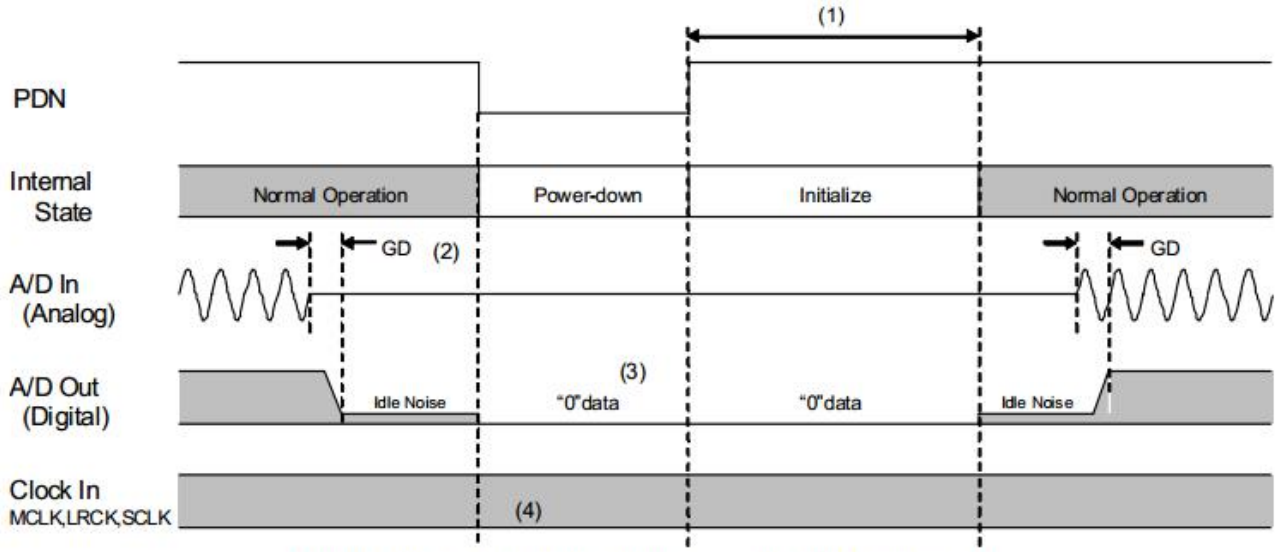


Figure 3. Power-down/up sequence example (PDN pin reset)

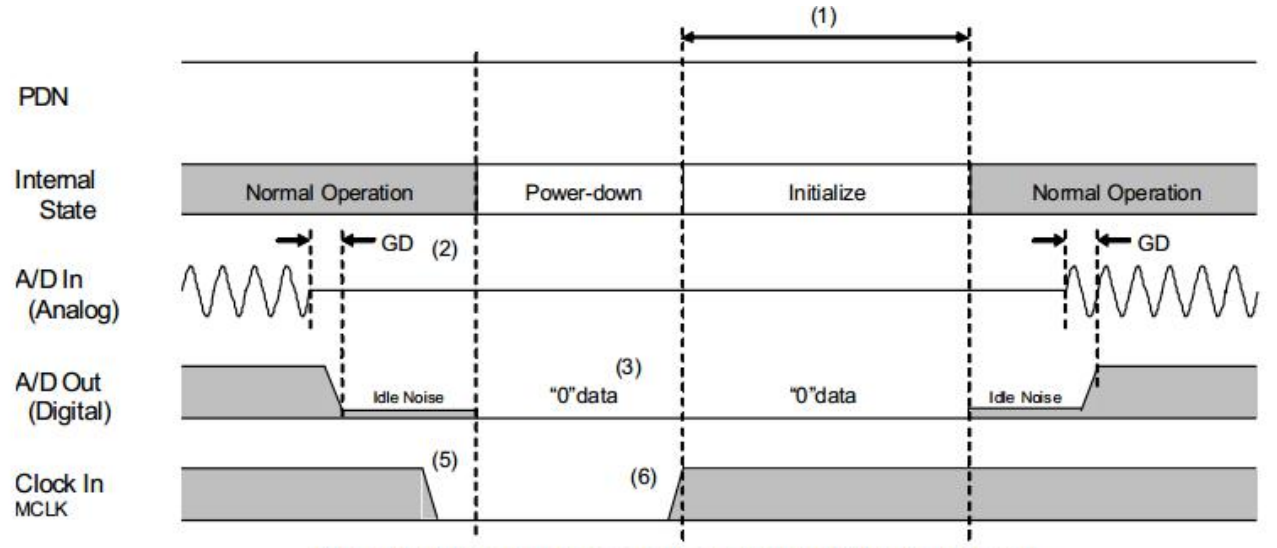


Figure 4. Power-down/up sequence example (MCLK stop reset)

Notes:

(1) 4132/fs in slave mode and 4129/fs in master mode.

(2) Digital output corresponding to analog input has the group delay (GD).

(3) A/D outputs "0" data at the power-down state.

(4) MCLK is input as normal operation.

(5) When MCLK is stopped more than 13us, the GC5358B becomes power down mode.

(6) MCLK and LRCK must be input to release power-down mode.

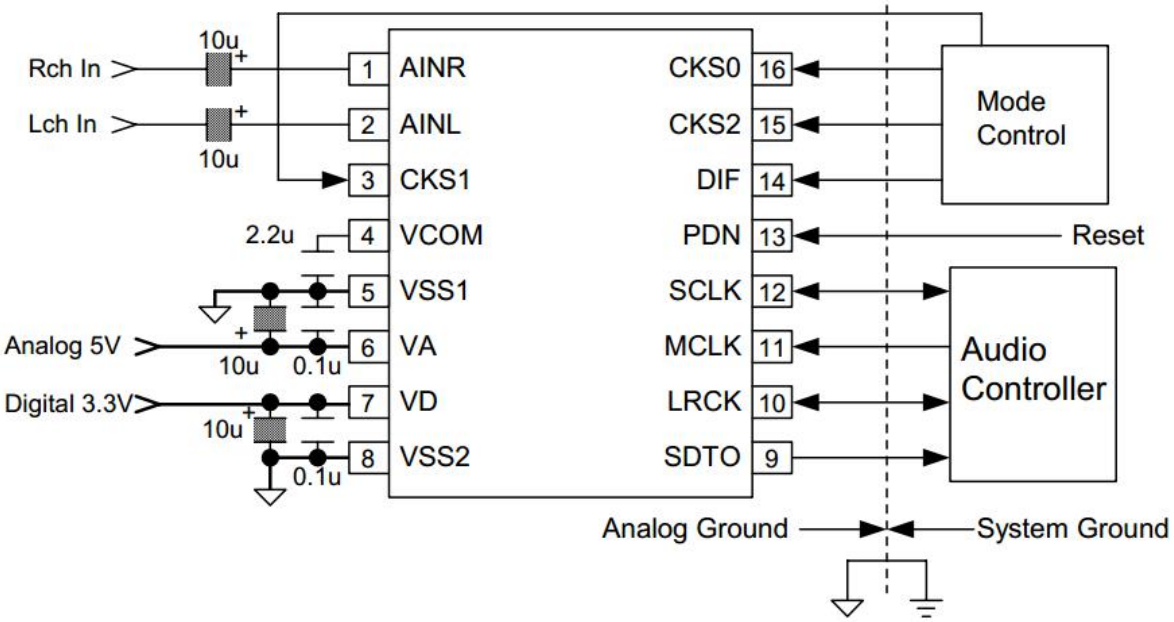
■ System Reset

The GC5358 must be reset once by bringing the PDN pin "L" or inputting MCLK 13us (min) after the GC5358 is powered-up. In slave mode, the internal timing starts clocking by the rising edge (falling edge at mode 1) of LRCK after exiting from reset and power down state by MCLK. The GC5358 is power down state until LRCK is input. In master

mode, the internal timing starts when MCLK is input.

SYSTEM DESIGN

Figure 5 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:

- VSS1 and VSS2 should be distributed separately from the ground of external digital devices(MPU, DSP etc.).
- All digital input pins should not be left floating.
- The CKS1 pin should be connected to VA or VSS1.

Figure 5. Typical Connection Diagram

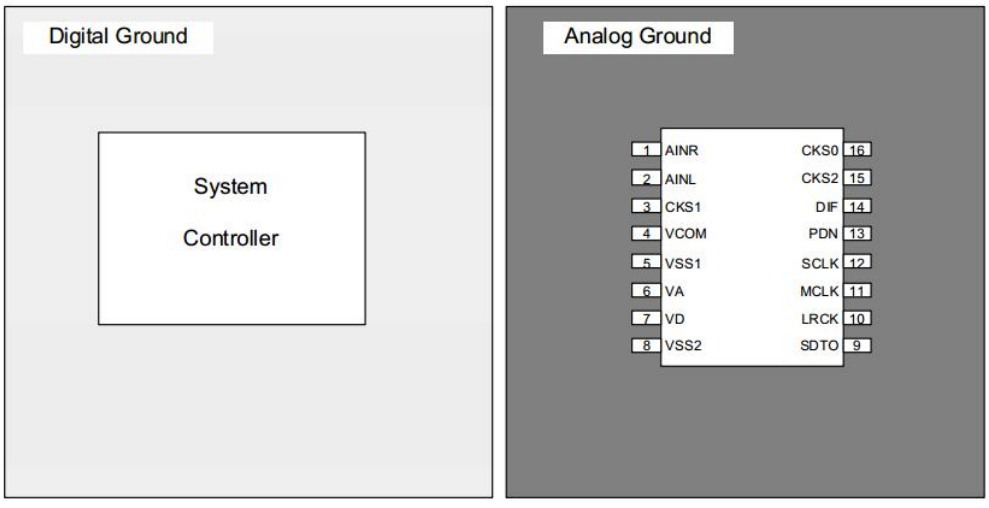


Figure 6. Ground Layout

Note: - VSS1 and VSS2 must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The GC5358 requires careful attention to power supply and grounding arrangements. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. VSS1 and VSS2 of the GC5358 must be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the GC5358 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The voltage input to VA sets the analog input range. VCOM are 50%VA and normally connected to VSS1 with a 0.1μF ceramic capacitor. A capacitor 2.2μF is attached to VCOM pin. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the GC5358.

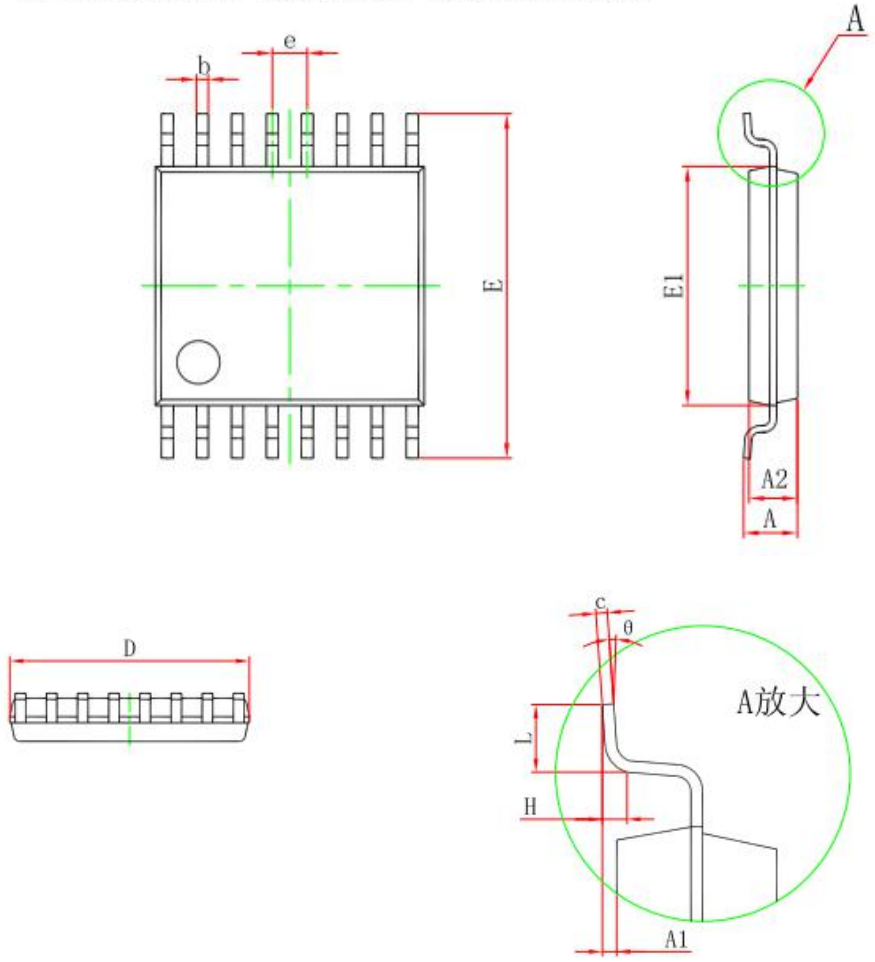
3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (50%VA) with 20kΩ (typ@fs=48kHz) resistance. The input signal range scales with the supply voltage and nominally 0.6xVA Vpp (typ). The ADC output data format is 2's complement. The internal HPF removes the DC offset.

TheGC5358 samples the analog inputs at 64fs (@fs=48kHz). The digital filter rejects noise above the stop band except for multiples of 64fs. TheGC5358 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

PACKAGE

TSSOP16 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65（BSC）		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°