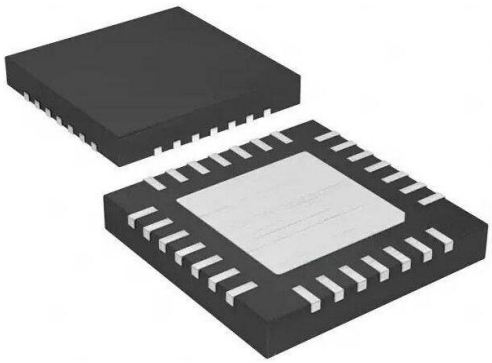
●Pin distribution diagram

Features and Benefits

●Drives 6 N-channel MOSFETs
●Wide operating voltage 4.7~36V
●Synchronous rectification for low power dissipation
●Hall element inputs
●Internal UVLO and thermal shutdown circuitry
●Standby mode
●FG outputs
●Dead time protection
●Lock detect protection
●Overvoltage protection



QFN28

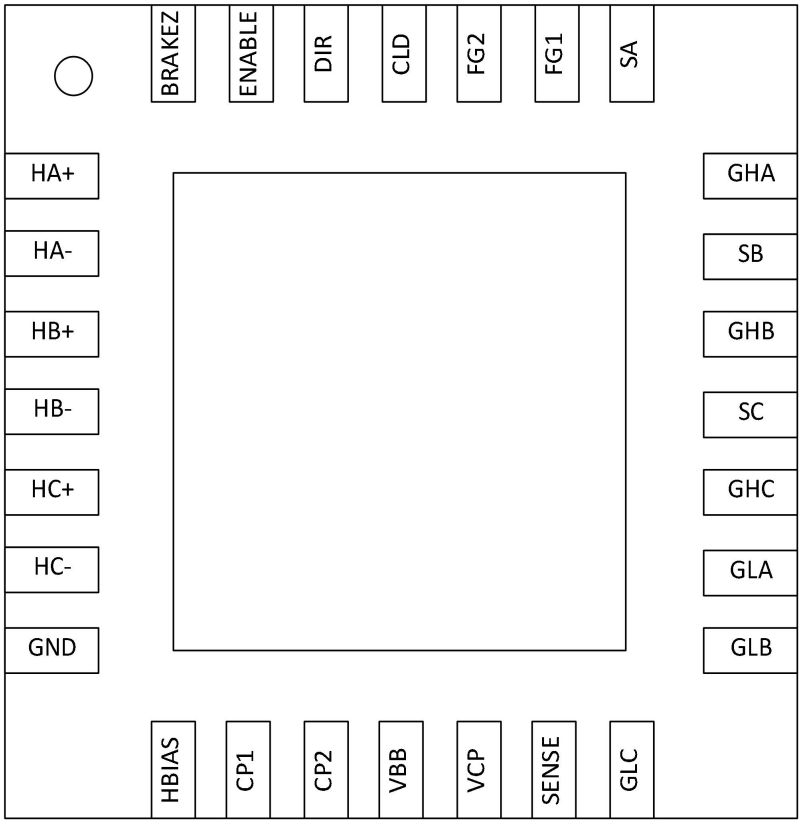
Description

The GC4931F is a complete 3-phase brushless DC motor pre-driver. The device is capable of driving a wide range of N-channel power MOSFETs and can support motor supply voltages up to 36 V. Commutation logic is determined by three Hall-element inputs spaced at 120°.

Other features include fixed off-time pulse width modulation (PWM) current control for limiting inrush current, locked-rotor protection with adjustable delay, thermal shutdown, overvoltage monitor, and synchronous rectification. Internal synchronous rectification reduces power dissipation by turning on the appropriate MOSFETs during current decay, thus shorting the body diode with the low RDS(on) MOSFET. Overvoltage protection disables synchronous rectification when the motor pumps the supply voltage beyond the overvoltage threshold during current recirculation

The GC4931F offers enable, direction, and brake inputs that can control current using either phase or enable chopping. Logic outputs FG1 and FG2 can be used to accurately measure motor rotation. Output signals toggle state during Hall transitions, providing an accurate speed output to a microcontroller or speed control circuit

Operating temperature range is –20°C to 105°C. The GC4931F is supplied in a 5 mm × 5 mm, 28-terminal QFN package with exposed thermal pad. This small footprint package is lead (Pb) free with 100% matte tin leadframe plating.



Pin description

Pin number QFN28	Pin name	I/O	Pin definition
1	HA+	I	HALL A Phase positive input
2	HA-	I	HALL A Phase negative input
3	HB+	I	HALL B Phase positive input
4	HB-	I	HALL B Phase negative input
5	HC+	I	HALL C Phase positive input
6	HC-	I	HALL C Phase negative input
7	GND	GND	GND
8	HBIAS	IO	5V Power output
9	CP1	IO	Charge pump 1
10	CP2	IO	Charge pump 2
11	VBB	POWER	Power supply
12	VCP	IO	Charge pump capacitor pin
13	SENSE	IO	Current monitoring pin
14	GLC	IO	C Phase lower arm bridge grid drive

15	GLB	IO	B Phase lower arm bridge grid drive
16	GLA	IO	A Phase lower arm bridge grid drive
17	GHC	IO	C Phase up arm bridge grid drive
18	SC	IO	C Phase output
19	GHB	IO	B Phase up arm bridge grid drive
20	SB	IO	B Phase output
21	GHA	IO	A Phase up arm bridge grid drive
22	SA	IO	A Phase output
23	FG1	O	Speed output pin（3ϕ）
24	FG2	O	Speed output pin（ϕA）
25	CLD	IO	Locked rotor protection external regulating capacitor pin
26	DIR	I	Motor direction foot
27	ENABLE	I	External PWM control pin (low effective)
28	BREAKZ	I	Brake (low effective)

Internal block diagram

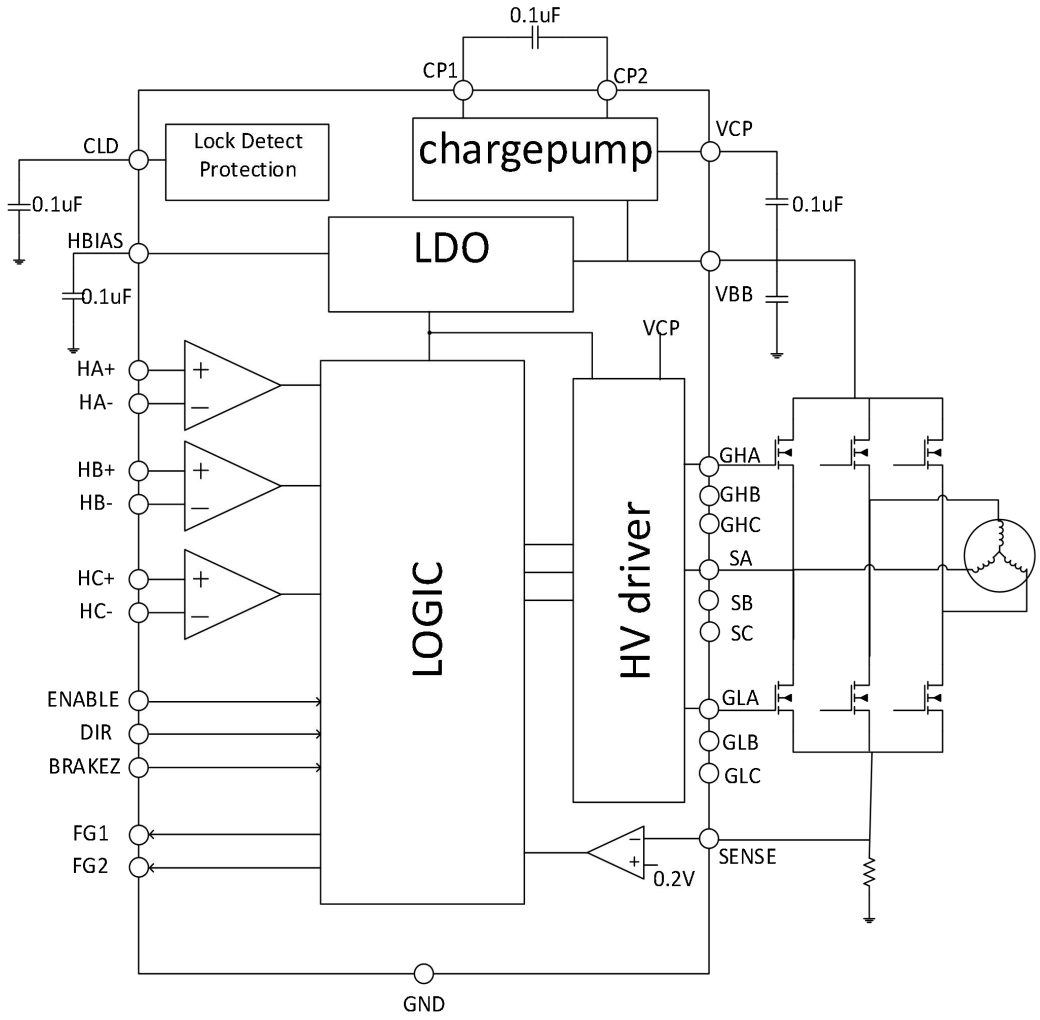


Figure 1 internal block diagram of GC4931F

Limit parameters (generally without other special notes, T=25℃)

Parameters	Symbol	Parameter range	unit
Maximum operating voltage	VBB	38	V
Hall input	VHx	-0.3~7	V
Logic input	Vin	-0.3~7	V
Maximum Junction Temperature	Tjmax	150	℃
Storage Temperature	Tstg	-60~150	℃
Electrostatic protection (HBM)	ESD	±4000	V

Electrical parameters (unless otherwise specified, test condition t = 25 ℃, VBB = 24V)

Pin parameters: (no other description, t = 25 ℃)

Parameters	Symbol	Test conditions	Min	Typ	Max	unit
supply voltage	V_{BB}	GC4931F	4.7		36	V
Operating current	I_{BB}	f_{PWM}<30kHz,C_{load}=1nF		4	6	mA
		Chargepump On, output off, power saving mode		3.3	3.6	mA
HBIAS Pin voltage	V_{Hbais}	0<$I_{Hbaislim}$<24	5.1	5.2	5.3	V
Hbias current	$I_{Hbaislim}$		35			mA
FG Support voltage	V_{FG}		0		6	V
FG Pin current	I_{FG}		0		14	mA

Module parameters: no other description，T=25℃，VBB=24V

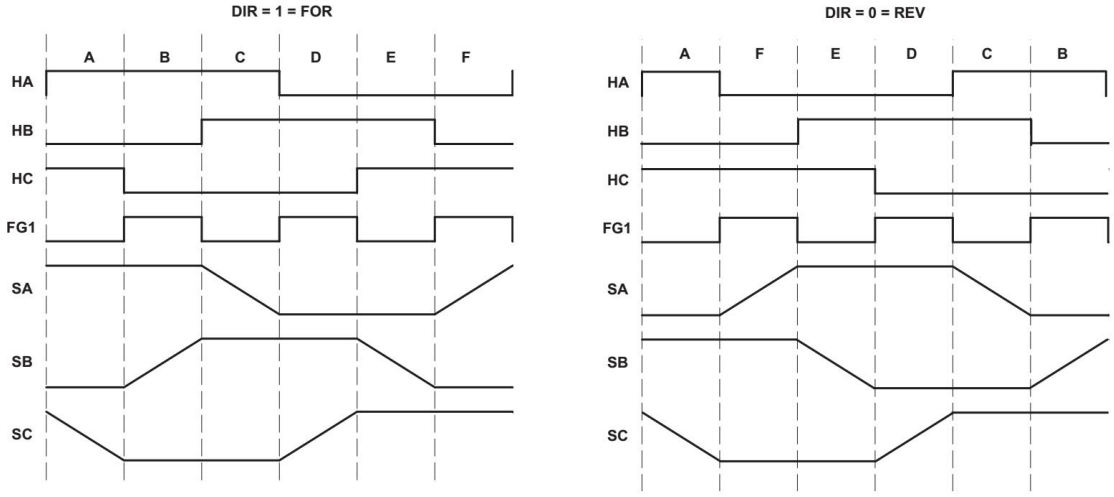
Logic input						
High level input voltage	V_{IN1}		2		HBIAS	V
Low level input voltage	V_{IN0}		0		0.8	V
Logic input pull-up resistance	RIN（pu）	ENABLE,BRAKEZ,DIR Pull up to the Hbias resistor		50K		Ω
Input anti shake hysteresis	T_{glitch}	ENABLE input	350	500	650	ns
		BRAKEZ，DIR input	700	1000	1300	ns
ENABLE Power saving mode delay	Td_{enable}	ENABLE High to output off	2.1	3	3.9	ms
Hbias Wake up time	Td_{Hbais}	Hbias cap 0.1uF		15	25	us
Output driver module						
High gate output	$V_{GS（H）}$	IGATE=2mA		5.2		V
Low gate output	$V_{GS（L）}$	IGATE=2mA		5.3		V
Gate drive current	I_{GATE}	GH=GL=4	20	30		mA
Gate drive pull-down resistance	R_{GATE}		10	28	40	Ω
Dead Time	T_{dead}	ID=-1A	0.7	1.0	1.3	us
Current limiting threshold voltage	V_{REF}	ID=1A		200		mV
Fixed attenuation period	T_{off}		18	25	37	us
Protection module						
Over temperature shutdown	TSD		155	170	185	℃
Hysteresis	△TSD			20		℃
VCP undervoltage protection voltage	Δ V_{CPUV}	be relative to VBB	4.6		6	V
Locked protection time	T_{lock}	CLD capacitance 0.1uF	1.5	2	2.5	s
VBB undervoltage protection	VBBuvlo	VBB Low voltage protection point	4.5	4.7	4.9	V
VBB overvoltage	V_{BBOV}	VBB overvoltage	28.5	29	29.5	V

protection		protection point				
VBB overvoltage protection hysteresis	ΔV_{BBOV}	VBB overvoltage protection hysteresis		2		V
HALL amplifier						
Input current	I_{HALL}	VIN=0.2~3.5V	-1	0	1	uA
Common mode voltage	V_{CMR}	Input CMR	0.2		3.5	V
Hall input sensitivity	V_{HALL}	Min differential input voltage		±10		mV
Hall input hysteresis	Vth		5	20	40	mV
Abnormal pulse filtering	T_{pulse}			2		us
FG 1/FG2						
On resistance	V_{FGsat}	IFG=2mA			0.5	V
Leakage current	I_{FGlkg}	VFG=5V			1	uA

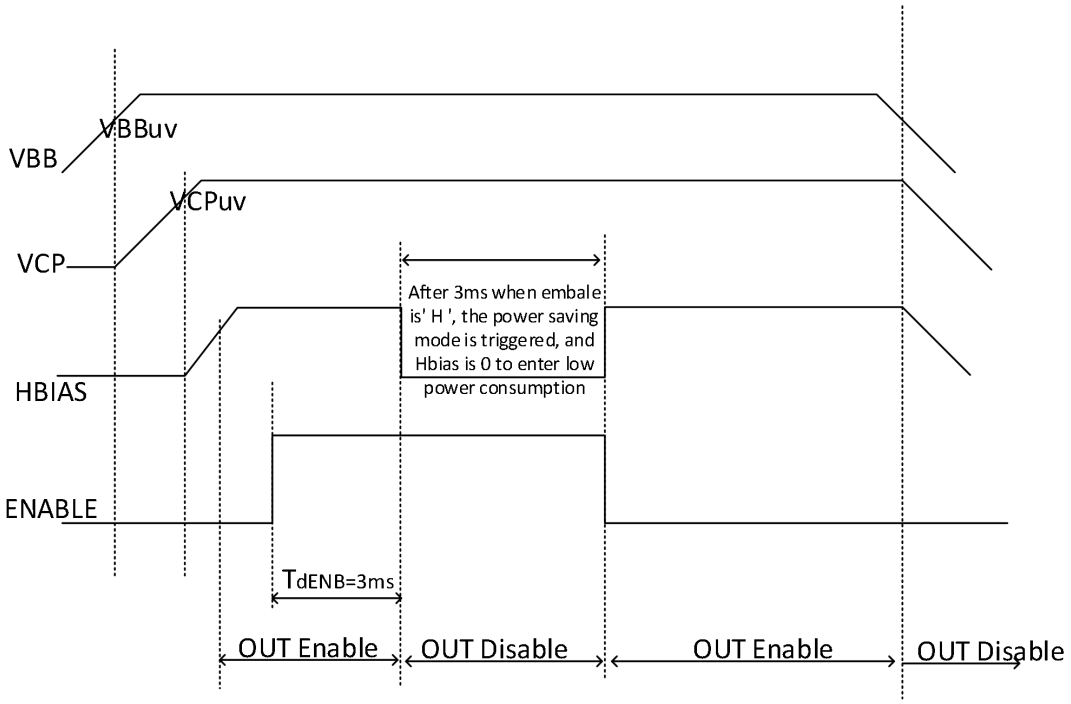
Function description

Logic truth table (x is arbitrary, Z is high resistance state)

Condition		Inputs					Resulting Pre-Driver Outputs						Motor Output		
		HA	HB	HC	BRAKEZ	ENB	GHA	GLA	GHB	GLB	GHC	GLC	A	B	C
DIR = 1 (Forward)	A	+	–	+	HI	LO	HI	LO	LO	HI	LO	LO	HI	LO	Z
	B	+	–	–	HI	LO	HI	LO	LO	LO	LO	HI	HI	Z	LO
	C	+	+	–	HI	LO	LO	LO	HI	LO	LO	HI	Z	HI	LO
	D	–	+	–	HI	LO	LO	HI	HI	LO	LO	LO	LO	HI	Z
	E	–	+	+	HI	LO	LO	HI	LO	LO	HI	LO	LO	Z	HI
	F	–	–	+	HI	LO	LO	LO	LO	HI	HI	LO	Z	LO	HI
DIR = 0 (Reverse)	A	+	–	+	HI	LO	LO	HI	HI	LO	LO	LO	LO	HI	Z
	F	–	–	+	HI	LO	LO	LO	HI	LO	LO	HI	Z	HI	LO
	E	–	+	+	HI	LO	HI	LO	LO	LO	LO	HI	HI	Z	LO
	D	–	+	–	HI	LO	HI	LO	LO	HI	LO	LO	HI	LO	Z
	C	+	+	–	HI	LO	LO	LO	LO	HI	HI	LO	Z	LO	HI
	B	+	–	–	HI	LO	LO	HI	LO	LO	HI	LO	LO	Z	HI
Fault*		+	+	+	HI	X	LO	LO	LO	LO	LO	LO	Z	Z	Z
Fault*		–	–	–	HI	X	LO	LO	LO	LO	LO	LO	Z	Z	Z
Brake*		X	X	X	LO	X	LO	HI	LO	HI	LO	HI	LO	LO	LO



Power on Sequence & power saving mode sequence diagram



Current Regulation

Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the full bridge are turned on, current increases in the motor winding until it reaches a value, Itrip, given by:

Itrip = 200mV / Rsense

When Itrip is reached, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off-time period.

ENABLE Logic

The Enable input terminal (ENB pin) allows external PWM. ENB low turns on the selected sink-source pair. ENB high switches off the appropriate drivers and the load current decays. If ENB is held low, the current will rise until it reaches the level set by the internal current control

circuit. Typically PWM frequency is in 20 kHz to 30 kHz range. If the ENB high pulse width exceeds 3 ms, the gate outputs are disabled. The Enable logic is summarized in the following table:

ENABLE	Output drive tube status	Motor drive status
0	Open	Effective
1	Upper arm bridge off	Slow attenuation band synchronous rectifier
1 （Duration greater than 3ms）	Turn off	invalid

Fixed attenuation period

The GC4931F fixed attenuation period is 25us

PWM Blank time

When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes as well as switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source Enable latch, the sense comparator is blanked. The blanking timer runs after the off-time counter completes, in order to provide the blanking function. The blanking timer is reset when ENB is chopped or DIR is changed. With external PWM control, a DIR change or an ENB on triggers the blanking function. The duration is fixed at 1.5 µs.

Synchronous Rectification

When a PWM-off cycle is triggered, either by a chop command on ENB or by an internal fixed off-time cycle, load current recirculates. The GC4931F synchronous rectification feature turns on the appropriate MOSFETs during the current decay, and effectively shorts out the body diodes with the low RDS(on) driver. This lowers power dissipation significantly and can eliminate the need for external Schottky diodes.

Brake Mode

A logic low on the BRAKEZ pin activates Brake mode. A logic high allows normal operation. Braking turns on all three sink drivers, effectively shorting out the motor-generated BEMF. The BRAKEZ input overrides the ENB input and also the Lock Detect function.

It is important to note that the internal PWM current control circuit does not limit the current when braking, because the current does not flow through the sense resistor. The maximum current can be approximated by VBEMF / RLOAD. Care should be taken to insure that the maximum ratings of the GC4931F are not exceeded in the worse case braking situation, high speed and high inertial load.

HBIAS Function

The chip has a built-in LDO output of 5.2v and a maximum current of 30mA for Hall IC.

Standby Mode

To prevent excessive power dissipation due to the current draw of the external Hall elements, Standby mode turns off the HBIAS output voltage. Standby mode is triggered by holding ENB high for longer than 3 ms. Note that Brake mode overrides Standby mode, so hold the BRAKEZ pin high in order to enter Standby mode.

Charge Pump

The internal charge pump is used to generate a supply above VBB to drive the high-side MOSFETs. The voltage on the VCP pin is internally monitored, and in case of a fault condition, the outputs of the device are disabled.

Fault Shutdown

In the event of a fault due to excessive junction temperature or due to low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up the UVLO circuit disables the drivers.

Overvoltage Protection

VBB is monitored to determine if a hazardous voltage is present due to the motor generator pumping up the supply bus. When the voltage exceeds VBBOV , the synchronous rectification feature is disabled.

Overtemperature Protection

If die temperature exceeds approximately 170°C, the Thermal Shutdown function will disable the outputs until the internal temperature falls below the 18°C hysteresis

However, because the over temperature protection is activated only when the chip junction temperature exceeds the set value, it does not guarantee that the product will be protected from damage with this circuit.

Hall State Reporting

Both FG1 pin and FG2 pin are open drain output pins to reflect the internal hall working state. FG1 outputs the change of Hall signal each time, and FG2 outputs the change of HAx.

Lock Detect Function

The IC will evaluate a locked rotor condition under either of these two different conditions:

1. The FG1 signal is not consistently changing.

The proper commutation sequence is not being followed. The motor can be locked in a condition in which it toggles between two specific Hall device states.

Both FG1 pin and FG2 pin are open drain output pins to reflect the internal hall working state. FG1 outputs the change of Hall signal each time, and FG2 outputs the change of Hax. When it is detected that the duration of the locked rotor condition exceeds tlock, the output drive will be closed and the locked rotor condition will be locked. It can be unlocked only when the following conditions occur:

1. DIR rising or falling edge
2. ENB continuous high exceeds $t_{lock}/2$
3. VBB elimination of low voltage detection (power on again)

Tlock is determined by the external capacitance of CLD pin. CLD pin is the external capacitance pin of 1.67v peak to peak triangular wave oscillator. The calculation formula of tlock is as follows: t_{lock} = Ccld x 20 s/uF

When the CLD is short circuited to the ground, the locked rotor protection function is closed.

When in braking mode, the stall detection counter is turned off.

Typical application circuit diagram

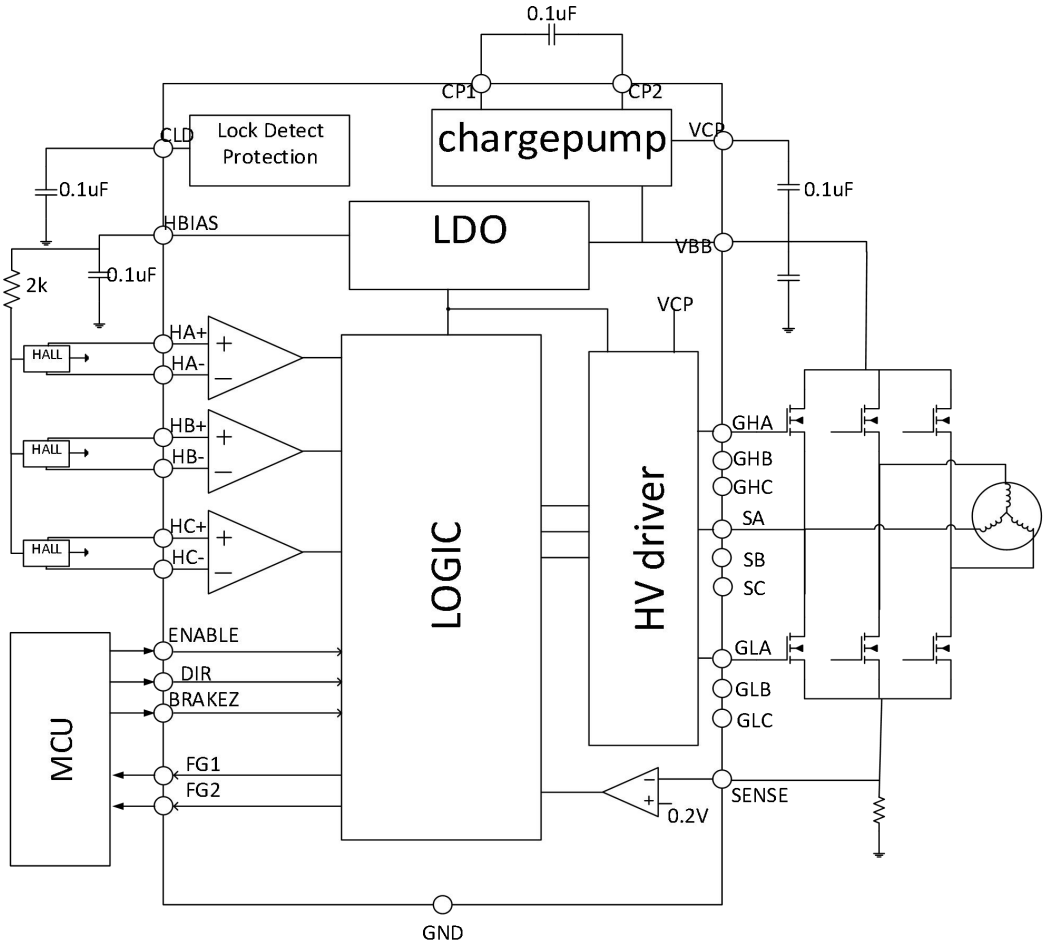
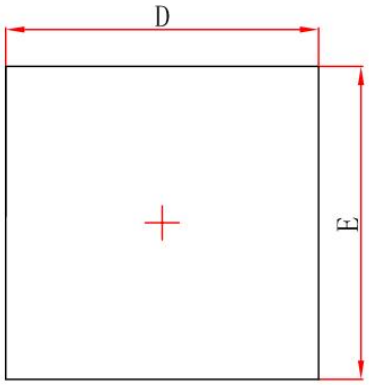
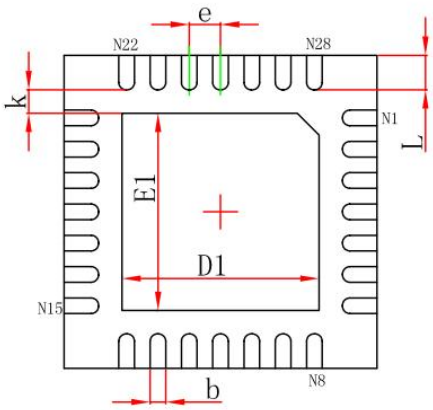


Figure 4 typical application diagram of GC4931F

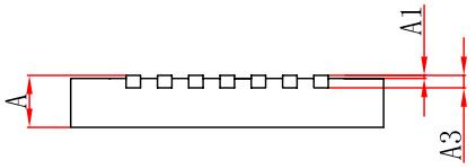
QFNWB5x5-28L(P0.5T0.75/0.8) **UNIT: mm**



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D1	3.050	3.250	0.120	0.128
E1	3.050	3.250	0.120	0.128
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.450	0.650	0.018	0.026