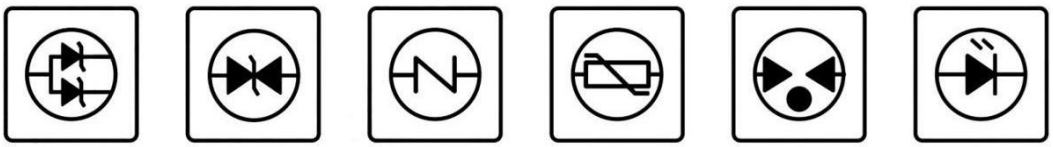
MSKSEMI 美森科
SEMICONDUCTOR



ESD9B5VL-MS

Product specification

FEATURES

- 35W peak pulse power per line (tP = 8/20μs)
- DFN1006-2L package
- Replacement for MLV(0402)
- Bidirectional configurations
- Response time is typically < 1ns
- High ESD protection
- Low clamping voltage
- RoHS compliant
- Transient protection for data lines to
- IEC61000-4-2(ESD) ±30KV(air), ± 30KV(contact)

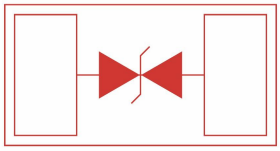
APPLICATIONS

- Cellular phones
- Portable devices
- Digital cameras
- Power supplies

Mechanical Characteristics

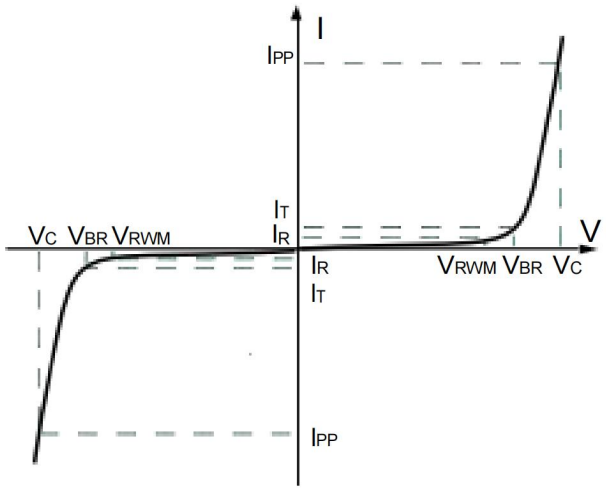
- Mounting position: Any
- Qualified max reflow temperature:260℃
- Device meets MSL 1 requirements
- DFN1006-2L without plating

Reference News

PACKAGE OUTLINE	PIN CONFIGURATION	Marking
		
DFN-1006		

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical characteristics per line@25℃(unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	I_t = 1mA	5.6	6.7	7.8	V
Reverse Leakage Current	I_R	V_{RWM} = 5V T=25℃			1.0	μA
Clamping Voltage	V_{CL}	I_{PP}=16A t_p=100ns		13.5		V
Clamping Voltage	V_C	I_{PP}=1A t_P = 8/20μs			9	V
Clamping Voltage	V_C	I_{PP}=3A t_P = 8/20μs			12	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		3		pF

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{pp}	35	W
Peak Pulse Current (t_p=8/20μs)	I_{pp}	3	A
Operating Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

Typical Characteristics

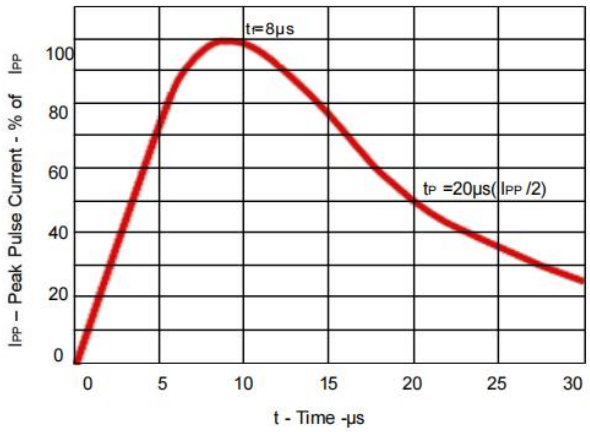


Fig 1.Pulse Waveform

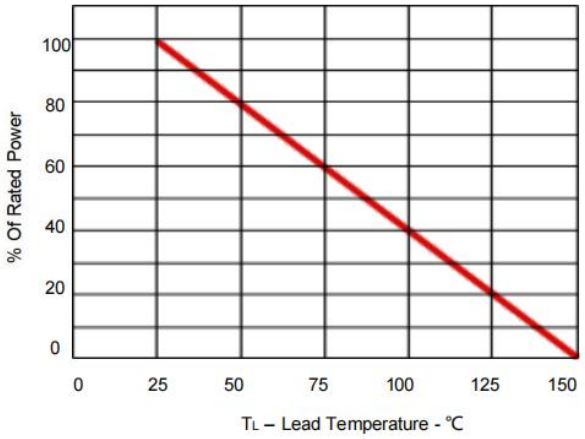


Fig 2.Power Derating Curve

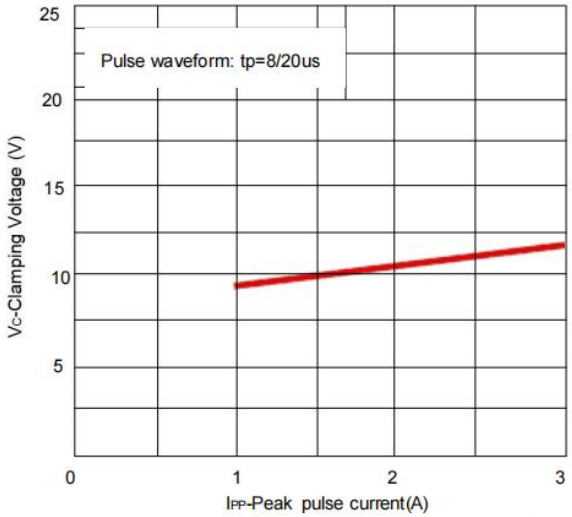


Fig 3. Clamping voltage vs. Peak pulse current

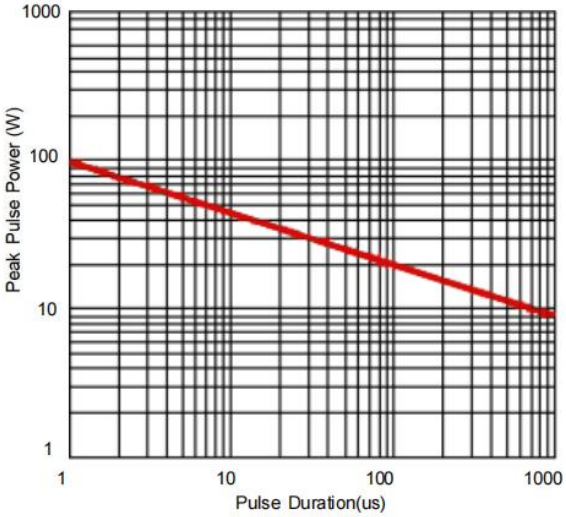


Fig 4. Non Repetitive Peak Pulse Power vs. Pulse time

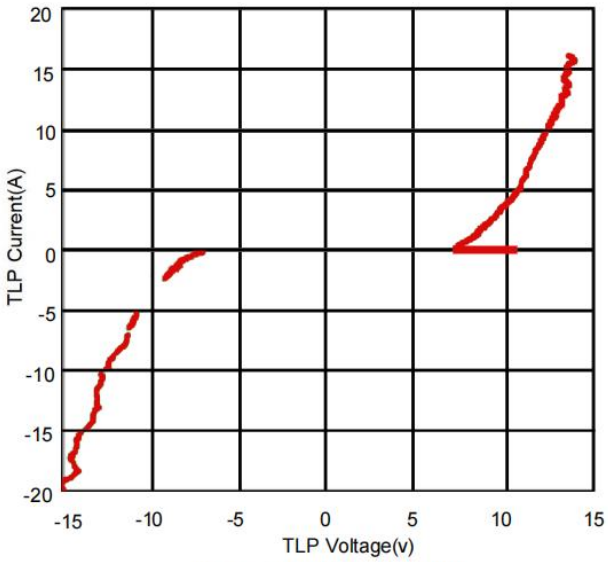
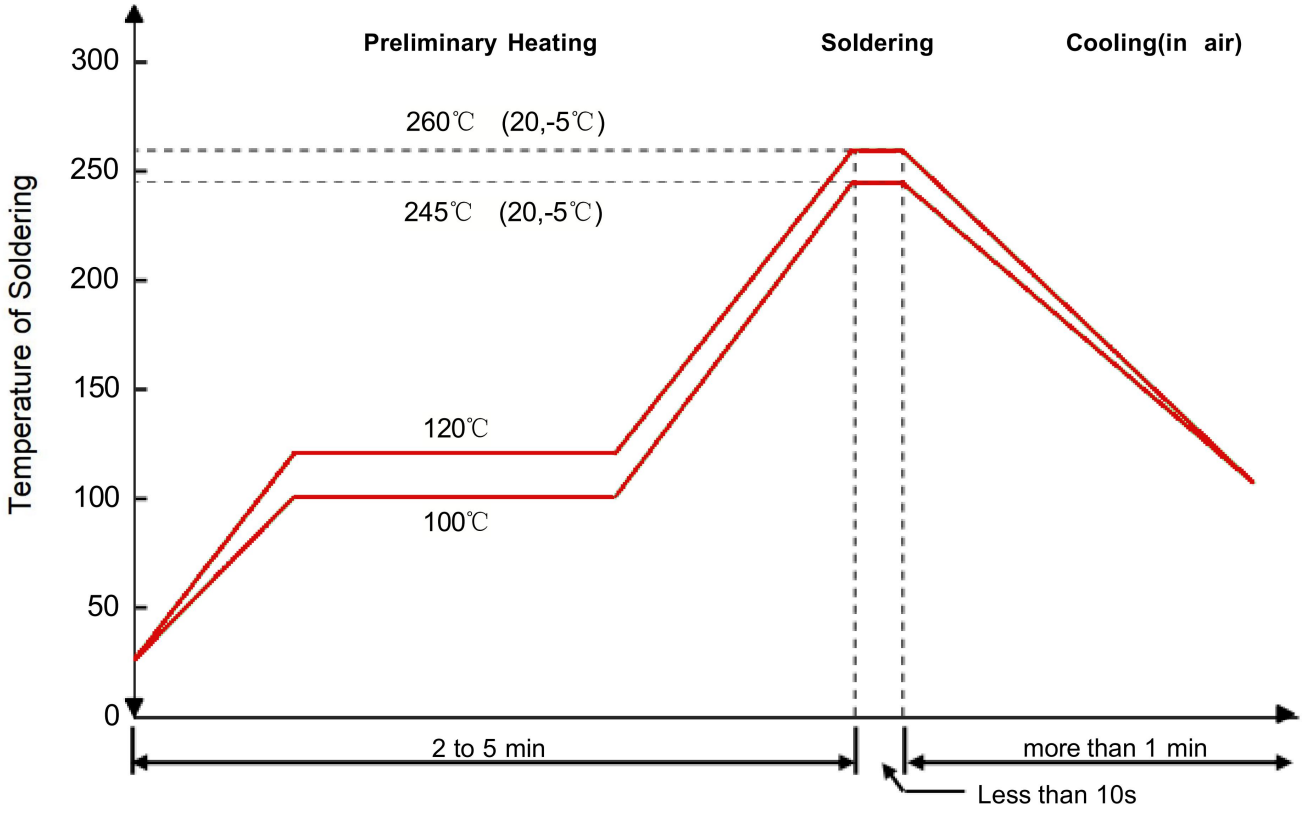


Fig 5. TLP Measurement

Solder Reflow Recommendation



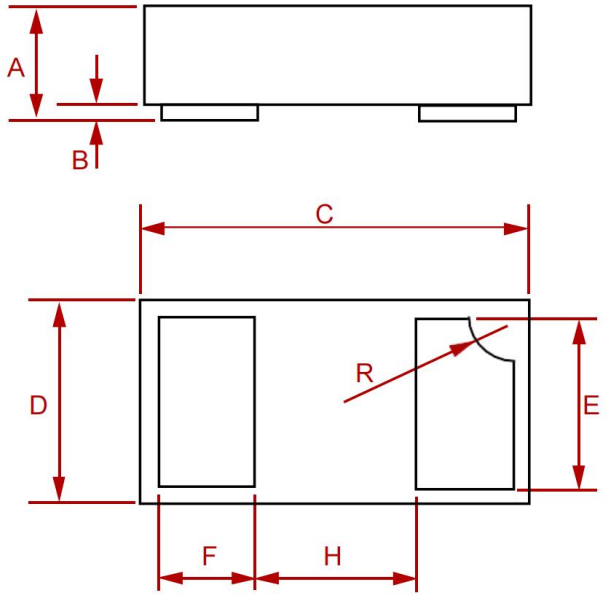
Remark: Pb free for 260℃; Pb for 245℃.

PCB Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

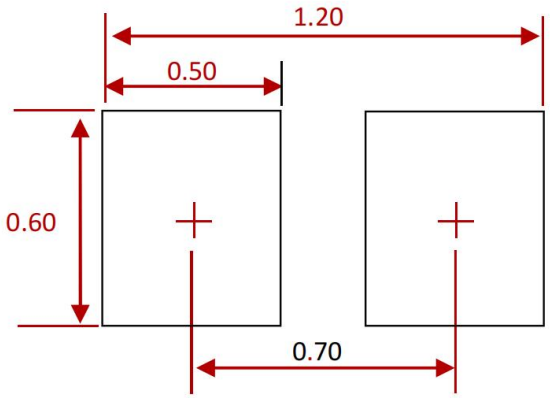
- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

PACKAGE MECHANICAL DATA



Dim	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.0125	0.02	0.32	0.52
B	0.000	0.002	0.00	0.05
C	0.037	0.043	0.95	1.080
D	0.022	0.027	0.55	0.680
E	0.016	0.024	0.40	0.60
F	0.008	0.012	0.20	0.30
H	0.015Typ.		0.40Typ.	
R	0.001	0.005	0.05	0. 15

Suggested Pad Layout



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

REEL SPECIFICATION

P/N	PKG	QTY
ESD9B5VL-MS	DFN-1006	10000

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