裕太微电子
Motorcomm

Motorcomm
YT9215RB Datasheet

LAYER 2 MANAGED 5+2 PORT 10/100/1000M SWITCH CONTROLLER

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General Description

YT9215RB is a LQFP128 E-PAD, high-performance 5+2-port Gigabit Ethernet switch. It integrates five PHY ports support 1000Base-T/100Base-TX/10Base-Te, and supports two extra MAC ports for specific applications which support MII/RMII/RGMII. YT9215RB is also embedded with a RSIC-V microprocessor.

The integrated GIGA-PHY complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE standard 802.3 and also support Motorcomm proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners. LRE100-4 in extended cable length applications up to 400 meter at 100Mbps over CAT5E cable.

The Extension GMAC1 and Extension GMAC2 of the YT9215RB support xMII for connecting with an external PHY, MAC, external CPU or RISC in specific applications. The xMII refer to Reduced Gigabit Media Independent Interface (RGMII), Media Independent Interface (MII), and Reduced Media Independent Interface (RMII). YT9215RB integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each of the entries can be configured as a static entry.

YT9215RB supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-and-port-based, VLAN translation ,Flow-based capability，and MAC-based, IP-subnet-based VLAN can be supported by configuration It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

The YT9215RB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. The YT9215RB supports storm control.

In order to support flexible traffic classification, the YT9215RB supports 384-hardware entry ACL rule check and multiple actions options. The 384 entries are composed of 48 rows, each row has 8 entries. To support long rule, rule extension is supported by any combinations of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority/DSCP value in 802.1q/Q tag, and rate policing.

Key Features

- High performance, nonblocking, 7 port Ethernet Switch integrating:
  - Five 10/100/1000Mbps PHYs with Advanced Virtual Cable Tester (VCT) diagnostic features
  - Each PHY supports 10/100/1000M full duplex connectivity (half duplex only supported in 10/100M mode)
  - Full duplex operation with IEEE 802.3x flow control and half duplex operation with backpressure
- Interface
  - Embedded 5-port 1000/100Base-T/ 10Base-Te PHY
  - Embedded two RGMII/MII/RMII interface
- Advanced Features
  - Supports parallel LED or serial LED outputs
  - Supports SPI/MDIO/I2C Slave interface
  - Supports MDIO/I2C Master interface
  - Supports 1 interrupt output to external CPU for notification
  - Supports 64K-byte EEPROM space for configuration
  - Link On Cable Length Power Saving
  - Link Down Power Saving
  - Supports 9K byte jumbo frames
- Supports 2 IEEE 802.3ad Link aggregation port groups
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Unknown DA filter mask
  - Supports Port Isolation
  - Supports Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
  - Supports DOS attack prevent
- Control, Management and Statistics
  - Supports RFC MIB Counters
    - MIB-II (RFC 1213)
    - Ethernet-Like MIB (RFC 3635)
    - Interface Group MIB (RFC 2863)
    - RMON (RFC 2819)
    - Bridge MIB (RFC 1493)
    - Bridge MIB Extension (RFC 2674)
  - Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
  - Supports Loop Detection
- Packet Process Engine
  - Supports 802.1Q VLANs
  - Supports 4K VLANs
  - Supports untag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision

- Supports Port based, Tag based, and Protocol based VLAN
- Supports per port egress VLAN tagging and untagging
- Supports IEEE 802.1D/s/w Spanning Tree Protocols
- Support Multicast VLAN (MVR)
- Supports IVL, SVL, and IVL/SVL
- Supports IEEE 802.1ad Stacking VLAN
- Support VLAN translation (1:1/2:1/2:2/ N:1/1:N)
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Supports ACL Rules
- Supports Hardware/Software IGMP/ MLD Snooping
  - Supports Fast Leave
  - Support IGMPV1/V2/V3
  - Static/Dynamic Router port
- Mirror
  - Port based mirror
  - Flow based mirror
- Support reserved multicast control
- Support WOL

- Quality of Service (QoS)
  - Supports Queue based DWRR/SP, packet/byte modes are both supported for DWRR
  - Support min-max queue based shaping, packet/byte modes are both supported
  - Support single token bucket for port based shaping, packet/byte modes are both supported
  - Supports per port Input Bandwidth Control, packet/byte modes are both supported
  - trTCM color aware/blind packet/byte modes
  - Traffic classification based on multiple source type
  - Support 8 unicast queues and 4 multicast queues for each port
  - Tail drop is supported for UQ/MQ, WRED is supported for UQ
- Microprocessor
  - Integrated RISC-V microprocessor
  - Supports Flash Interface (Dual mode/Single mode)
- 25MHz crystal or 3.3V OSC input
- TQFP 128-pin E-PAD package

Block Diagram

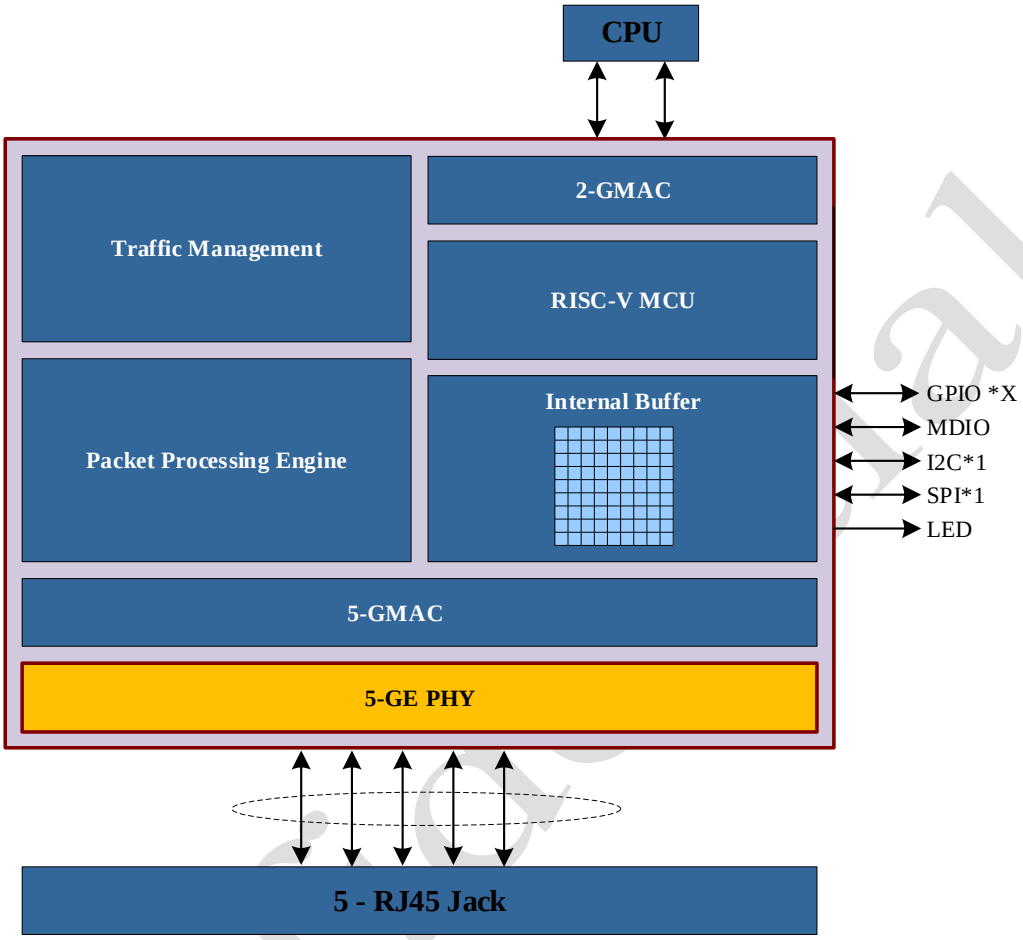

Figure 1. Block Diagram

System Applications

- 5-Port 1000Base-T + 2-Port RGMII
- 5-Port 1000Base-T Router with Single MII/RGMII
- 5-Port 1000Base-T Router with Dual MII/RGMII
- 5-Port 1000Base-T NVR
- 5-Port 1000Base-T ONU

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Revision History

Revision	Release Date	Summary
Draft_01	2022/10/09	First version.
Draft_02	2022/12/10	
Draft_03	2022/12/31	
Draft_04	2023/01/15	
Draft_05	2023/02/16	1. Revised the description in section 2; 2. Add section 3 and 4.

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1.1. Pin Assignment

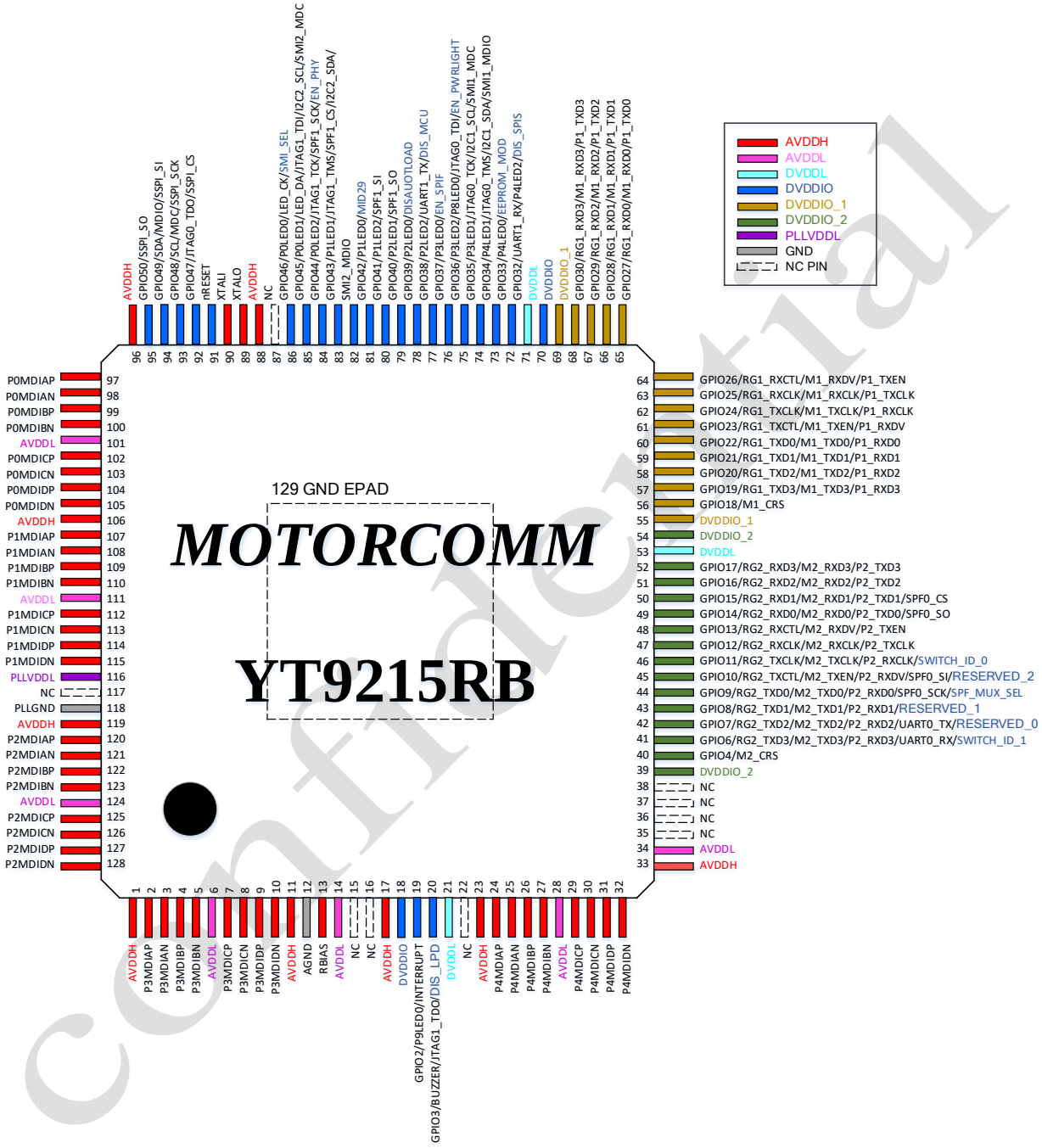


Figure 2. Pin Assignment

1.2. Pin Assignment Table

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground pin
- PU: Internal pull up
- LI: Latched Input During Power UP
- OD: Open Drain
- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power pin
- AG: Analog Ground pin
- PD: Internal pull down
- XT: Crystal Related

Table 1. Pin Assignment

No.	Pin Name	Type
1	AVDDH	AP
2	P3MDIAP	AIO
3	P3MDIAN	AIO
4	P3MDIBP	AIO
5	P3MDIBN	AIO
6	AVDDL	AP
7	P3MDICP	AIO
8	P3MDICN	AIO
9	P3MDIDP	AIO
10	P3MDIDN	AIO
11	AVDDH	AP
12	AGND	AG
13	RBIAS	AO
14	AVDDL	AP
15	NC	–
16	NC	–
17	AVDDH	AP
18	DVDDIO	P
19	GPIO2/P9LED0/INTERRUPT	IO/PU/OD
20	GPIO3/BUZZER/JTAG1_TDO/	IO/LI/

No.	Pin Name	Type
	DIS_LPD	PU
21	DVDDL	P
22	NC	–
23	AVDDH	AP
24	P4MDIAP	AIO
25	P4MDIAN	AIO
26	P4MDIBP	AIO
27	P4MDIBN	AIO
28	AVDDL	AP
29	P4MDICP	AIO
30	P4MDICN	AIO
31	P4MDIDP	AIO
32	P4MDIDN	AIO
33	AVDDH	AP
34	AVDDL	AP
35	NC	–
36	NC	–
37	NC	–
38	NC	–
39	DVDDIO_2	P
40	GPIO4/M2_CRS	IO/PD

No.	Pin Name	Type
41	GPIO6/RG2_TXD3/M2_TXD3/P2_RXD3/UART0_RX/SWITCH_ID_1	IO/LI/PD
42	GPIO7/RG2_TXD2/M2_TXD2/P2_RXD2/UART0_TX/RESERVED_0	IO/PU
43	GPIO8/RG2_TXD1/M2_TXD1/P2_RXD1/RESERVED_1	IO/PU
44	GPIO9/RG2_TXD0/M2_TXD0/P2_RXD0/SPF0_SCK/SPF_MUX_SEL	IO/LI/PD
45	GPIO10/RG2_TXCTL/M2_TXEN/P2_RXDV/SPF0_SI/RESERVED_2	IO/PD
46	GPIO11/RG2_TXCLK/M2_TXCLK/P2_RXCLK/SWITCH_ID_0	IO/LI/PD
47	GPIO12/RG2_RXCLK/M2_RXCLK/P2_TXCLK	IO/PU
48	GPIO13/RG2_RXCTL/M2_RXDV/P2_TXEN	IO/PU
49	GPIO14/RG2_RXD0/M2_RXD0/P2_TXD0/SPF0_SO	IO/PU
50	GPIO15/RG2_RXD1/M2_RXD1/P2_TXD1/SPF0_CS	IO/PU
51	GPIO16/RG2_RXD2/M2_RXD2/P2_TXD2	IO/PU
52	GPIO17/RG2_RXD3/M2_RXD3/P2_TXD3	IO/PU
53	DVDDL	P
54	DVDDIO_2	P
55	DVDDIO_1	P
56	GPIO18/M1_CRS	IO/PD
57	GPIO19/RG1_TXD3/M1_TXD3/P1_RXD3	IO/PU
58	GPIO20/RG1_TXD2/M1_TXD2/P1_RXD2	IO/PU
59	GPIO21/RG1_TXD1/M1_TXD1/P1_RXD1	IO/PU
60	GPIO22/RG1_TXD0/M1_TXD0/P1_RXD0	IO/PU
61	GPIO23/RG1_TXCTL/M1_TXEN/P1_RXDV	IO/PD
62	GPIO24/RG1_TXCLK/M1_TXCLK/P1_RXCLK	IO/PU
63	GPIO25/RG1_RXCLK/M1_RXCLK/P1_TXCLK	IO/PU
64	GPIO26/RG1_RXCTL/M1_RXDV/P1_TXEN	IO/PU
65	GPIO27/RG1_RXD0/M1_RXD0/P1_TXD0	IO/PU
66	GPIO28/RG1_RXD1/M1_RXD1/P1_TXD1	IO/PU
67	GPIO29/RG1_RXD2/M1_RXD2/P1_TXD2	IO/PU
68	GPIO30/RG1_RXD3/M1_RXD3/P1_TXD3	IO/PU
69	DVDDIO_1	P
70	DVDDIO	P
71	DVDDL	P
72	GPIO32/UART1_RX/P4LED2/DIS_SPIS	IO/LI/PU
73	GPIO33/P4LED0/EEPROM_MOD	IO/LI/PU
74	GPIO34/P4LED1/JTAG0_TMS/I2C1_SDA/SMI1_MDIO	IO/PU/OD
75	GPIO35/P3LED1/JTAG0_TCK/I2C1_SCL/SMI1_MDC	IO/PU/OD
76	GPIO36/P3LED2/P8LED0/JTAG0_TDI/EN_PWRLIGHT	IO/LI/PU
77	GPIO37/P3LED0/EN_SPIF	IO/LI/PU
78	GPIO38/P2LED2/UART1_TX/DIS_MCU	IO/LI/PU
79	GPIO39/P2LED0/DISAUOTLOAD	IO/LI/PU
80	GPIO40/P2LED1/SPF1_SO	IO/PU
81	GPIO41/P1LED2/SPF1_SI	IO/PU
82	GPIO42/P1LED0/MID29	IO/LI/

No.	Pin Name	Type
		PU
83	GPIO43/P1LED1/JTAG1_TMS/SPF1_CS/I2C2_SDA/SMI2_MDIO	IO/PU/OD
84	GPIO44/P0LED2/JTAG1_TCK/SPF1_SCK/EN_PHY	IO/LI/PU
85	GPIO45/P0LED1/LED_DA/JTAG1_TDI/I2C2_SCL/SMI2_MDC	IO/PU/OD
86	GPIO46/P0LED0/LED_CK/SMI_SEL	IO/LI/PU
87	NC	–
88	AVDDH	AP
89	XTALO	XT
90	XTALI	XT
91	nRESET	AI/PU
92	GPIO47/JTAG0_TDO/SSPI_CS	IO/PU
93	GPIO48/SCL/MDC/SSPI_SCK	IO/PU/OD
94	GPIO49/SDA/MDIO/SSPI_SI	IO/PU/OD
95	GPIO50/SSPI_SO	IO/PU
96	AVDDH	AP
97	P0MDIAP	AIO
98	P0MDIAN	AIO
99	P0MDIBP	AIO
100	P0MDIBN	AIO
101	AVDDL	AP
102	P0MDICP	AIO

No.	Pin Name	Type
103	P0MDICN	AIO
104	P0MDIDP	AIO
105	P0MDIDN	AIO
106	AVDDH	AP
107	P1MDIAP	AIO
108	P1MDIAN	AIO
109	P1MDIBP	AIO
110	P1MDIBN	AIO
111	AVDDL	AP
112	P1MDICP	AIO
113	P1MDICN	AIO
114	P1MDIDP	AIO
115	P1MDIDN	AIO
116	PLLVDDL	AP
117	NC	–
118	PLLGND	AG
119	AVDDH	AP
120	P2MDIAP	AIO
121	P2MDIAN	AIO
122	P2MDIBP	AIO
123	P2MDIBN	AIO
124	AVDDL	AP
125	P2MDICP	AIO
126	P2MDICN	AIO
127	P2MDIDP	AIO
128	P2MDIDN	AIO
129	GND EPAD	G

2. Pin Description

2.1. MDI Interface Pins

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
97	P0MDIAP	AIO	Port 0 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
98	P0MDIAN	AIO	
99	P0MDIBP	AIO	Port 0 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
100	P0MDIBN	AIO	
102	P0MDICP	AIO	Port 0 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
103	P0MDICN	AIO	
104	P0MDIDP	AIO	Port 0 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
105	P0MDIDN	AIO	
107	P1MDIAP	AIO	Port 1 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
108	P1MDIAN	AIO	
109	P1MDIBP	AIO	Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
110	P1MDIBN	AIO	
112	P1MDICP	AIO	Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
113	P1MDICN	AIO	
114	P1MDIDP	AIO	Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
115	P1MDIDN	AIO	
120	P2MDIAP	AIO	Port 2 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
121	P2MDIAN	AIO	
122	P2MDIBP	AIO	Port 2 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
123	P2MDIBN	AIO	
125	P2MDICP	AIO	Port 2 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
126	P2MDICN	AIO	
127	P2MDIDP	AIO	Port 2 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
128	P2MDIDN	AIO	
2	P3MDIAP	AIO	Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
3	P3MDIAN	AIO	
4	P3MDIBP	AIO	Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
5	P3MDIBN	AIO	
7	P3MDICP	AIO	Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
8	P3MDICN	AIO	
9	P3MDIDP	AIO	Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
10	P3MDIDN	AIO	

24	P4MDIAP	AIO	Port 4 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
25	P4MDIAN	AIO	
26	P4MDIBP	AIO	Port 4 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
27	P4MDIBN	AIO	
29	P4MDICP	AIO	Port 4 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
30	P4MDICN	AIO	
31	P4MDIDP	AIO	Port 4 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
32	P4MDIDN	AIO	

2.2. RGMII Interface Pins

Table 3. RGMII 1 Interface Pins

No.	Pin Name	Type	Description
62	RG1_TXCLK	IO/PU	RGMII 1 transmit reference clock will be 125Mhz, 25MHz, or 2.5MHz depending on speed. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively. This pin is output in RGMII mode.
61	RG1_TXCTL	IO/PD	RGMII 1 Transmit Control Signal from the MAC. This pin is output in RGMII mode.
57	RG1_TXD3	IO/PU	RGMII 1 transmit Data. Data is transmitted from MAC to PHY via TXD[3:0] . These pins are output in RGMII mode.
58	RG1_TXD2	IO/PU	
59	RG1_TXD1	IO/PU	
60	RG1_TXD0	IO/PU	
63	RG1_RXCLK	IO/PU	RGMII 1 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. This pin is input in RGMII mode.
64	RG1_RXCTL	IO/PU	RGMII 1 receive Control Signal to the MAC. This pin is input in RGMII mode.
68	RG1_RXD3	IO/PU	RGMII 1 receive Data. Data is transmitted from PHY to MAC via RXD[3:0]. These pins are input in RGMII mode.
67	RG1_RXD2	IO/PU	
66	RG1_RXD1	IO/PU	
65	RG1_RXD0	IO/PU	

Table 4. RGMII 2 Interface Pins

No.	Pin Name	Type	Description
46	RG2_TXCLK	IO/LI/PD	RGMII 2 transmit reference clock will be 125Mhz, 25MHz,

			or 2.5MHz depending on speed. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively. This pin is output in RGMII mode.
45	RG2_TXCTL	IO/PD	RGMII 2 Transmit Control Signal from the MAC. This pin is output in RGMII mode.
41	RG2_TXD3	IO/LI/PD	RGMII 2 transmit Data. Data is transmitted from MAC to PHY via TXD[3:0]. These pins are output in RGMII mode.
42	RG2_TXD2	IO/PU	
43	RG2_TXD1	IO/PU	
44	RG2_TXD0	IO/LI/PD	
47	RG2_RXCLK	IO/PU	RGMII 2 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. This pin is input in RGMII mode.
48	RG2_RXCTL	IO/PU	RGMII 2 receive Control Signal to the MAC. This pin is input in RGMII mode.
52	RG2_RXD3	IO/PU	RGMII 2 receive Data. Data is transmitted from PHY to MAC via RXD[3:0]. These pins are input in RGMII mode.
51	RG2_RXD2	IO/PU	
50	RG2_RXD1	IO/PU	
49	RG2_RXD0	IO/PU	

2.3. MII Interface Pins

Table 5. MII1 Interface Pins

No.	Pin Name	Type	Description
62	M1_TXCLK/ P1_RXCLK	IO/PU	1. M_TXCLK Pin in MII MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. 2. P_RXCLK Pin in MII PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
61	M1_TXEN/ P1_RXDV	IO/PD	1. M_TXEN Pin in MII MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXCLK. 2. P_RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous output is

			asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXCLK.
57	M1_TXD3/ P1_RXD3	IO/PU	1. M_TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXCLK. 2. P_RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXCLK.
58	M1_TXD2/ P1_RXD2	IO/PU	
59	M1_TXD1/ P1_RXD1	IO/PU	
60	M1_TXD0/ P1_RXD0	IO/PU	
63	M1_RXCLK/ P1_TXCLK	IO/PU	1. M_RXCLK Pin in MII 1 MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. 2. P_TXCLK Pin in MII PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
64	M1_RXDV/ P1_TXEN	IO/PU	1. M_RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD bus. M_RXDV is synchronous to M_RXCLK. 2. P_TXEN Pin in MII PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXCLK.
68	M1_RXD3/ P1_TXD3	IO/PU	1. M_RXD[3:0] Pin in MII MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXCLK. 2. P_TXD[3:0] Pin in MII 1 PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXCLK .
67	M1_RXD2/ P1_TXD2	IO/PU	
66	M1_RXD1/ P1_TXD1	IO/PU	
65	M1_RXD0/ P1_TXD0	IO/PU	

Table 6. MII2 Interface Pins

No.	Pin Name	Type	Description

46	M2_TXCLK/ P2_RXCLK	IO/LI/PD	1. M_TXCLK Pin in MII MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. 2. P_RXCLK Pin in MII PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
45	M2_TXEN/ P2_RXDV	IO/PD	1. M_TXEN Pin in MII MAC Mode. MII Transmit Enable.The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXCLK. 2. P_RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXCLK.
41	M2_TXD3/ P2_RXD3	IO/LI/PD	1. M_TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXCLK. 2. P_RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXCLK.
42	M2_TXD2/ P2_RXD2	IO/PU	
43	M2_TXD1/ P2_RXD1	IO/PU	
44	M2_TXD0/ P2_RXD0	IO/LI/PD	
47	M2_RXCLK/ P2_TXCLK	IO/PU	1. M_RXCLK Pin in MII 1 MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. 2. P_TXCLK Pin in MII PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
48	M2_RXDV/ P2_TXEN	IO/PU	1. M_RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD bus. M_RXDV is synchronous to M_RXCLK. 2. P_TXEN Pin in MII PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXCLK.
52	M2_RXD3/ P2_TXD3	IO/PU	1. M_RXD[3:0] Pin in MII MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to

51	M2_RXD2/ P2_TXD2	IO/PU	M_RXCLK. 2. P_TXD[3:0] Pin in MII 1 PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXCLK .
50	M2_RXD1/ P2_TXD1	IO/PU	
49	M2_RXD0/ P2_TXD0	IO/PU	

2.4. RMII Interface Pins

Table 7. RMII1 Interface Pins

No.	Pin Name	Type	Description
62	M1_TXCLK/ P1_RXCLK	IO/PU	REFCLK pin in RMII Mode. 1. In RMII MAC Mode, REFCLK is an input pin. 2. In RMII PHY Mode, REFCLK is an output pin. REF_CLK is a 50Mhz clock that provides the timing reference for RXDV, RXD[1:0], TXEN, TXD[1:0].
61	M1_TXEN/ P1_RXDV	IO/PD	1. TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 2. RXDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK.
59	M1_TXD1 / P1_RXD1	IO/PU	1. TXD[1:0] Pin in RMII MAC Mode, synchronous to REFCLK. 2. RXD[1:0] Pin in RMII PHY Mode, synchronous to REFCLK.
60	M1_TXD0 / P1_RXD0	IO/PU	
64	M1_RXDV/ P1_TXEN	IO/PU	1. RXDV Pin in RMII MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. 2. TXEN Pin in RMII PHY Mode. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK.
66	M1_RXD1/ P1P_TXD1	IO/PU	1. RXD[1:0] Pin in RMII MAC Mode, is synchronous to RXC. 2. TXD[1:0] Pin in RMII PHY Mode, is synchronous to TXC .
65	M1_RXD0/ P1_TXD0	IO/PU	

Table 8. RMII2 Interface Pins

No.	Pin Name	Type	Description
46	M2_REFCLK / P2_REFCLK	IO/LI/PD	REFCLK pin in RMII Mode. 1. In RMII MAC Mode, REFCLK is an input pin. 2. In RMII PHY Mode, REFCLK is a output pin. REF_CLK is a 50Mhz clock that provides the timing reference for RXDV, RXD[1:0], TXEN, TXD[1:0].
45	M2_TXEN/ P2_RXDV	IO/PD	3. TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 1. RXDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK.
43	M2_TXD1/ P2_RXD1	IO/PU	1. TXD[1:0] Pin in RMII MAC Mode, synchronous to REFCLK. 2. RXD[1:0] Pin in RMII PHY Mode, synchronous to REFCLK.
44	M2_TXD0/ P2_RXD0	IO/PD	
48	M2_RXDV/ P2_TXEN	IO/PU	1. RXDV Pin in RMII MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. 2. TXEN Pin in RMII PHY Mode. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK.
50	M2_RXD1/ P2_TXD1	IO/PU	1. RXD[1:0] Pin in RMII MAC Mode, is synchronous to RXC. 2. TXD[1:0] Pin in RMII PHY Mode, is synchronous to TXC .
49	M2_RXD0/ P2_TXD0	IO/PU	

2.5. Parallel LED Pins

Table 9. Parallel LED Pins

No.	Pin Name	Type	Description
72	P4LED2	IO/LI/PU	Default port 4 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM

74	P4LED1	IO/PU/OD	Default port 4 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
73	P4LED0	IO/LI/PU	Default port 4 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
76	P3LED2	IO/LI/PU	Default port 3 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
75	P3LED1	IO/PU/OD	Default port 3 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
77	P3LED0	IO/LI/PU	Default port 3 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
78	P2LED2	IO/LI/PU	Default port 2 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
80	P2LED1	IO/PU	Default port 2 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
79	P2LED0	IO/LI/PU	Default port 2 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
81	P1LED2	IO/PU	Default port 1 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
83	P1LED1	IO/PU/OD	Default port 1 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
82	P1LED0	IO/LI/PU	Default port 1 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
84	P0LED2	IO/LI/PU	Default port 0 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
85	P0LED1	IO/PU/OD	Default port 0 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
86	P0LED0	IO/LI/PU	Default port 0 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

2.6. Serial LED Pins

Table 10. Serial LED Pins

No.	Pin Name	Type	Description
86	LED_CK	IO/LI/PU	Serial Mode LED Clock Signal.
85	LED_DA	IO/PU/OD	Serial Mode LED Data Signal.

2.7. SPI FLASH Pins

Table 11. SPI FLASH 0 Interface Pins

No.	Pin Name	Type	Description
50	SPF0_CS	IO/PU	SPI FLASH chip select signal.
49	SPF0_SO	IO/PU	In Serial I/O Mode, SPI Serial FLASH Serial Data Output (YT9215RB input pin) In Dual I/O Mode, SPI FLASH bi-directional pin (this is MSB)
45	SPF0_SI	IO/LI/PD	In Serial I/O Mode SPI Serial FLASH Serial Data Input (YT9215RB output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
44	SPF0_SCK	IO/PD	SPI FLASH Clock.

Table 12. SPI FLASH 1 Interface Pins

No.	Pin Name	Type	Description
83	SPF1_CS	IO/PU/OD	SPI FLASH chip select signal.
80	SPF1_SO	IO/PU	In Serial I/O Mode, SPI Serial FLASH Serial Data Output (YT9215RB input pin) In Dual I/O Mode, SPI FLASH bi-directional pin (this is MSB)
81	SPF1_SI	IO/PU	In Serial I/O Mode SPI Serial FLASH Serial Data Input (YT9215RB output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
84	SPF1_SCK	IO/LI/PU	SPI FLASH Clock.

2.8. JTAG Interface Pins

Table 13. JTAG 0 Interface Pins

No.	Pin Name	Type	Description
92	JTAG0_TDO	IO/PU	Test Data Out.
76	JTAG0_TDI	IO/LI/PU	Test Data In.
74	JTAG0_TMS	IO/PU/OD	Test Mode Select.
75	JTAG0_TCK	IO/PU/OD	Test Clock.

Table 14. JTAG 1 Interface Pins

No.	Pin Name	Type	Description
20	JTAG1_TDO	IO/PU	Test Data Out.
85	JTAG1_TDI	IO/PU/OD	Test Data In.
83	JTAG1_TMS	IO/PU/OD	Test Mode Select.
84	JTAG1_TCK	IO/LI/PU	Test Clock.

2.9. UART Interface Pins

Table 15. UART 0 Interface Pins

No.	Pin Name	Type	Description
41	UART0_RX	IO/LI/PD	UART RX pin.
42	UART0_TX	IO/LI/PU	UART TX pin.

Table 16. UART 1 Interface Pins

No.	Pin Name	Type	Description
72	UART1_RX	IO/LI/PU	UART RX pin.
78	UART1_TX	IO/LI/PU	UART TX pin.

2.10. Master I2C Interface Pins

Table 17. Master I2C 1 Interface Pins

No.	Pin Name	Type	Description
75	I2C1_SCL	IO/PU/OD	SCL pin in Group1 Master I2C.
74	I2C1_SDA	IO/PU/OD	SDA pin in Group1 Master I2C.

Table 18. Master I2C 2 Interface Pins

No.	Pin Name	Type	Description
85	I2C2_SCL	IO/LI/PU	SCL pin in Group2 Master I2C.
83	I2C2_SDA	IO/PU/OD	SDA pin in Group2 Master I2C.

2.11. Master MDIO Interface Pins

Table 19. Master MDIO 1 Interface Pins

No.	Pin Name	Type	Description
75	SMI1_MDC	IO/PU/OD	MDC pin in Group1 Master SMI.
74	SMI1_MDIO	IO/PU/OD	MDIO pin in Group1 Master SMI.

Table 20. Master MDIO 2 Interface Pins

No.	Pin Name	Type	Description
85	SMI2_MDC	IO/LI/PU	MDC pin in Group2 Master SMI.
83	SMI2_MDIO	IO/PU/OD	MDIO pin in Group2 Master SMI.

2.12. Management Interface Pins

Table 21. Management Interface Pins

No.	Pin Name	Type	Description
92	SSPI_CS	IO/PU	SPI slave Mode Chip Select Input.
93	SCL/ MDC/ SSPI_SCK	IO/PU/OD	1. EEPROM auto load mode serial clock output 2. I2C slave mode serial clock input 3. MDC/MDIO slave mode serial clock input 4. SPI slave Mode serial clock input
94	SDA/ MDIO/ SSPI_SI	IO/PU/OD	1. EEPROM auto load mode serial data input 2. I2C slave mode serial data 3. MDC/MDIO slave mode serial data 4. SPI slave Mode serial data input
95	SSPI_SO	IO/PU	SPI slave Mode serial data output

2.13. GPIO Pins

Table 22. GPIO Pins

No.	Pin Name	Type	Description
19	GPIO2	IO/PU/OD	General Purpose Input/Output Interfaces IO2.
20	GPIO3	IO/PU	General Purpose Input/Output Interfaces IO3.
40	GPIO4	IO/PD	General Purpose Input/Output Interfaces IO4.
41	GPIO6	IO/LI/PD	General Purpose Input/Output Interfaces IO6.
42	GPIO7	IO/LI/PU	General Purpose Input/Output Interfaces IO7.
43	GPIO8	IO/LI/PU	General Purpose Input/Output Interfaces IO8.
44	GPIO9	IO/LI/PD	General Purpose Input/Output Interfaces IO9.
45	GPIO10	IO/LI/PD	General Purpose Input/Output Interfaces IO10.
46	GPIO11	IO/LI/PD	General Purpose Input/Output Interfaces IO11.
47	GPIO12	IO/PU	General Purpose Input/Output Interfaces IO12.
48	GPIO13	IO/PU	General Purpose Input/Output Interfaces IO13
49	GPIO14	IO/PU	General Purpose Input/Output Interfaces IO14.

50	GPIO15	IO/PU	General Purpose Input/Output Interfaces IO15.
51	GPIO16	IO/PU	General Purpose Input/Output Interfaces IO16.
52	GPIO17	IO/PU	General Purpose Input/Output Interfaces IO17.
56	GPIO18	IO/PD	General Purpose Input/Output Interfaces IO18.
57	GPIO19	IO/PU	General Purpose Input/Output Interfaces IO19.
58	GPIO20	IO/PU	General Purpose Input/Output Interfaces IO20.
59	GPIO21	IO/PU	General Purpose Input/Output Interfaces IO21.
60	GPIO22	IO/PU	General Purpose Input/Output Interfaces IO22.
61	GPIO23	IO/PD	General Purpose Input/Output Interfaces IO23.
62	GPIO24	IO/PU	General Purpose Input/Output Interfaces IO24.
63	GPIO25	IO/PU	General Purpose Input/Output Interfaces IO25.
64	GPIO26	IO/PU	General Purpose Input/Output Interfaces IO26.
65	GPIO27	IO/PU	General Purpose Input/Output Interfaces IO27.
66	GPIO28	IO/PU	General Purpose Input/Output Interfaces IO28.
67	GPIO29	IO/PU	General Purpose Input/Output Interfaces IO29.
68	GPIO30	IO/PU	General Purpose Input/Output Interfaces IO30.
72	GPIO32	IO/LI/PU	General Purpose Input/Output Interfaces IO32.
73	GPIO33	IO/LI/PU	General Purpose Input/Output Interfaces IO33.
74	GPIO34	IO/PU/OD	General Purpose Input/Output Interfaces IO34.
75	GPIO35	IO/PU/OD	General Purpose Input/Output Interfaces IO35.
76	GPIO36	IO/LI/PU	General Purpose Input/Output Interfaces IO36.
77	GPIO37	IO/LI/PU	General Purpose Input/Output Interfaces IO37.
78	GPIO38	IO/LI/PU	General Purpose Input/Output Interfaces IO38.
79	GPIO39	IO/LI/PU	General Purpose Input/Output Interfaces IO39.
80	GPIO40	IO/PU	General Purpose Input/Output Interfaces IO40.
81	GPIO41	IO/PU	General Purpose Input/Output Interfaces IO41.
82	GPIO42	IO/LI/PU	General Purpose Input/Output Interfaces IO42.
83	GPIO43	IO/PU/OD	General Purpose Input/Output Interfaces IO43.
84	GPIO44	IO/LI/PU	General Purpose Input/Output Interfaces IO44.
85	GPIO45	IO/PU/OD	General Purpose Input/Output Interfaces IO45.
86	GPIO46	IO/LI/PU	General Purpose Input/Output Interfaces IO46.
92	GPIO47	IO/PU	General Purpose Input/Output Interfaces IO47.
93	GPIO48	IO/PU/OD	General Purpose Input/Output Interfaces IO48.
94	GPIO49	IO/PU/OD	General Purpose Input/Output Interfaces IO49.
95	GPIO50	IO/PU	General Purpose Input/Output Interfaces IO50.

2.14. Configuration Pins

Table 23. Configuration Pins

No.	Pin Name	Type	Description
20	DIS_LPD	IO/LI/PU	Loop detection configuration Pull Up: disable LPD. Pull Down: enable LPD.
41	SWITCH_ID_1	IO/LI/PD	Switch_ID[1:0] for slave MDC/MDIO format.
46	SWITCH_ID_0	IO/LI/PD	
44	SPF_MUX_SEL	IO/PD	SPI FLASH Interface Position Select. Pull Up: Select Spi-Flash-1 pin 50\49\45\44. Pull Down: Select Spi-Flash-2 pin 83\80\81\84.
72	DIS_SPIS	IO/LI/PU	Disable Slave SPI Interface for External CPU Access YT9215RB Register Pull Up: Disable SPI Slave Interface and refer to [SMI_SEL] Pull Down: Enable SPI Slave Interface
73	EEPROM_MOD	IO/LI/PU	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~). Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16).
76	EN_PWRLIGHT	IO/LI/PU	Disable/Enable LED function When Powered On. Pull Up: Enable LED. Pull Down: Disable LED.
77	EN_SPIF	IO/LI/PU	Enable SPI FLASH Interface. Pull Up: Enable FLASH interface. Pull Down: Disable FLASH interface
78	DIS_MCU	IO/LI/PU	Disable Embedded MCU. Pull Up: Disable embedded MCU upon power on or reset Pull Down: Enable embedded MCU upon power on or reset
79	DISAUTOLOAD	IO/LI/PU	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset
82	MID29	IO/LI/PU	Slave SMI (MDC/MDIO) Device Address. Pull Up: Slave SMI (MDC/MDIO) Device Address is 0x1d Pull Down: Slave SMI (MDC/MDIO) Device Address is 0x0
84	EN_PHY	IO/LI/PU	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY
86	SMI_SEL	IO/LI/PU	EEPROM SMI/MII Management Interface Selection.

			Pull Up: EEPROM SMI interface when DIS_SPIS = 1 Pull Down: MII Management interface when DIS_SPIS = 1
42	RESERVED_0	–	Reserved. This pin must be pulled up to DVDDIO via an external 4.7k ohm resistor upon power on.
43	RESERVED_1	–	Reserved. This pin must be pulled up to DVDDIO via an external 4.7k ohm resistor upon power on.
45	RESERVED_2	–	Reserved. This pin must be pulled up to DVDDIO via an external 4.7k ohm resistor upon power on.

2.15. Power Related Pins

Table 24. Power Related Pins

No.	Pin Name	Type	Description
18,70	DVDDIO	P	Digital power 3.3V
55,69	DVDDIO_1	P	Digital power 3.3V for Extension Port 1
39,54	DVDDIO_2	P	Digital power 3.3V for Extension Port 2
21,53,71	DVDDL	P	Digital power 1.1V
1,11,17,23,33, 88,96,106,119	AVDDH	AP	Analog power 3.3V
6,14,28,34, 101,111,124	AVDDL	AP	Analog power 1.1V
116	PLLVDDL	AP	PLL Power 1.1V.
12	AGND	AG	Analog GND.
118	PLLGND	AG	PLL GND.
129	GND EPAD	G	GND

2.16. Clock Pins

Table 25. Clock Pins

No.	Pin Name	Type	Description
90	XTAL_I	XT	25MHz Crystal Input pin. If use external oscillator or clock from another device. 1. When connect an external 25Hhz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25Hhz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
89	XTAL_O	XT	25Mhz Crystal Output pin.

			If use external oscillator or clock from another device. 1. When connect an external 25Hhz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25Hhz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

2.17. Reset Pins

Table 26. Reset Pins

No.	Pin Name	Type	Description
91	nRESET	AI/PU	Hardware reset, active low. Requires an external pull-up resistor

2.18. Miscellaneous Pins

Table 27. Miscellaneous Pin

No.	Pin Name	Type	Description
15,16,22,35,36,37,38,87,117	NC	-	Not connect. Must be left floating in normal operation.

3. Integrated PHY Functional Overview

YT9215RB integrates five 10/100/1000M Giga PHY ports. Each PHY port support 1000Base-T, 100Base-TX, and 10Base-Te by four signal pairs, namely MDIAP/N, MDIBP/N, MDICP/N and MDIDP/N. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. For 1000Base-T, all four pairs are used in both directions at the same time. For 100Base-TX and 10Base-Te, only pairs MDIAP/N and MDIBP/N are used.

3.1. Transmit Encoder Modes

3.1.1. 1000BASE-T

In 1000BASE-T mode, the PHY port scrambles data bytes to be transmit from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT 5E UTP cable.

3.1.2. 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

3.1.3. 10BASE-Te

In 10BASE-Te mode, the PHY port transmits Manchester-encoded data.

3.2. Receive Decoder Modes

3.2.1. 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

3.2.2. 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to MAC interfaces after data stream delimiters have been translated.

3.2.3. 10BASE-Te

In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester then aligned.

3.3. Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The PHY port implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

3.4. NEXT Canceller

The 1000BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The PHY port uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The PHY port cancels NEXT by subtracting an estimate of these signals from the equalizer output.

3.5. Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000BASE-T environment than in 100BASE-TX due to the DC baseline shift in the transmit and receive signals. The YT8531S device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

3.6. Digital Adaptive Equalizer

The digital adaptive equalizer removes inter- symbol interference at the receiver. The digital adaptive equalizer takes signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

3.7. Auto-Negotiation

The integrated PHY port negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation

supports choosing the mode of operation automatically by comparing its own abilities and abilities received from link partner.

Auto negotiation is enabled for YT9215RB by default, and can be disabled by software control.

3.8. Auto Crossover and Polarity Correction

The integrated PHY port can detect and correct two types of cable errors: auto crossover of pairs within the UTP cable (between pair 0 and pair 1, and(or) between pair 2 and pair 3) and swapping of polarity within a pair.

4. General Function Description

4.1. Reset

4.1.1. Hardware Reset

YT9215RB have a hardware reset pin (nRESET) which is low active. The reset signal should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

The reset pin is also used for power on strapping. After reset is released, YT9215RB latches input value on strapping pins which are used as configuration information to provide flexible applications.

Table 28. Transceiver Interface

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

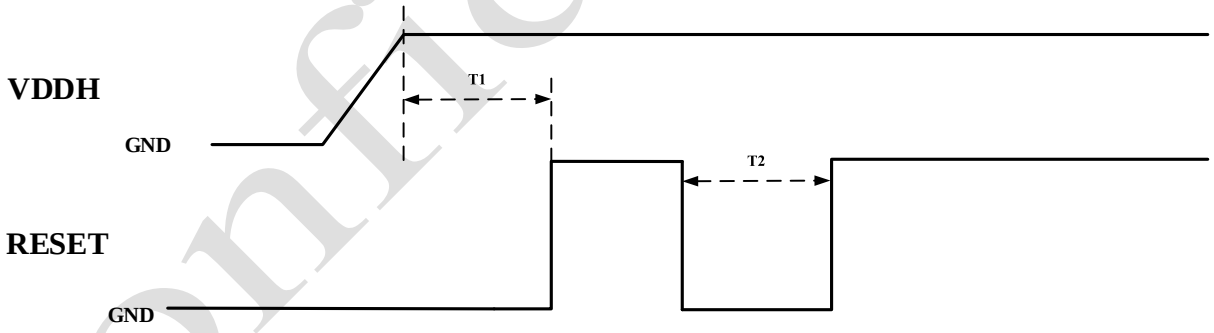


Figure 3. Reset Timing Diagram

4.1.2. Software Reset

The YT9215RB supports two software resets: a chip reset (CHIP_RESET) and a software reset (SW_RESET).

4.1.2.1. CHIP_RESET

4.1.2.2. SW_RESET

4.2. IEEE 802.3x Full Duplex Flow Control

The YT9215RB supports IEEE 802.3x flow control in 10/100/1000M full duplex modes. Flow control ability can be decided in two ways:

- When Auto-Negotiation is enabled, flow control ability depends on the result of Auto-Negotiation.
- When Auto-Negotiation is disabled, flow control ability depends on software configuration.

4.3. Half Duplex Flow Control

When PHY port work as 10/100M half duplex modes, it will collide with the link partner when transmit and receive data at the same time. Then this will make the buffer over flow and drop packets. YT9215RB support two methods, jam mode and defer mode, to avoid this from happening.

The maximum retry count limitation is 16 defined in IEEE 802.3. But for YT9215RB the retry count limitation is configurable, and will not drop packet by default.

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Table 29. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	–	+125	℃
Storage Temperature	−45	+125	℃
DVDDIO, DVDDIO_1, DVDDIO_2, AVDDH, Supply Referenced to GND and AGND	GND−0.3	+3.70	V
DVDDL, AVDDL_1, PLLVDDL, Supply Referenced to GND, AGND, and PLLGND	GND−0.3	+1.40	V
Digital Input Voltage	GND−0.3	VDDIO+0.3	V

5.2. Recommended Operating Range

Table 30. Recommended Operating Range

Parameter		Min	TYP	Max	Units
Ambient Operating Temperature(Ta)		0	–	70	℃
AVDDH Supply Voltage Range		3.135	3.3	3.63	V
DVDDIO Supply Voltage Range	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
DVDDIO_1 Supply Voltage Range(DVDDIO_1: Extension Port 2 Supports 1.8V,2.5V,3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.62	1.8	1.98	V
DVDDIO_2 Supply Voltage Range(DVDDIO_2: Extension Port 2 Supports 1.8V,2.5V,3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.62	1.8	1.98	V
DVDDL,AVDDL,PLLVDDL Supply Voltage Range		1.045	1.1	1.32	V

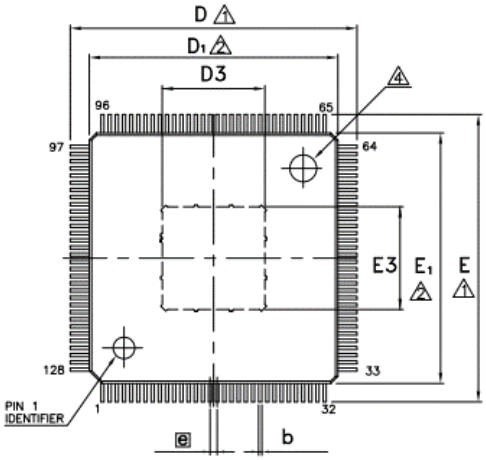
5.3. DC Characteristics

Table 31. DC Characteristics

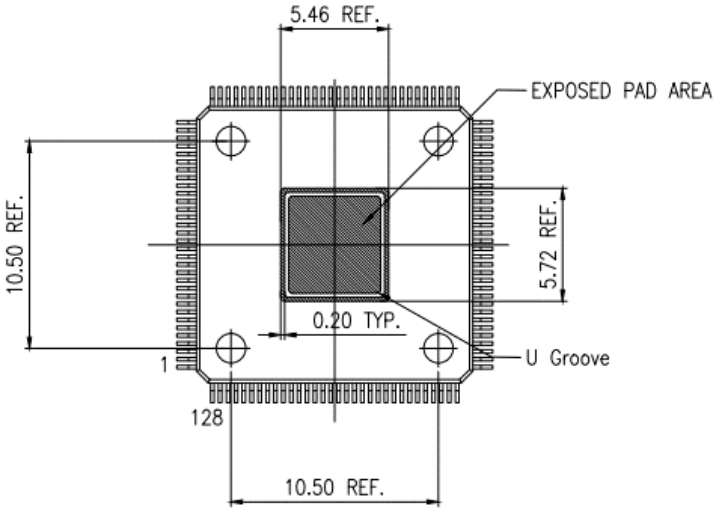
Symbol	Parameter	Min	Typ	Max	Units
Voh (3.3V)	Minimum High Level Output Voltage	2.4	–	3.63	V
Vol (3.3V)	Maximum Low Level Output Voltage	−0.3	–	0.4	V
Vih (3.3V)	Minimum High Level Input Voltage	2	–	–	V
Vil (3.3V)	Maximum Low Level Input Voltage	–	–	0.8	V
Voh (2.5V)	Minimum High Level Output Voltage	2	–	2.8	V
Vol (2.5V)	Maximum Low Level Output Voltage	−0.3	–	0.4	V
Vih (2.5V)	Minimum High Level Input Voltage	1.7	–	–	V
Vil (2.5V)	Maximum Low Level Input Voltage	–	–	0.7	V
Voh (1.8V)	Minimum High Level Output Voltage	1.62	–	2.1	V
Vol (1.8V)	Maximum Low Level Output Voltage	−0.3	–	0.4	V
Vih (1.8V)	Minimum High Level Input Voltage	1.2	–	–	V
Vil (1.8V)	Maximum Low Level Input Voltage	–	–	0.5	V

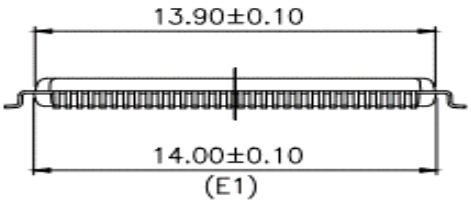
6. Mechanical Information

Top View



Bottom View





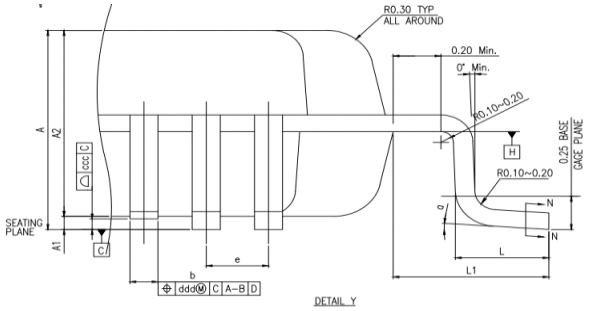


Table 32. Mechanical Dimensions in mm

	SYMBOL	MIN	NOM	MAX
OVERALL HEIGHT	A	–	–	1.6
STANDOFF	A1	–	–	0.127
PKG THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH	b	0.13	0.18	0.23
LEAD TIP TO TIP	D	15.85	16	16.15
LEAD TIP TO TIP	E	15.85	16	16.15
PKG LENGTH	D1	13.9	14	14.1
PKG WIDTH	E1	13.9	14	14.1
	E-PAD	5.72 REF x5.46 REF.		
LEAD PITCH	e	0.4BSC		
FOOT LENGTH	L	0.45	0.6	0.75
LEAD LENGTH	L1	1.0 REF.		

7. Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 33. Pin Assignment

Part Number	Grade	Package	Pack	Status	Operation Temp
YT9215RB	Consumer	LQFP128-E	Tray 900ea		0~70℃
YT9215RBH	Industrial	LQFP128-E	Tray 900ea		-40~85℃