裕太微电子
Motorcomm

Motorcomm

YT6801/ YT6801S Datasheet

INTEGRATED 10/100/1000M GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

VERSION V1.01

DATE 2022-12-08

1. General Description

The YT6801/YT6801S is a single gigabit port Ethernet controller. It integrates IEEE802.3 Ethernet media access controller (MAC), single triple-speed physical layer (PHY) port, One Time Programmable (OTP) and PCI Express x1 controller. It is highly compacted to 32 pin QFN 4x4 package.

The embedded PHY is fully IEEE 802.3 standard compliant which supports 1000Base-T, 100Base-TX and 10Base-Te. With AFE, DFE, echo canceller, cross-talk canceller, packets transmit and receive at 1000Mbps rate with no error over 100m or longer CAT.5E cable. Besides, good ESD/Surge performance is also achieved due to the robust analog design. Other features, such as Auto-Crossover, polarity correction and EEE/smart-EEE are also supported.

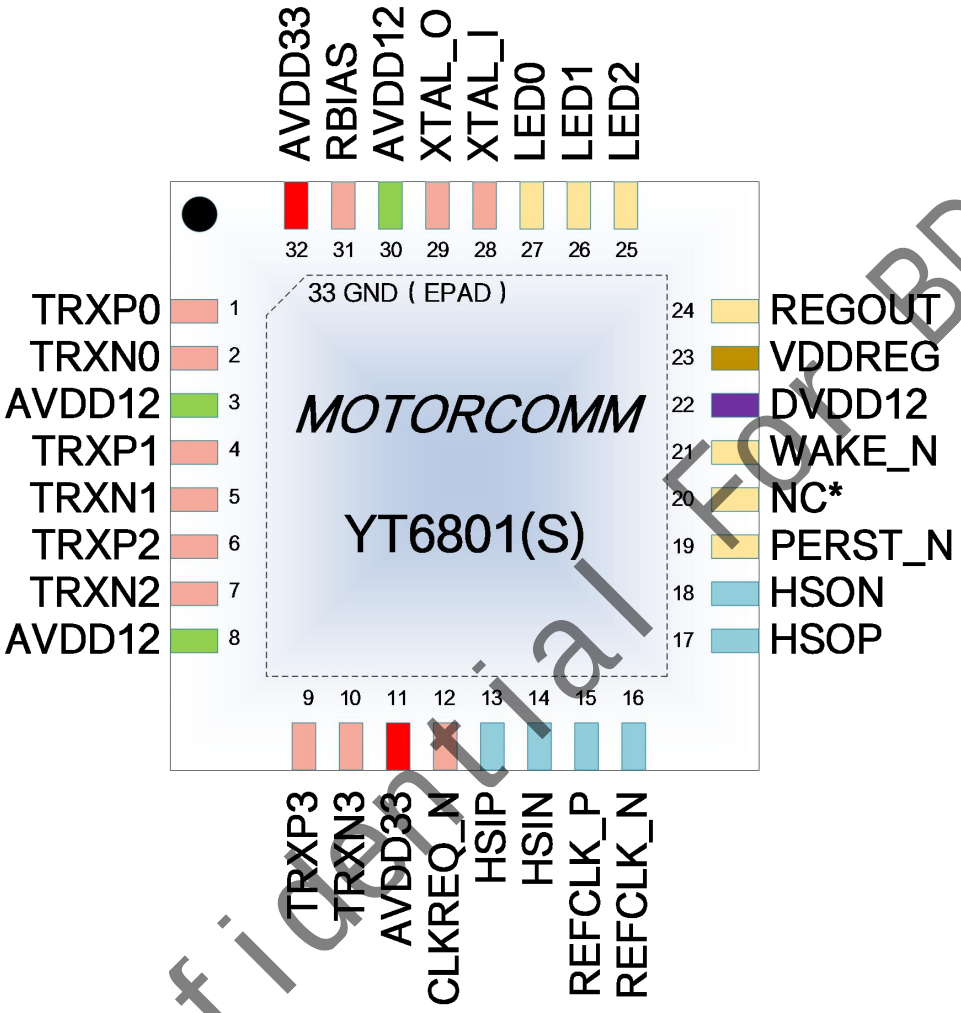
The MAC supports full duplex and half duplex modes. Flow control is supported. It also introduces rich protocol offload functions: ARP/NS offload, TCP large send offload, TCP/UDP checksum offload, IPV4/IPV6 checksum offload. Receive-Side scaling (RSS) is supported to balance the loading of CPUs. Customer can remote wake up PC with WOL function which supports frame pattern matching, magic packet, link change and Microsoft WPI.

The PCIe 1.1 controller is enhanced to support various power states, including L0, L1, L1SS, L2 and L3. Together with ASPM/ACPI function, the whole system could enter various low power states, such as Sleep, Hibernation and Modern Stand-by, to save more power. And the controller supports Latency Tolerance Reporting (LTR). MSI and MSI-X are also supported.

Only 1 external power rail (3.3V) is needed. Analog and digital core power are generated by the built-in LDO (YT6801) and SWR regulator (YT6801S).

4. Pin Assignment

4.1. YT6801(S) QFN32



Note:
The same color system represents the same power domain.
Red: AVDD33: Analog power 3.3V.
Yellow: VDDREG: Digital power 3.3V.
Blue: DVDD12 or AVDD12: Digital or Analog power 1.2V.
Green: AVDD12: Analog power 1.2V.
Purple: DVDD12: Digital power 1.2V.

**Note:*
Pin 20 is NC, which means no connection.

Figure 2. Pin Assignment Diagram

4.2. Pin Assignment

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Power
- G: Ground
- OD: Open Drain
- PU: Internal pull up
- PD: Internal pull down
- I_c: 1.8V/3.3V compatible input

Table 1. Pin Assignment

No.	Pin Name	Type
1	TRXP0	IO
2	TRXN0	IO
3	AVDD12	P
4	TRXP1	IO
5	TRXN1	IO
6	TRXP2	IO
7	TRXN2	IO
8	AVDD12	P
9	TRXP3	IO
10	TRXN3	IO
11	AVDD33	P
12	CLKREQ_N	I_c/OD/PU
13	HSIP	I
14	HSIN	I
15	REFCLK_P	I
16	REFCLK_N	I

No.	Pin Name	Type
17	HSOP	O
18	HSON	O
19	PERST_N	I_c/PD
20	NC	
21	WAKE_N	I_c/OD/PU
22	DVDD12	P
23	VDDREG	P
24	REGOUT	O
25	LED2	O/PD
26	LED1	O/PD
27	LED0	O/PU
28	XTAL_I	I
29	XTAL_O	IO
30	AVDD12	P
31	RBIAS	I
32	AVDD33	P
33	GND	G

8. Timing and DC Characteristics

8.1. DC Characteristics

Table 13. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AVDD33	3.3V Supply Mean Voltage	-	2.97	3.3	3.63	V
AVDD12, DVDD12	1.2V Supply Mean Voltage	-	1.08	1.2	1.32	V
Voh	Minimum High Level Output Voltage	Ioh = -4mA	0.9*VDD33	-	AVDD33	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	0	-	0.1*AVDD33	V
Vih	Minimum High Level Input Voltage for 3.3V & 1.8 V compatible Pinout	-	1.50	-	-	V
	Minimum High Level Input Voltage for 3.3V only Pinout	-	2	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V

8.2. Crystal Requirements

Table 14. Crystal Requirements

Symbol	Description/ Condition	Min	Typ	Max	Units
Fref	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type	-	25	-	MHz
Fref Stability	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. Ta=0°C~70°C	-30	-	+30	ppm
Fref Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. Ta=25°C	-50	-	+50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm

DL	Drive Level	–	–	0.3	mW

8.3. Oscillator Requirements

Table 15. Oscillator Requirements

Parameter	Condition	Min	Typ	Max	Units
Frequency	–	–	25	–	MHz
Frequency Stability	Ta=0°C~70°C	-30	–	+30	ppm
Frequency Tolerance	Ta=25°C	-50	–	+50	ppm
Duty Cycle	–	40	–	60	%
Broadband Peak-to-Peak Jitter	–	–	–	200	ps
Vih	–	1.4	–	–	V
Vil	–	–	–	0.4	V
Rise Time	–	–	–	10	ns
Fall Time	–	–	–	10	ns
Operation Temp Range	–	0	–	70	℃

9. PCI Express Bus Parameters

9.1. Differential Transmitter Parameters

Table 16. Differential Transmitter Parameters

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.80	-	1.20	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eve Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between The Jitter Median and Maximum Deviation from The Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+	ps

				2*UI	
C_{TX}	AC Coupling Capacitor	75	–	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	–	1	ms

Note 1: For the correct measurement environment settings for each parameter, refer to the PCI Express Base Specification, Revision 1.1.

Note 2: The data rate can be modulated with an SSC (spread spectrum clock) of +0 to −0.5% of the nominal data rate frequency, with a modulation rate in the range of no more than 30kHz−33kHz. The ± 300ppm requirement still exists, which requires modulation of both communication ports so that the total difference does not exceed 600ppm.

10. Power Requirements

10.1. Absolute Maximum Ratings

Table 19. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
AVDD33	Supply Voltage 3.3V	−0.3	3.7	V
AVDD12; DVDD12	Supply Voltage 1.2V	−0.2	1.4	V
3.3V DCinput 3.3V DCoutput	Input Voltage Output Voltage	−0.3	3.7	V
1.2V DCinput 1.2V DCoutput	Input Voltage Output Voltage	−0.3	1.4	V
N/A	Storage Temperature	−55	+125	℃

10.2. Recommended Operating Conditions

Table 20. Recommended Operating Conditions

Description	Pins	Min	Typ	Max	Units
Supply Voltage	AVDD33	2.97	3.3	3.63	V
	AVDD12; DVDD12	1.08	1.2	1.32	V
Ambient Operating Temperature Ta		0	–	70	℃
Maximum Junction Temperature		–	–	125	℃

10.3. Power Sequence

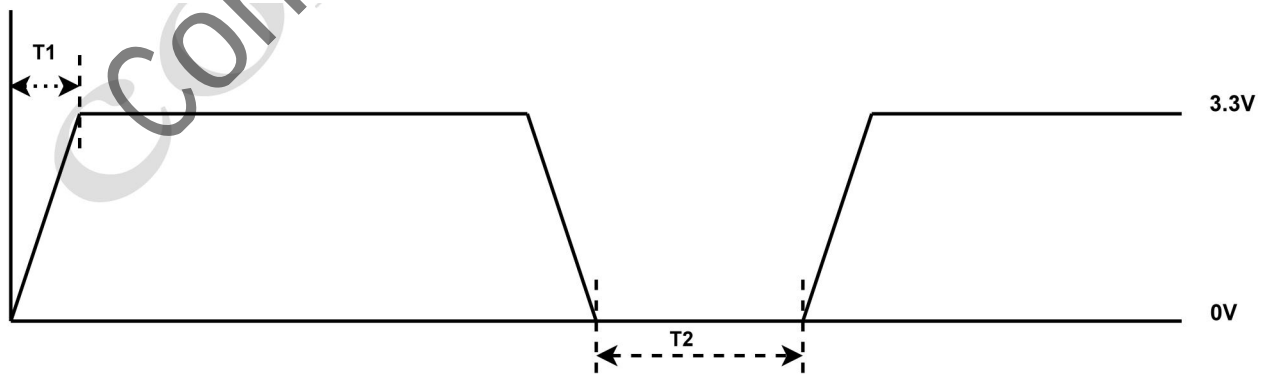


Figure 3. Power Sequence

Table 21. Power Sequence Parameters

Symbol	Description	Min	Typ	Max	Units
T1	3.3V rising time	0.5	–	100	ms
T2	3.3V off time	100	–	–	ms

10.4. Power Consumption

Table 22. YT6801 Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Link Down	49	106	511
Traffic @1000Mbps	91	228	1052

Table 23. YT6801S Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Link Down	48	46	310
Traffic @1000Mbps	89	112	663

10.5. Maximum Power Consumption

Table 24. YT6801 Maximum Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Traffic @1000Mbps	96	255	1158.3

Table 25. YT6801S Maximum Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Traffic @1000Mbps	95	130	742.5

Note: Test by YT6801/YT6801S FF corner IC in 1000Mbps bidirectional traffic mode with AVDD33/VDDREG = 3.3V at high temperature 85℃.

12. Mechanical Information

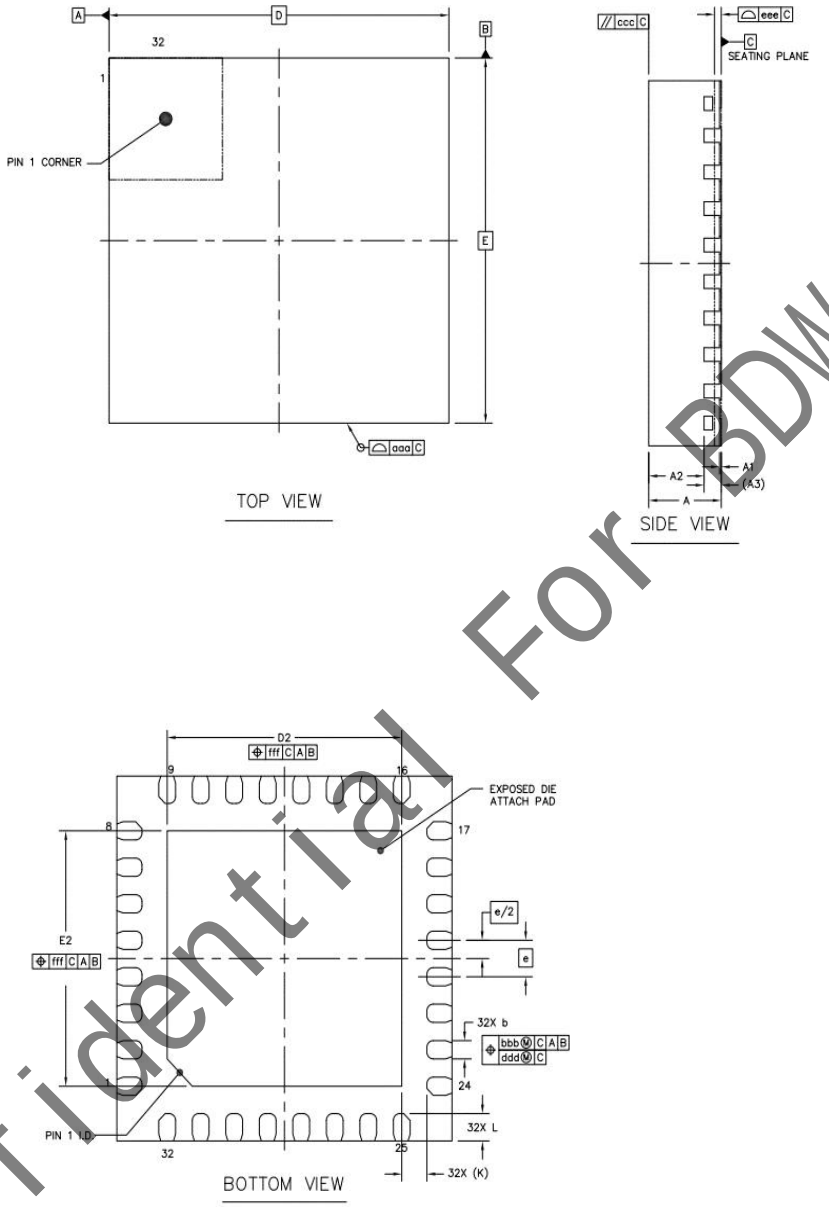


Figure 4. Package Outline Drawing

Table 28. Mechanical Dimensions in mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	4 BSC		
	Y	E	4 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	2.6	2.75	2.9
	Y	E2	2.6	2.75	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K	0.3	0.35	0.4

13. Ordering Information

Table 29. Ordering Information

Part number	Grade	Package	Pack	Status
YT6801S	Consumer	QFN32 EPAD	Tape Reel 3000 ea	Mass Product
YT6801	Consumer	QFN32 EPAD	Tape Reel 3000 ea	Mass Product
YT6801SH	Industrial	QFN32 EPAD	Tape Reel 3000 ea	Engineering Sample