2.75V - 42V, Low I_Q, LDO Linear Regulator

FEATURES

- Low I_Q < 35μA
- Wide Input Voltage Range: 2.75V to 42V
- ±2%, 3.3V, 5V and 15V Fixed Outputs and 0.6V to 24V Adjustable Output
- Up to 250mA Output Current
- Shutdown Current < 3μA
- PG Indicator with Adjustable Delay for MCU Applications
- High PSRR 70dB @ 100Hz
- Stable Close-Loop Operation with only 1μF Low ESR Ceramic Output Capacitor
- Low Dropout: 160mV @ 100mA
- Up to 42V High Voltage EN Pin with Logic Threshold
- Over-Current Protection
- Over Temperature Shutdown and Auto Restart
- Internal Soft Start
- -40˚C to 150˚C Junction Temperature
- Thermally Enhanced ESOP-8 Package

APPLICATIONS

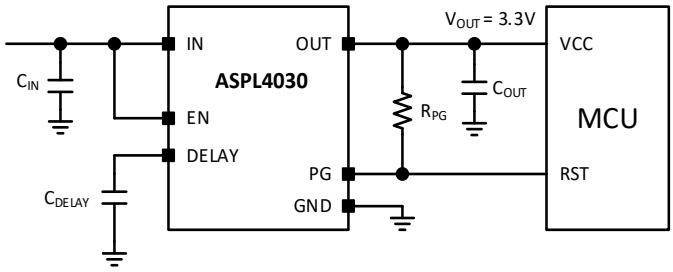
- Automotive Power Supplies
- Industrial Power Supplies
- Battery Powered Systems

DESCRIPTION

ASPL4030 are low quiescent current, low dropout linear regulators (LDOs) with a wide input voltage range of 2.75V to 42V. The series provides 3.3V, 5V and 15V fixed outputs or 0.6V to 24V adjustable output, and delivers up to 250mA output current. The shutdown current of ASPL4030 is less than 3μA, while the quiescent current under no-load condition is less than 35μA.

ASPL4030 provides a power good indicator with programmable delay to directly drive the reset pin of a microprocessor (MCU), moreover, there are options of highly accurate fixed output of 5V or 3.3V or 15V.

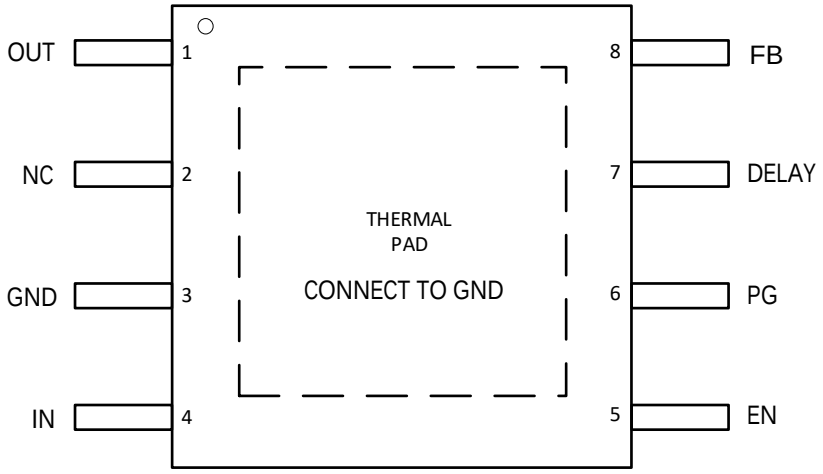
ASPL4030 features over-current protection and over-temperature shutdown with auto restart. The product family is available in thermally enhanced ESOP-8 package.



Typical MCU Application Diagram

PIN CONFIGURATION AND FUNCTION

Pin Configuration



ESOP-8

Pin Function

Name	Number	Description
IN	4	Input pin, place a ceramic capacitor of at least 1μF between IN and GND.
EN	5	Enable pin, connect to a logic control signal or to IN directly.
NC	2	Connect to GND.
GND	3	Connect to GND.
DELAY	7	Power good delay pin, place a ceramic capacitor between DELAY and GND.
PG	6	Power good pin, open drain, connect a pull-up resistor between PG and an external supply or to OUT pin, if not used, keep floating.
FB	8	Feedback pin, connect to the center leg of the voltage divider between OUT and GND. This pin has no internal connection for fixed output versions
OUT	1	Output pin, place a ceramic capacitor of at 1μF between OUT and GND.

Package Thermal Parameters

Parameter (1)		ESOP-8	Units
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	58	˚C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	3	˚C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind , 2W loss, and 25 ˚C ambient temperature.

SPECIFICATIONS

Absolute Maximum Ratings

Parameters	Min	Max	Unit
V_{IN}	-0.3	45	V
V_{EN}	-0.3	V_{IN}	
V_{FB}	-0.3	5.5	
V_{PG}	-0.3	5.5	
V_{OUT}	-0.3	V_{IN}	
V_{DELAY}	-0.3	2	
Junction Temperature	-40	150	˚C
Storage Temperature	-55	150	

ESD Ratings

Parameters	Min	Max	Unit
HBM Human Body Model		±3000	V
CDM Charge Device Model		±750	

Recommented Operating Condition

Parameters	Min	Max	Unit
V_{IN}	-0.3	42	V
V_{EN}	-0.3	V_{IN}	
V_{FB}	-0.3	0.7	
V_{PG}	-0.3	5.5	
V_{OUT}	-0.3	V_{IN} - V_{DO}	
V_{DELAY}	-0.3	2	
Junction Temperature	-40	150	˚C

Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 13.5V.

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN, VOUT (IN, OUT, GND PINS)						
V_{IN}	Operating Input Voltage Range		2.75		42	V
V_{OUT}	Operating Output Voltage Range for Adjustable Output		0.6		24	V
I_{Q-SH}	Input Shutdown Current	V_{EN} = 0V, V_{IN} = 13.5V		0.8	3	μA
I_{Q-NL}	Input Quiescent Current with PG Function	V_{EN} = 5V, V_{IN} = 13.5V, I_{OUT} = 0A		11	35	μA
REGULATION, (OUT, FB PINS)						
V_{FB}	Regulated Feedback Voltage	V_{FB} = V_{OUT}, 28V > V_{IN} > 4.3V, IOUTMAX > I_{OUT} > 1mA	0.588	0.6	0.612	V
		V_{FB} = V_{OUT}, 42V > V_{IN} > 28V, 75%*IOUTMAX > I_{OUT} > 1mA				
I_{FB}	Feedback Input Leakage Current	V_{FB} = 0.6V	-0.1	0	0.1	μA
V_{OUT}%	Regulated Output Voltage Error for Fixed V_{OUT} Parts	28V > V_{IN} > V_{OUT} + 1V, IOUTMAX > I_{OUT} > 1mA	-2		2	%
		42V > V_{IN} > 28V, 75%*IOUTMAX > I_{OUT} > 1mA				
	Line Regulation	42V > V_{IN} > V_{OUT} + 1V, 75%*IOUTMAX > I_{OUT} > 1mA		±0.1		%
	Load Regulation	42V > V_{IN} > V_{OUT} + 1V, 75%*IOUTMAX > I_{OUT} > 1mA		±0.5		%
DROP OUT						
$V_{DO-100mA}$	Drop Out Voltage	I_{OUT} = 100mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} >= 5V	160		260	mV
$V_{DO-200mA}$	Drop Out Voltage	I_{OUT} = 200mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} >= 5V	260		400	mV
$V_{DO-100mA-3.3V}$	Drop Out Voltage	I_{OUT} = 100mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} = 3.3V	200		300	mV
$V_{DO-200mA-3.3V}$	Drop Out Voltage	I_{OUT} = 200mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} = 3.3V	300		400	mV

Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 13.5V.

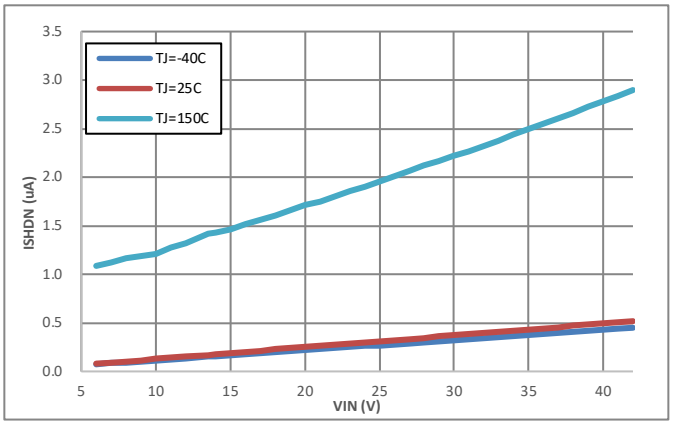
Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVER CURRENT PROTECTION						
I_{LIMIT}	Current Limit Threshold	V_{OUT} = 90% * $V_{OUT-NOM}$, V_{IN} = 13.5V	250	280	500	mA
POWER SUPPLY REJECTION RATIO (PSRR)						
$G_{PSRR-100Hz}$	PSRR@100Hz	I_{OUT} = 50mA, V_{OUT} = 5 V or 3.3V		70 (1)		dB
ENABLE (EN PIN)						
V_{EN}	EN Pin Voltage Range		-0.3		V_{IN}	V
V_{EN-H}	EN Enable Threshold Voltage		1.5			V
V_{EN-L}	EN Disable Threshold Voltage				0.9	V
I_{EN-H}	EN Leakage Current	V_{EN} = 5V	0.5		2	µA
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		151	170 (1)		˚C
	Thermal Shutdown Recovery Hysteresis			13 (1)		˚C
POWER GOOD (PG, DELAY PINS)						
$V_{PG-RISE}$	Power Good Rising Threshold	V_{FB} Ramping Up	87	92.5	98	%
$V_{PG-FALL}$	Power Good Falling Threshold	V_{FB} Ramping Down	83.5	88	92.5	%
R_{PG-DN}	Power Good Internal Pull-Down Resistor	V_{PG} = 1V	180	200	280	Ω
$I_{D-CHARGE}$	Delay Capacitor Charge Current	V_D = 1V	2		18	µA
$I_{D-DISCHARGE}$	Delay Capacitor Discharge Current	V_D = 1V	2		25	mA
V_{D-RISE}	Delay Rising Threshold				0.80	V
V_{D-FALL}	Delay Falling Threshold				0.70	V

(1) Not subject to production test, specified by bench characterization.

Typical Characteristics

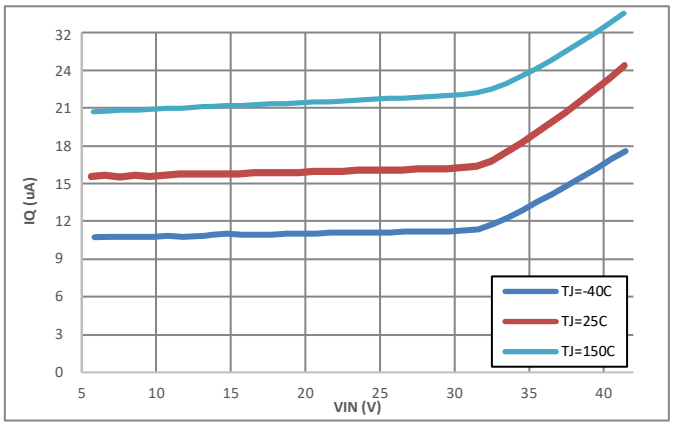
Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as the specification. T_J = -40˚C to 150˚C.



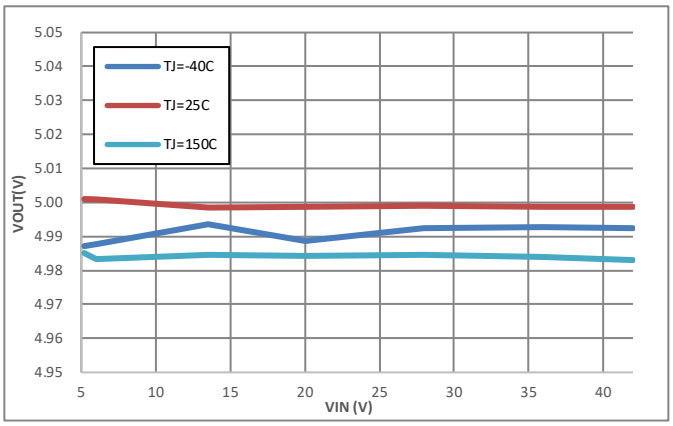
Fixed V_{OUT} = 5V, No load

Figure 1. I_{SHDN}



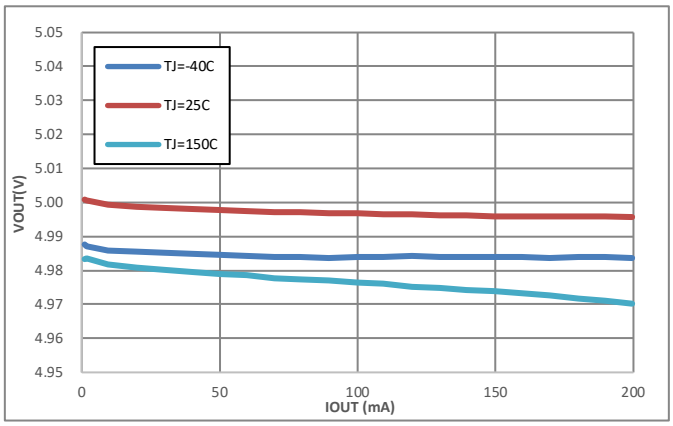
Fixed V_{OUT} = 5V, No load

Figure 2. I_Q



Adjustable V_{OUT} = 5V, I_{OUT} = 1mA

Figure 3. Line Regulation

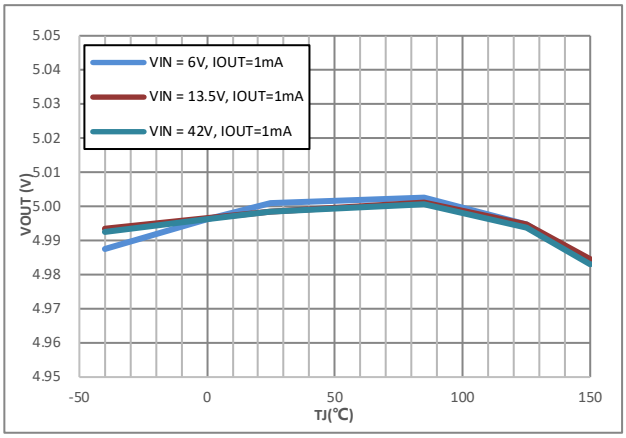


Adjustable V_{OUT} = 5V, V_{IN} = 13.5V

Figure 4. Load Regulation

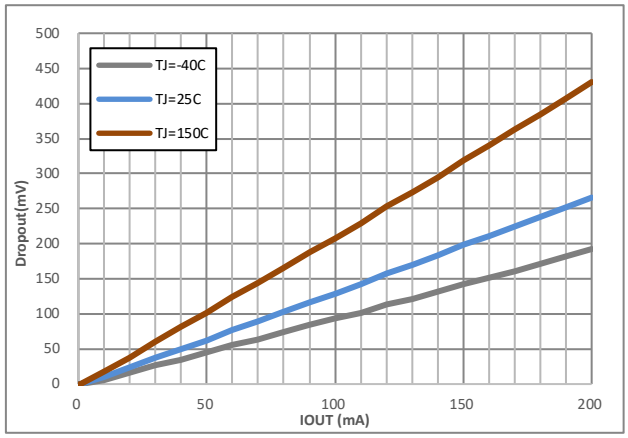
Characteristics Over Temperature (Continued)

Unless otherwise stated, the test conditions are the same as the specification. T_J = -40˚C to 150˚C.



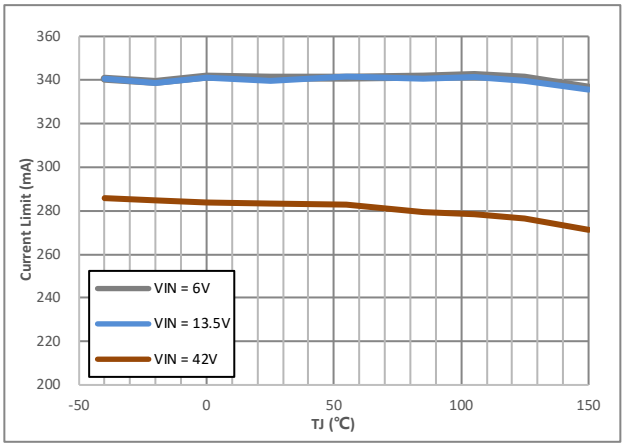
Adjustable V_{OUT} = 5V, I_{OUT} = 1mA

Figure 5. V_{OUT} vs. Temperature



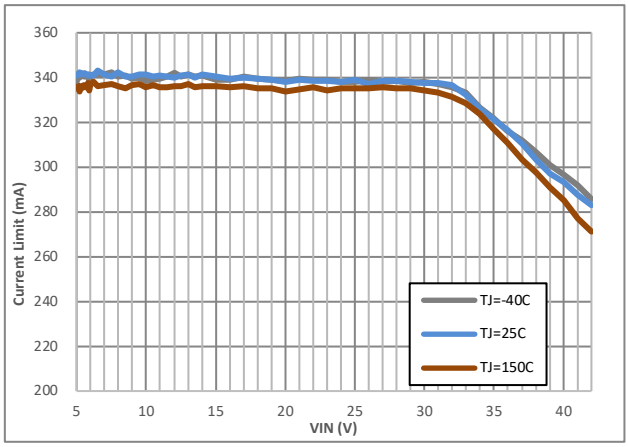
Adjustable V_{OUT} = 5V

Figure 6. Dropout



Fixed V_{OUT} = 5V, Measured at V_{OUT} short

Figure 7. Current Limit vs. Temperature

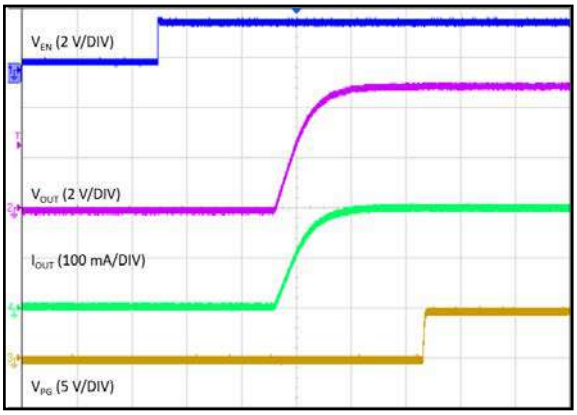


Fixed V_{OUT} = 5V, Measured at V_{OUT} short

Figure 8. Current Limit vs. VIN

Typical Characteristics

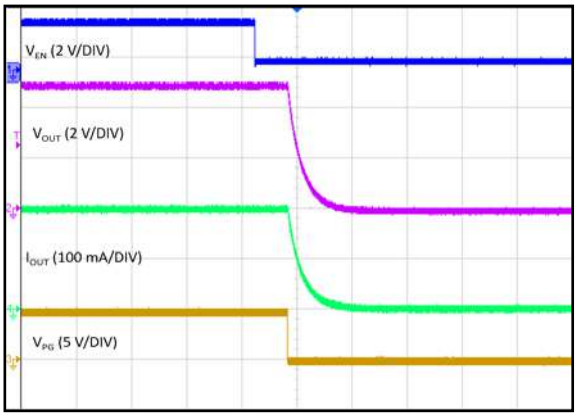
Unless otherwise stated, the test conditions are the same as the specification. T_J = -40˚C to 150˚C.



Time (100µs/DIV)

Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

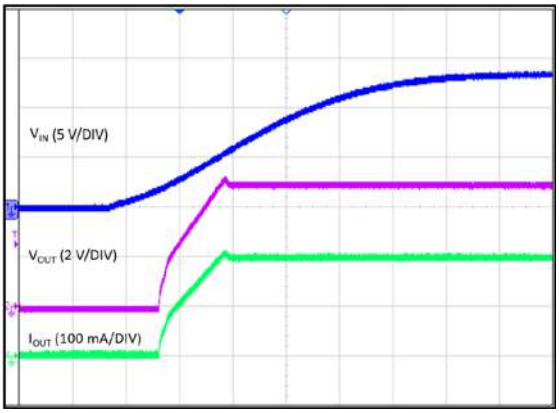
Figure 9. Startup with EN



Time (100µs/DIV)

Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

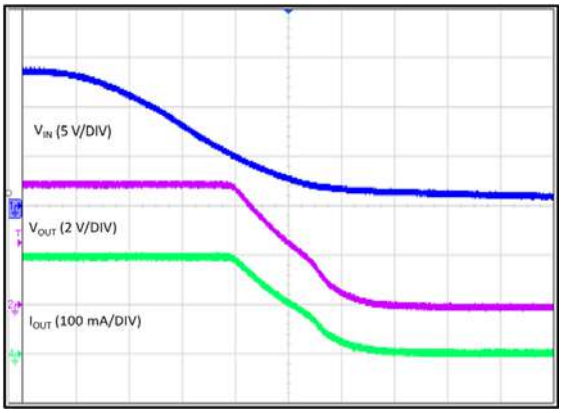
Figure 10. Shutdown with EN



Time (2ms/DIV)

Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

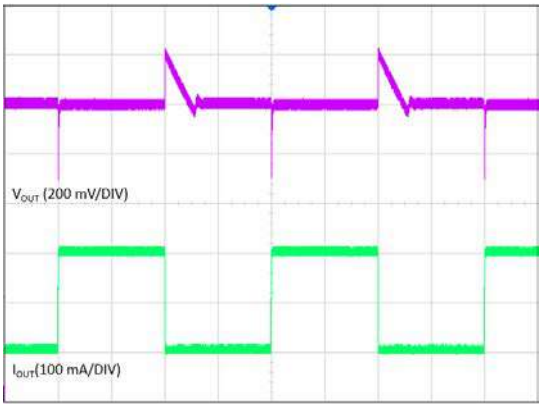
Figure 11. Startup with V_{IN}



Time (2ms/DIV)

Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

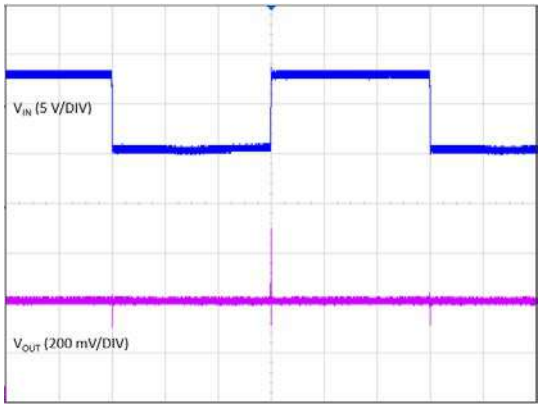
Figure 12. Shutdown with V_{IN}



Time (5ms/DIV)

Fixed V_{OUT} = 5V, V_{IN} = 13.5V, Slew Rate↑↓ = 0.1A/us

Figure 13. Load Transient 0 <-> 200mA



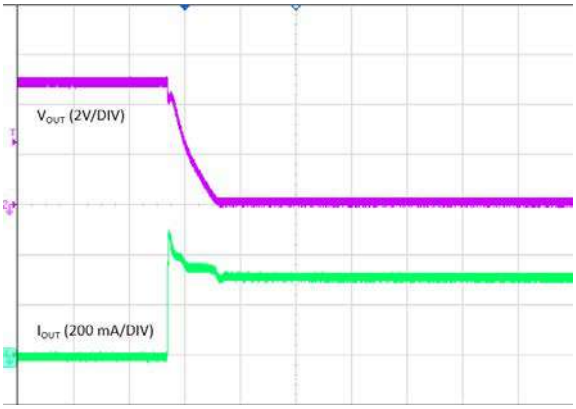
Time (1ms/DIV)

Fixed V_{OUT} = 5V, I_{OUT} = 200mA, Slew Rate↑ = 5V/us

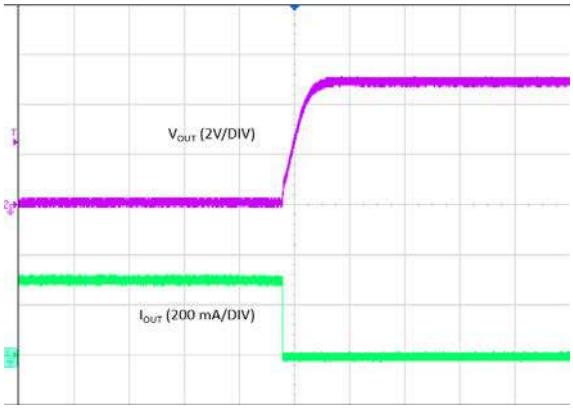
Figure 14. Line Transient 6 <-> 13.5V

Typical Characteristics (Continued)

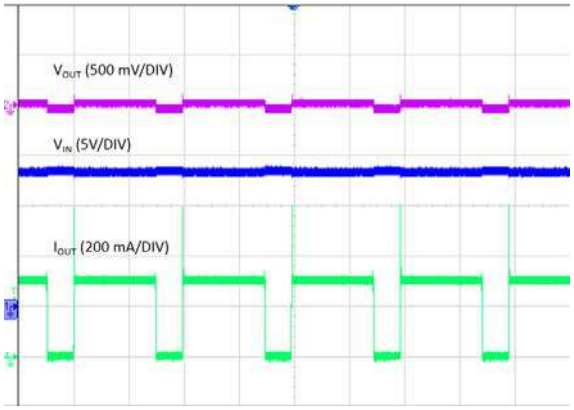
Unless otherwise stated, the test conditions are the same as the specification. T_J = -40˚C to 150˚C.



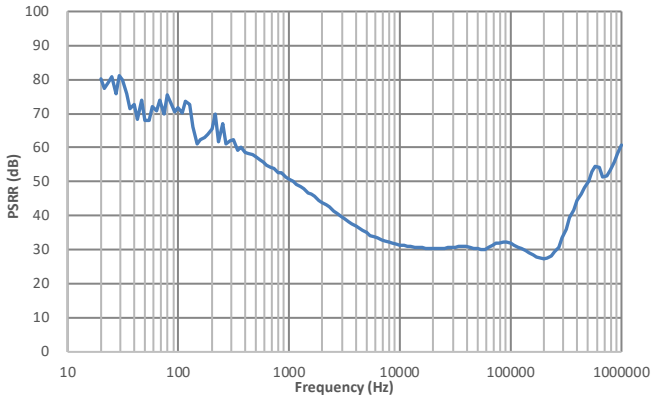
Time (200µs/DIV)
Adjustable V_{OUT} = 5V, V_{IN} = 13.5V
Figure 15. Short Circuit Entry



Time (200µs/DIV)
Adjustable V_{OUT} = 5V, V_{IN} = 13.5V
Figure 16. Short Circuit Recovery



Time (5ms/DIV)
Adjustable V_{OUT} = 5V, V_{IN} = 13.5V
Figure 17. Constant Short Circuit



Adjustable V_{OUT} = 5V, C_{IN} = 100pF, V_{IN} = 6V, I_{OUT} = 10mA
Figure 18. PSRR

FUNCTIONAL DESCRIPTION

Overview

ASPL4030 are low quiescent current, low dropout linear regulators (LDOs) with a wide input voltage range of 2.75V to 42V. The series provides 3.3V, 5V and 15V fixed outputs or 0.6V to 24V adjustable output, and delivers up to 250mA output current. The shutdown current of ASPL4030 is less than 3μA, while the quiescent current under no-load condition is less than 35μA.

ASPL4030 provides a power good indicator with programmable DELAY pin to directly drive the reset pin of a microprocessor (MCU), moreover, there are options of highly accurate fixed output of 5V, 3.3V or 15V.

ASPL4030 features over-current protection and over-temperature shutdown with auto restart. The over-current threshold drops when the input voltage is above 30V.

The product family is available in thermally enhanced ESOP-8 package.

Funtional Diagram

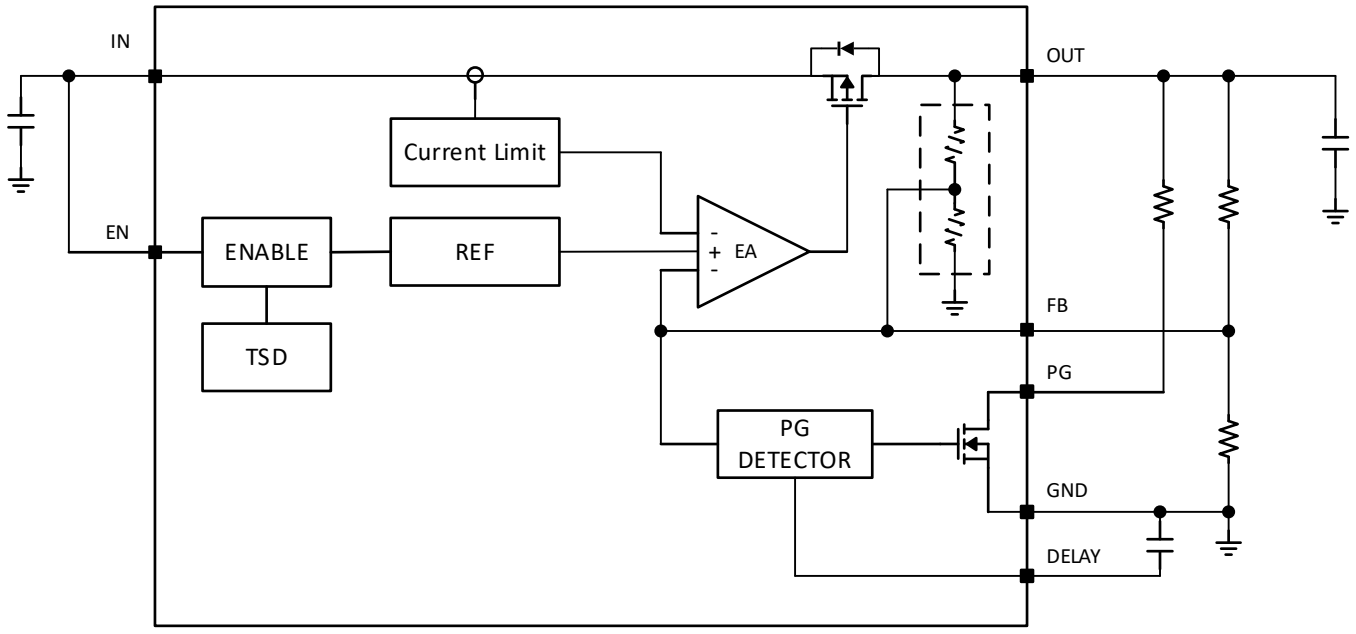


Figure 19. ASPL4030 Functional Diagram

APPLICATIONS

Applicaition Diagram with Full Features

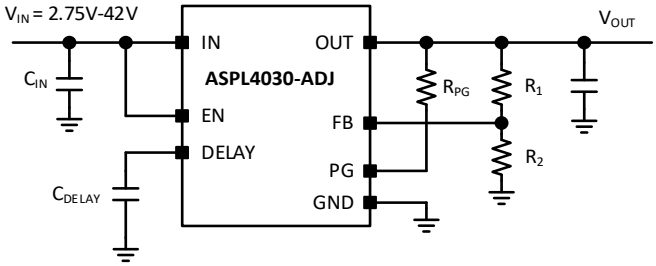


Figure 20. ASPL4030-ADJ with full features

Minimum Application Diagram

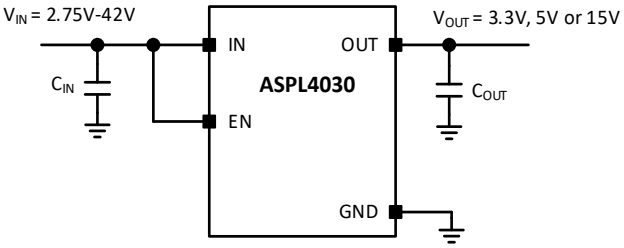


Figure 21. ASPL4030 with minimum external components

Application Considerations

Input and Ouput Decouple Capacitors

For control loop stabilities, ASPL4030 integrates internal compensation and only requires ceramic capacitors with minimum capacitance of 1uF between VIN and GND, and VOUT and GND, respectively. It is recommended that the capacitor is placed as close to the device pins as possible with minimum PCB trace length.

EN Pin

EN is the enable pin of the internal device supply and the output of the LDO. When the voltage on EN pin rises above the rising threshold V_{EN-H}, the LDO output is allowed; and when the voltage on EN falls below the falling threshold V_{EN-L}, the LDO output is disabled and the device goes into shutdown mode. Another way of using EN pin is connecting EN directly to the input voltage, the pin has the same maximum operating voltage of 42V as the LDO input.

OUT

To adjust the output voltage, connect a voltage divider between OUT and GND, and connect the center of the divider to FB pin. The steady state V_{FB} is typically at 0.6V. The output voltage can be derived from:

$$V_{OUT} = (1 + \frac{R_1}{R_2}) \times V_{FB}$$

To fully unitize the low I_Q capability of the product family, it is recommended to use resistors with tolerance better than 1%， and with temperature coefficients less than 100ppm for the divider design. A typical selection of R_2 is 1MΩ, R_1 can then be calculated from:

$$R_1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R_2$$

When using the fixed VOUT products, there is no external divider.

PG and DELAY Pins

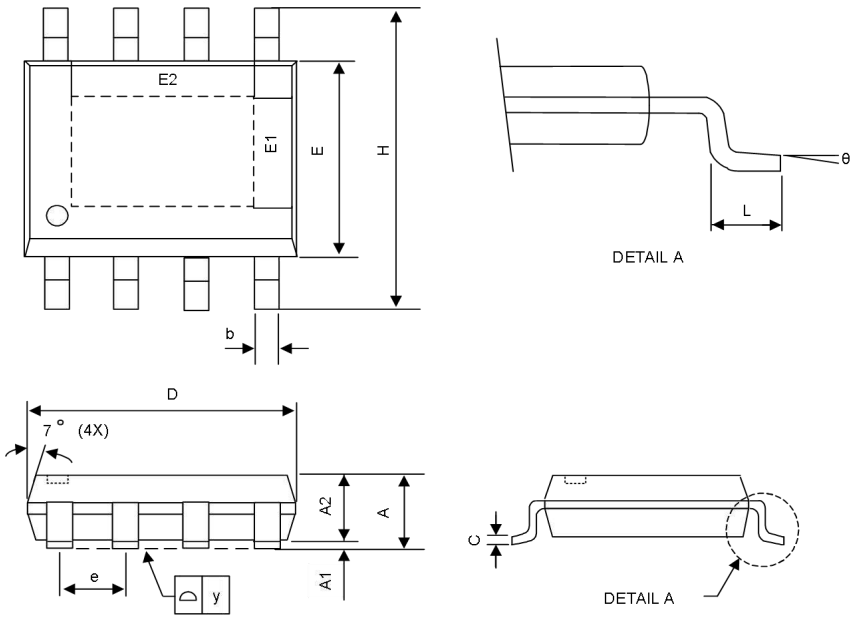
The PG pin is connected to the open drain of an internal N-MOSFET. Externally, the PG pin needs to be pulled up to a voltage source by a resistor. The PG pin can directly drive the reset pin of a MCU. When EN is high and V_{OUT} rises above the power good threshold $V_{PG\text{-}RISE}$, the DELAY pin starts to output a current $I_{D\text{-}Charge}$ to charge the external delay capacitor, when the voltage on the DELAY pin rises across $V_{D\text{-}RISE}$， PG is pulled up. The external delay capacitor is selected based on the desired MCU delay t_{Delay} and is calculated based on:

$$C_{Delay} = \frac{I_{D-Charge} \times t_{Delay}}{V_{D-Rise}}$$

PACKAGE INFORMATION

Package Outline

ESOP-8



REF	Millimeter	
	Min	Max
A		1.75
A1	0.10	0.25
A2	1.25	
C	0.10	0.25
D	4.70	5.10
E	3.70	4.10
H	5.80	6.20
L	0.40	1.27
b	0.31	0.51
e	1.27 BSC	
y		0.10
θ	0	8°
E1	2.20 BSC	
E2	3.30 BSC	

ORDER INFORMATION

Ordering Device No.	Package	Packing	Quantity
ASPL4030-ADJW-R	ESOP-8	Tape&Reel	4000/Reel
ASPL4030-33W-R	ESOP-8	Tape&Reel	4000/Reel
ASPL4030-50W-R	ESOP-8	Tape&Reel	4000/Reel
ASPL4030-150W-R	ESOP-8	Tape&Reel	4000/Reel

Note: ”ADJ, 33, 50, 150” stands for Output Voltage. "ADJ": adjustable output voltage. "33": 3.3V, "50": 5.0V, "150": 15V.
Note: ”W” stands for package. "W": ESOP-8.
Note: ”R” stands for Packing, Tape&Reel.

IMPORTANT NOTICE

ShenZhen Ascend Semiconductor incorporated MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A

PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

ShenZhen Ascend Semiconductor Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. ShenZhen Ascend Semiconductor Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does ShenZhen Ascend Semiconductor Incorporated convey any license under its patent or trademark rights,

nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume .

all risks of such use and will agree to hold Ascendsemi Incorporated and all the companies whose products are represented on ShenZhen Ascend Semiconductor Incorporated website, harmless against all damages.

ShenZhen Ascend Semiconductor Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use ShenZhen Ascend Semiconductor Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold ShenZhen Ascend Semiconductor Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

www.ascendsemi.com